T.O. 33-D7-32-12-2

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9100 Series

Service Manual

P/N 809210
May, 1988

FLUKE ®

LIMITED WARRANTY

John Fluke Mfg. Co., Inc. (Fluke) warrants your 9100/9105A to be free from defects in material and workmanship under normal use and service for 90 days from the date of shipment. Software and firmware products are provided "AS IS." We do not warrant that software or firmware products will be error free, operated without interruption or that all errors will be corrected. This warranty extends to you if you are the original purchaser and does not apply to fuses, batteries or any product which, in our sole opinion, has been subject to misuse, alteration or abnormal conditions of operation or handling.

To obtain warranty service, contact a Fluke Service Center or send the product, with the description of the difficulty, postage prepaid, to the nearest Fluke Service Center. Fluke assumes no risk for damage in transit.

Fluke will, at our option, repair or replace the defective product free of charge. However, if we determine that the failure was caused by misuse, alteration, or abnormal condition of operation or handling, you will be billed for the repair. The repaired product will be returned to you, transportation prepaid.

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SUPPLEMENTAL PARTS LIST

The information in this supplement replaces the parts lists found in the following manual:

MANUAL

Title: 9100 Series Service
Part Number: 809210
Print Date: May 1988
Rev. and Date: ---

Table 5-1. Model Configurations

RELATED PARTS LISTS:

Table	Assembly/Option	9105A Digital Test Station	9100A-011 Video, Color (Table 5-24)	9100A-009 Video, Monochrome (Table 5-23)	9100A-005 Programmer's Station, Color (Table 5-21)	9100A-004 Programmer's Station, Mono	9100A-003 Parallel I/O Module	9100A Digital Test System	9100A/SYS Digital Test Programming Station
5-2	Final Assembly	X						X	X
5-3	A1 Main PCA	X						X	X
5-4	A2 Display Interface PCA	X						X	X
5-5	A4 Video Controller PCA		X	X	X	X			X
5-6	A5 Probe PCA	X						X	X
5-7	A6 Clock Module PCA	X						X	X
5-8	A7 I/O Module (Main) PCA						X		X
5-9	A8 I/O Module (Top) PCA						X		X
5-10	A9 Probe I/O PCA	X						X	X
5-11	A10 Multi-Function I/F PCA							X	X
5-12	A11 I/O Connector PCA	X						X	X
5-13	A12 Half-Width Clip Module								X
5-14	A13 Full-Width Clip Module								X
5-15	A14 Calibration Module						X		X
5-16	A15 Flying Lead Module						X		X
5-17	A16 512K RAM Module*	X						X	X
5-18	A19 Monochrome Monitor			X		X			X
5-19	-003 Parallel I/O Module								X
5-20	-004 Programmer's Station, Mono								X
5-22	-008 Real-Time Clock PCA (optional)	X							
5-25	-013 Programmer's Keyboard				X	X			X

* -007 512K Memory Expansion is included in Table 5-17.

Table 5-2. 9100 Series Final Assembly
(See Figure 5-1.)

REFERENCE DESIGNATOR -A>-NUMERICS--->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE---	TOT QTY-	R S -Q	N O T -E-
A 1	*	MAIN PCA	768754	89536	768754	1		
A 2	*	DISPLAY INTERFACE PCA	768689	89536	768689	1		
A 3		KEYPAD ASSEMBLY	846357	89536	846357	1		
A 5	*	PROBE ASSEMBLY	773911	89536	773911	1		
A 6	*	CLOCK MODULE ASSEMBLY	768812	89536	768812	1		
A 9	*	PROBE I/O INTERFACE PCA	768796	89536	768796	1		
A 10	*	MULTI-FUNCTION INTERFACE PCA	767988	89536	767988	1		1
A 11	*	I/O CONNECTOR PCA	767996	89536	767996	1		
A 16	*	512K RAM MODULE	822858	89536	822858	4		3
A 101		PWR SUP,150W,+5V,(2)+12V,-5V	772988	61852	XL160-3416	1		
A 102	*	DISK DRIVE,FLOPPY,3.5"	829671	89536	829671	1		2
A 104	*	DISK DRIVE,HARD,3.5",FRMTD,20MBYTS	834234	89536	834234	1		1
A 105	*	WINCHESTER HARD DISK CONTROLLER	780940	52840	WD1002S-SHD	1		1
CR 1	*	LED,RED,PCB MNT,LUM INT=0.5MCD	369777	28480	5082-4480	1	1	
E 1		TERM,FASTON,REC,18-22AWG,CRIMP,INSUL	655001	59730	RAD20377	1		
F 1		FUSE,1/4 X 1-1/4,SLOW,2A,250V	109181	71400	MDX2	1	5	
F 1		FUSE,5X20MM,SLOW,1A,250V	808055	61935	034.3117	1	5	
H 1		SPACER,HEX,ALUM,4-40X0.500	192872	COMMERCIAL		1		
H 2		SCREW,MACH,PHP SEMS,STL,4-40X1/4	185918	COMMERCIAL		2		
H 3		SCREW,MACH,PHP,STL,4-40X1/2	558825	COMMERCIAL		4		
H 4		SCREW,MACH,PH,P,STL,6-32X0.250	152140	COMMERCIAL		1		
H 5		NUT,WELD TAB,FLOATING,STEEL,10-32	743393	COMMERCIAL		2		
H 6		SCREW,MACH,PH,P,STL,6-32X0.250	152140	COMMERCIAL		5		
H 7		SCREW,MACH,PH,P,STL,10-32X0.750	114306	COMMERCIAL		2		
H 8		SCREW,MACH,PH,P,STL,6-32X0.250	152140	COMMERCIAL		14		
H 9		SCREW,MACH,PH,P,STL,8-32X0.375	114124	COMMERCIAL		2		
H 10		CONN ACC,D-SUB,LATCH BLOCK,SHORT,SLOT	811653	00779	745245-3	12		
H 11		SCREW,MACH,FIHS,STL,4-40X3/8	129916	COMMERCIAL		12		
H 12		CONN ACC,D-SUB,SLIDING LOCK,POST ASSY	353201	54492	D53018	2		
H 13		CONN ACC,D-SUB,JACK SCREW,4-40	448092	89536	448092	4		
H 14		SCREW,MACH,PH,P,STL,6-32X0.250	152140	COMMERCIAL		4		
H 15		RIVET,PUSH,UNIV,NYL,.16,.32	799957	06915	SR-4080	4		
H 16		SCREW,MACH,PH,P,STL,6-32X0.375	152165	COMMERCIAL		2		
H 17		NUT,CAP EXT LW,STL,6-32X7/64	152819	COMMERCIAL		2		
H 18		DUST FILTER, SET	773994	89536	773994	1		
H 19		WASHER,SHLDR,NYLON,.320X.141X.065	733345	7W423	2703-1865-N141	4		
H 20		RIVET,POP,DOME,AL,0.125X0.440	800763	COMMERCIAL		4		
H 21		FASTENER,STUD REC,TUBLR,0.187 X 0.46	783134	78553	C2694-156-4	2		
H 22		SCREW,MACH,PH,P,STL,6-32X0.250	152140	COMMERCIAL		8		
H 23		SCREW,MACH,PH,P,STL,8-32X0.375	114124	COMMERCIAL		4		
H 24		SCREW,MACH,SEMS,PH,P,STL,6-32X0.375	177022	COMMERCIAL		4		
H 25		SCREW,MACH,PHS,M3 X 12	799502	COMMERCIAL		4		
H 26		SCREW,MACH,PH,P,STL,6-32X0.500	152173	COMMERCIAL		4		
H 27		SCREW,MACH,PH,P,STL,6-32X0.250	152140	COMMERCIAL		2		
H 28		SCREW,MACH,PH,P,STL,6-32X0.250	152140	COMMERCIAL		3		
H 29		SCREW, SHOULDER	775999	89536	775999	2		
H 30		CONN ACC,D-SUB,DUST CAP,37 SCKT	615138	71468	DC-59-20	4		
H 31		CONN ACC,D-SUB,DUST CAP,25 PIN	816371	71468	DB-60-20	2		
H 32		SCREW,MACH,PH,P,STL,4-40X0.250	129890	COMMERCIAL		1		
J 1		CONN,COAX,BNC(F),PANEL	152033	95712	30355-1	1		
MP 1		BOX,MAILER,CONVOLUTED FOAM INSIDE	707851	0DSM7	CPC400	2		
MP 2		DISPLAY WINDOW, SHIELD	784009	89536	784009	1		
MP 3		9100A ACCESSORIES	788554	89536	788554	1	1	
MP 5		SHIELD, CLOCK MODULE	755793	89536	755793	1		
MP 6		CASE, CLOCK MODULE	755827	89536	755827	1		
MP 7		COVER	755686	89536	755686	1		
MP 8		CASE, CLOCK MODULE	755652	89536	755652	1		
MP 10		KEYPAD CASE TOP	765008	89536	765008	1		
MP 11		KEYTOP, SET	775858	89536	775858	1		
MP 12		KEYPAD, ELASTOMERIC	764910	89536	764910	1	1	
MP 13		CORD,LINE,5-15/IEC,3-18AWG,SVT	343723	70903	17237	1		
MP 14		TORSION SPRING	784025	89536	784025	2	1	
MP 15		KEYPAD CASE BOTTOM	765016	89536	765016	1		
MP 16		SPRING DETENT	765032	89536	765032	2		
MP 17		NAMEPLATE	787275	89536	787275	1		
MP 18		FRONT PANEL, PAINTED	764894	89536	764894	1		
MP 19		LENS	783993	89536	783993	1		4
MP 20		KEYPAD OPENING SHIELD	767889	89536	767889	1		
MP 21		HINGE/DETENT HOUSING	765024	89536	765024	2		
MP 22		MAINFRAME BASE	767848	89536	767848	1		

An * in 'S' column indicates a static-sensitive part.

Table 5-2. 9100 Series Final Assembly (cont.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-	TOT QTY	R S Q	NOTE
MP 24		DECAL, CHASSIS CONNECTOR	803221	89536	803221	1		
MP 25		FOOT,VINYL,NYL.PUSH RIVET,0.787X0.236	801001	06915	FF-008-P4X7	4		
MP 26		REAR PANEL	767855	89536	767855	1		
MP 27		HLDR PART,FUSE,CAP,1/4X1-1/4	460238	61935	031.1666	1		
MP 29		EXPANSION SLOT COVER	768010	89536	768010	1		
MP 30		VIDEO SLOT COVER	768655	89536	768655	1		
MP 31		HLDR PART,FUSE,CAP,5X20MM	461020	61935	031.1663	1		
MP 32		CABLE TIE,MOUNT,ADHESIVE,0.19" WIDTH	565036	06383	ABM2S-ATO	1		
MP 33		CABLE TIE,4"L,0.100"W,0.75 DIA	172080	06383	SST1MC	1		
MP 34		SLEEV,POLYOL,SHRINK,.750-.375ID,BLACK	226365	92914	ALPHLEX FIT-221	4		
MP 35		MAINFRAME TOP COVER	773986	89536	773986	1		
MP 36		SHIELD, RFI	768028	89536	768028	1		5
MP 37		LOUVER	787846	89536	787846	1		6
MP 38		POWER SUPPLY SHIELD ASSEMBLY, PLATED	830398	89536	830398	1		
MP 39		CABLE TIE,MOUNT,ADHESIVE,0.19" WIDTH	565036	06383	ABM2S-ATO	1		
MP 40		CABLE TIE,3.62"L,0.091"W,5/8 DIA	381533	06383	PLT1M	1		
MP 41		HARD DISK AND FLOPPY HOUSING	802033	89536	802033	1		7
MP 42		MOUNT,VIBRATION,GROMMET	782623	36000	G-1163T	8		
MP 43		SPACER,NYLON,0.195X0.300	782631	36000	T-306	8		
MP 44		SPACER,PWB,NYL,.125	806703	06915	LMSP-201	2		1
MP 45		NAMEPLATE, SERIAL -REAR PANEL-	472795	89536	472795	1		
MP 46		SYSTEM SOFTWARE, SLEEVED	809103	89536	809103	1		
MP 47		MFI SLOT ESD COVER	819680	89536	819680	1		10
MP 48		REC.MEDIA,DISK,3.5",DSDD,BOX.OF 10	757229	89536	757229	1		
MP 49		CARTON, 9100A	809038	89536	809038	1		
MP 50		END CAP SET, 9100A	809046	89536	809046	1		
MP 51		TRAY/DIVIDERS, 9100A	809053	89536	809053	1		
MP 52		CARTON, PADDED DISK	809129	89536	809129	1		
SW 1		SWITCH,ROTARY,LINE SEL.,DPDT,2 POS.	799551	61935	SWA003.4501	1	1	
SW 2		SWITCH,ROCKER,DPST	800649	62440	232KW20B2C	1	1	
TM 1		9100 SERIES GETTING STARTED MANUAL	787960	89536	787960	1		
TM 2		9100 SERIES AUTOMATED OPERATIONS MAN	809228	89536	809228	1		
TM 3		9100 SERIES TECHNICAL USER'S MANUAL	813832	89536	813832	1		
TM 4		9100 SERIES APPLICATIONS MANUAL	813840	89536	813840	1		
TM 5		SUPPLEMENTAL POD INFO FOR 9100A/9105A	822866	89536	822866	1		
W 3		CABLE, A C POWER CONNECT	749903	89536	749903	1		
W 4		CABLE ASSEMBLY, LINE SELECT	773267	89536	773267	1		
W 5		LINE FILTER ASSEMBLY	773424	89536	773424	1		
W 6		CABLE, PROBE I/O INTERFACE	773432	89536	773432	2		
W 7		CABLE,DISK DRIVE	773846	89536	773846	1		8
W 8		CABLE,DISPLAY INTERFACE	773853	89536	773853	1		
W 9		CABLE,KEYPAD INTERFACE	773861	89536	773861	1		
W 10		CABLE ASSEMBLY, D C HARNESS	773887	89536	773887	1		
W 11		CABLE ASSY, CLOCK MODULE	783969	89536	783969	1		
W 12		CABLE ASSEMBLY, RS232 M	787838	89536	787838	2		
W 13		CABLE ASSEMBLY, HARD DISK TO MFI	787895	89536	787895	1		1
W 15		CABLE, HARD DISK TO CONTROLLER	788448	89536	788448	1		1
W 16		CABLE, HARD DISK TO CONTROL DATA	788455	89536	788455	1		1
W 17		FAN ASSEMBLY	788471	89536	788471	1		
W 18		CABLE ASSEMBLY, BNC	801944	89536	801944	1		
W 19		CABLE ASSEMBLY, MICRO-CLIP	809178	89536	809178	1		
W 21		CABLE, DISK DRIVE POWER	788430	89536	788430	1		9
XF 1		HLDR PART,FUSE,BODY 1/4X1-1/4,5X20MM	460329	61935	031.1673	1		

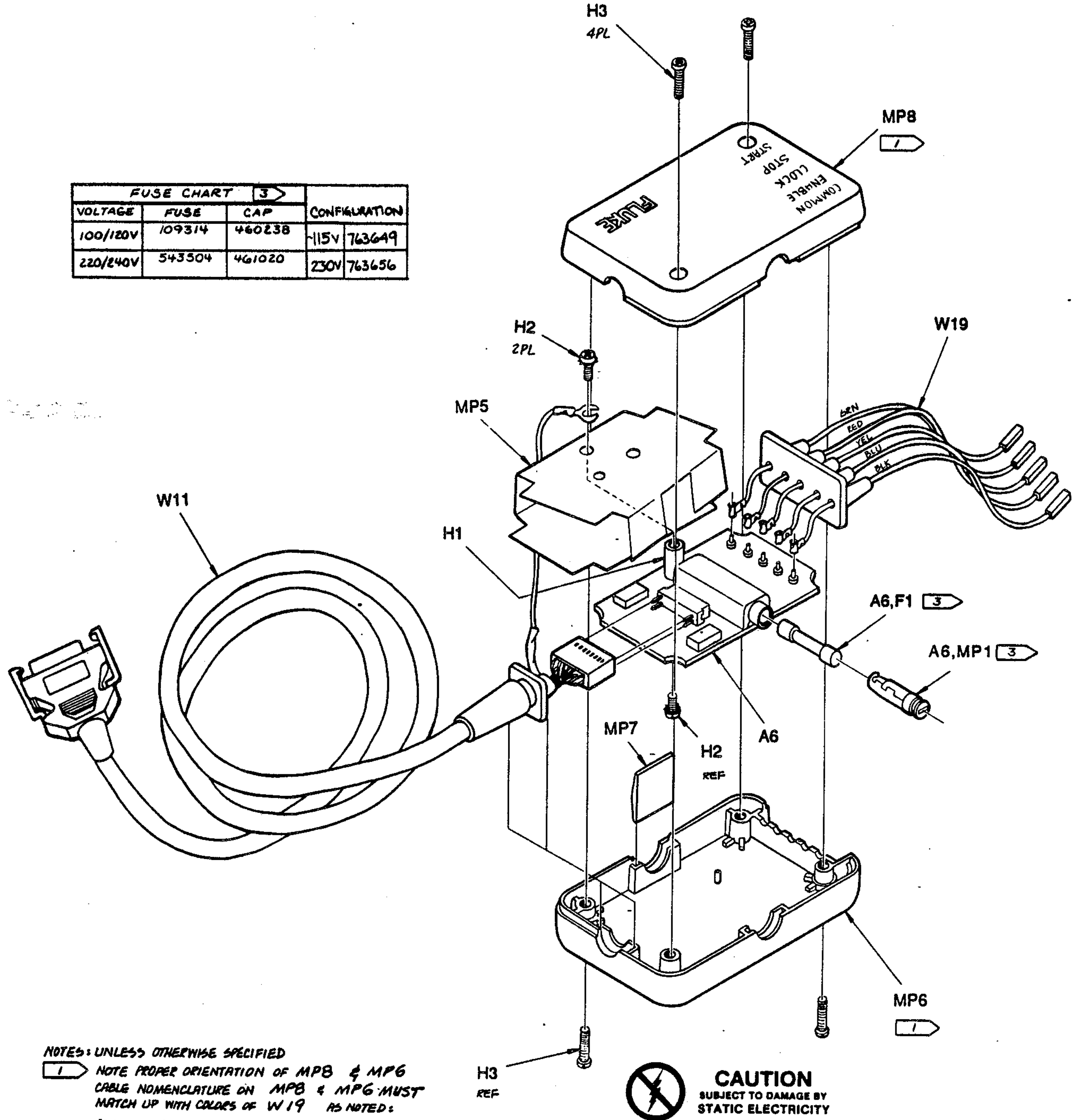
An * in 'S' column indicates a static-sensitive part.

NOTES:

1 - Not used on 9105A.
2 - For 9105A, quantity is 2.
3 - For 9105A S/Ns prior to 4352000, two 512K + two 256K (799833) were used.
4 - For 9105A, order p/n 805721.
5 - For 9105A, order p/n 805713, quantity 2.
6 - For 9105A, order p/n 787853.
7 - For 9105A, order p/n 788521.
8 - For 9105A, order p/n 788547.
9 - For 9105A, order p/n 805705.
10 - For 9105A, order p/n 802009.

A101 through A105 are Original Equipment Manufacturer (OEM) assemblies.
List of replaceable parts is not available.

FUSE CHART 3			CONFIGURATION	
VOLTAGE	FUSE	CAP		
100/120V	109314	460238	115V	763649
220/240V	543504	461020	230V	763656



NOTES: UNLESS OTHERWISE SPECIFIED

1 NOTE PROPER ORIENTATION OF MP8 & MP6 CABLE NOMENCLATURE ON MP8 & MP6 MUST MATCH UP WITH COLORS OF W19 AS NOTED:

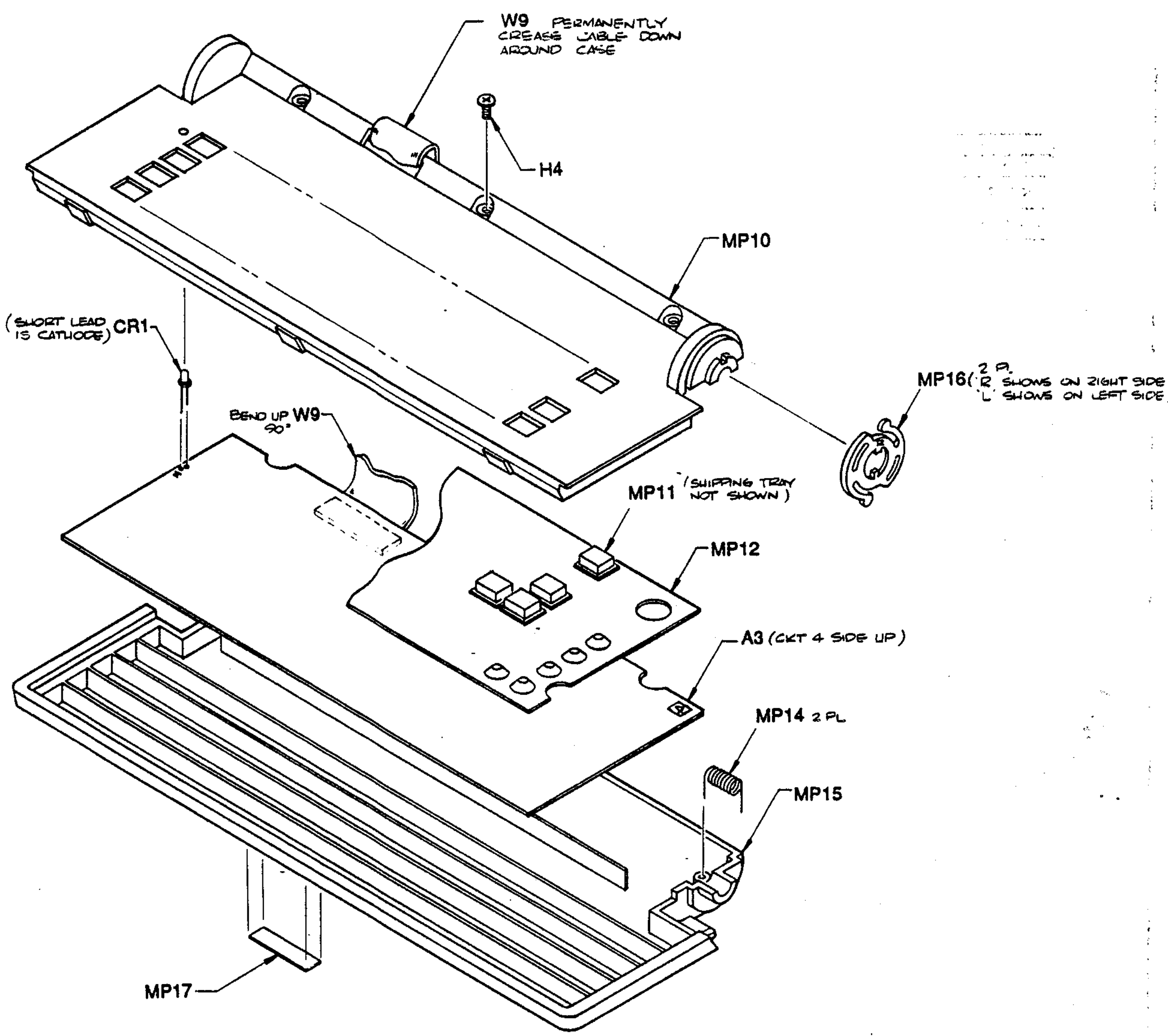
COMMON - BLACK WIRE
UNABLE - BLUE WIRE
CLOCK - YELLOW WIRE
STOP - RED WIRE
START - GREEN WIRE

2. WARNING: Ⓢ INDICATES USAGE OF MOS DEVICE(S) WHICH MAY BE DAMAGED BY STATIC DISCHARGE. USE SPECIAL HANDLING PER S.O.P. 18.1

3 FUSE & FUSE CAP VARY FOR DIFFERENT VOLTAGE CONFIGURATIONS: SEE FUSE CHART FOR FUSE & CAP PART NO.S.

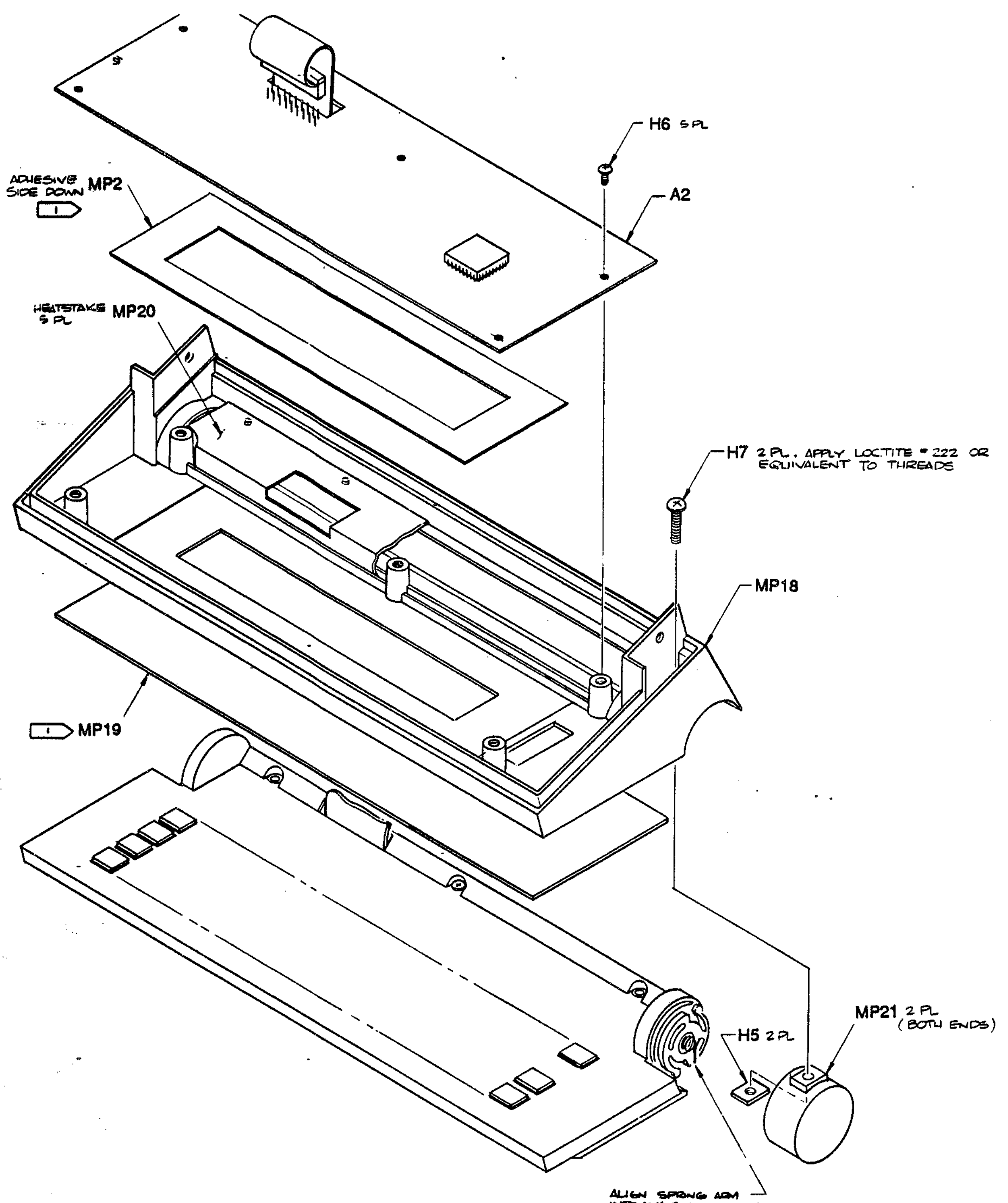
9100A T&B
(1 of 9)

Figure 5-1. 9100 Series Final Assembly



9100A T&B
(2 of 9)

Figure 5-1. 9100 Series Final Assembly (cont.)



NOTES:

1. VIEWING WINDOWS OF MP2 & MP19 TO BE FREE OF FINGERPRINTS & SMUDGES. USE OF WHITE GLOVES RECOMMENDED.

9100A T&B
(3 of 9)

Figure 5-1. 9100 Series Final Assembly (cont.)

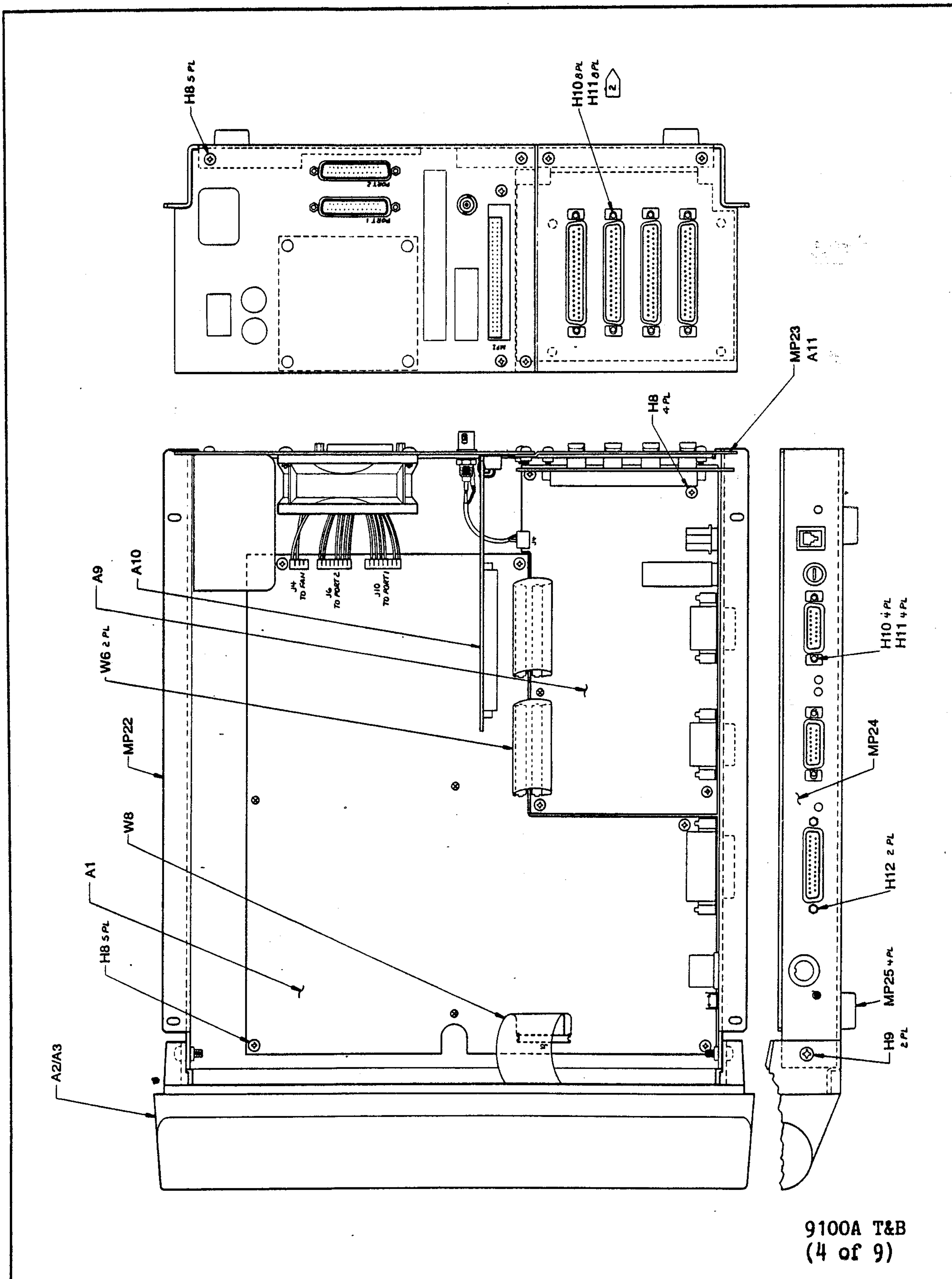


Figure 5-1. 9100 Series Final Assembly (cont.)

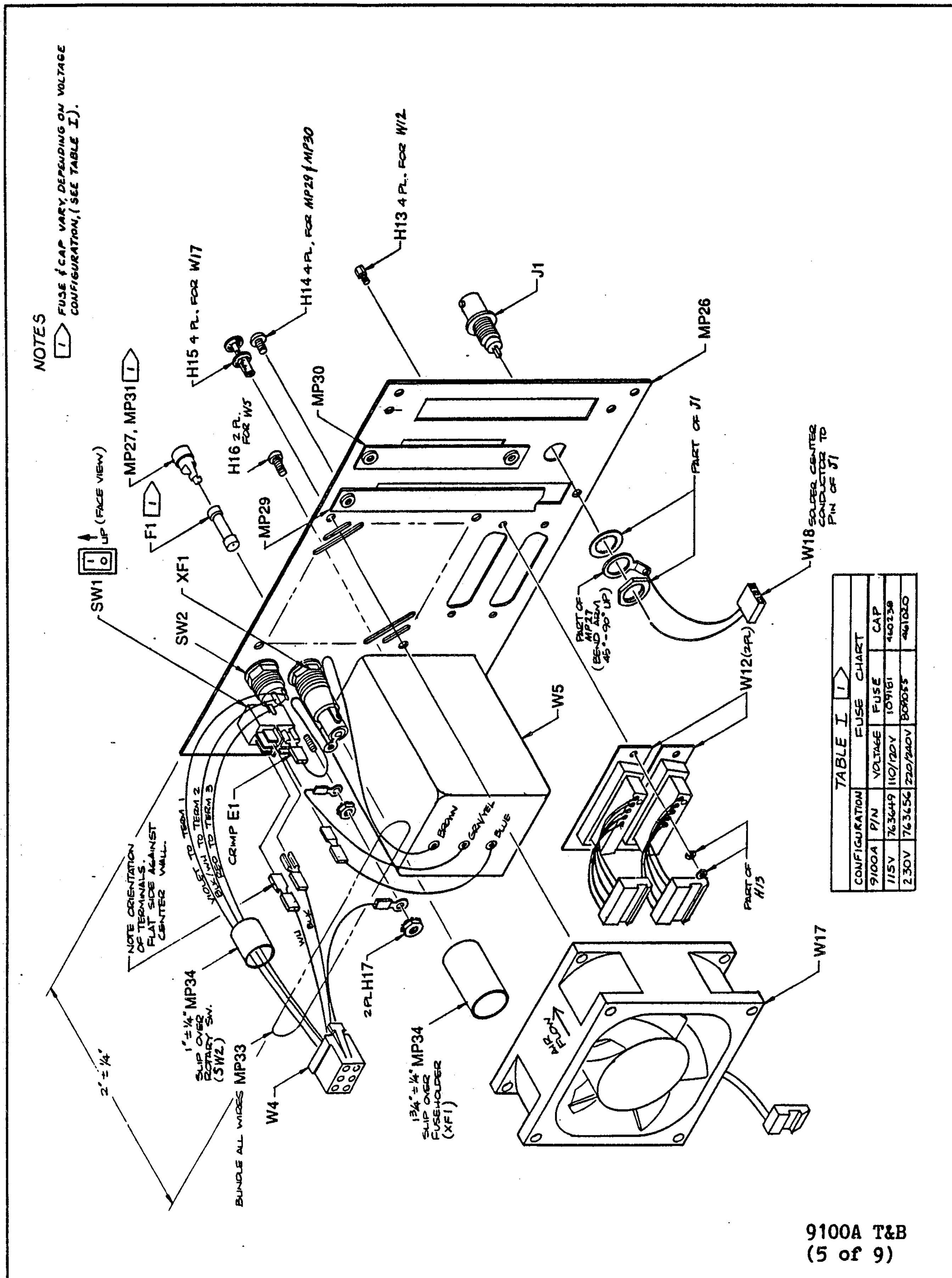
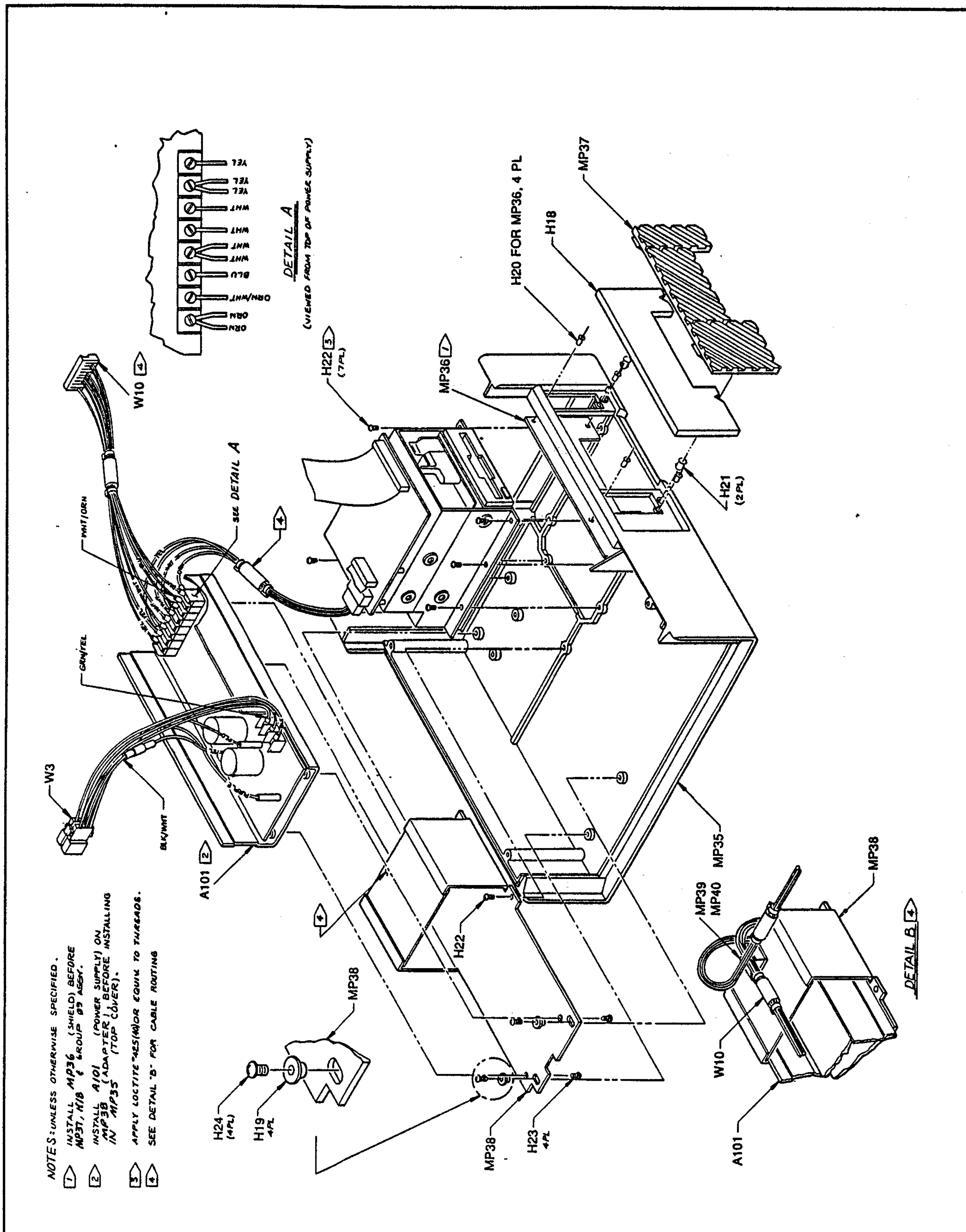


TABLE I — FUSE CHART

CONFIGURATION 9100A	P/N	VOLTAGE	FUSE	CAP
115V	763649	110/120V	109161	460238
230V	763656	220/240V	809055	461020

Figure 5-1. 9100 Series Final Assembly (cont.)



9100A T&B
(6 of 9)

Figure 5-1. 9100 Series Final Assembly (cont.)

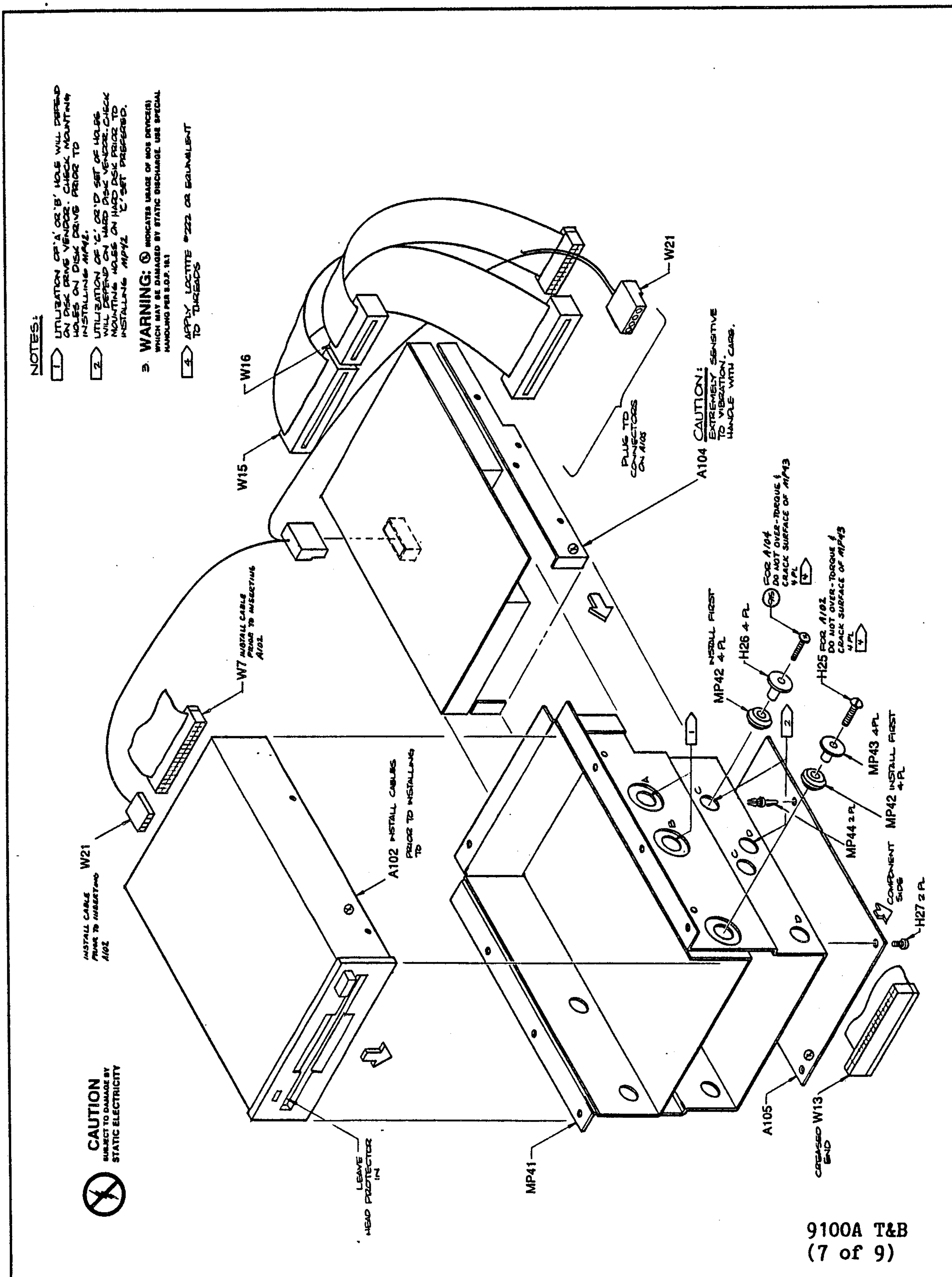


Figure 5-1. 9100 Series Final Assembly (cont.)

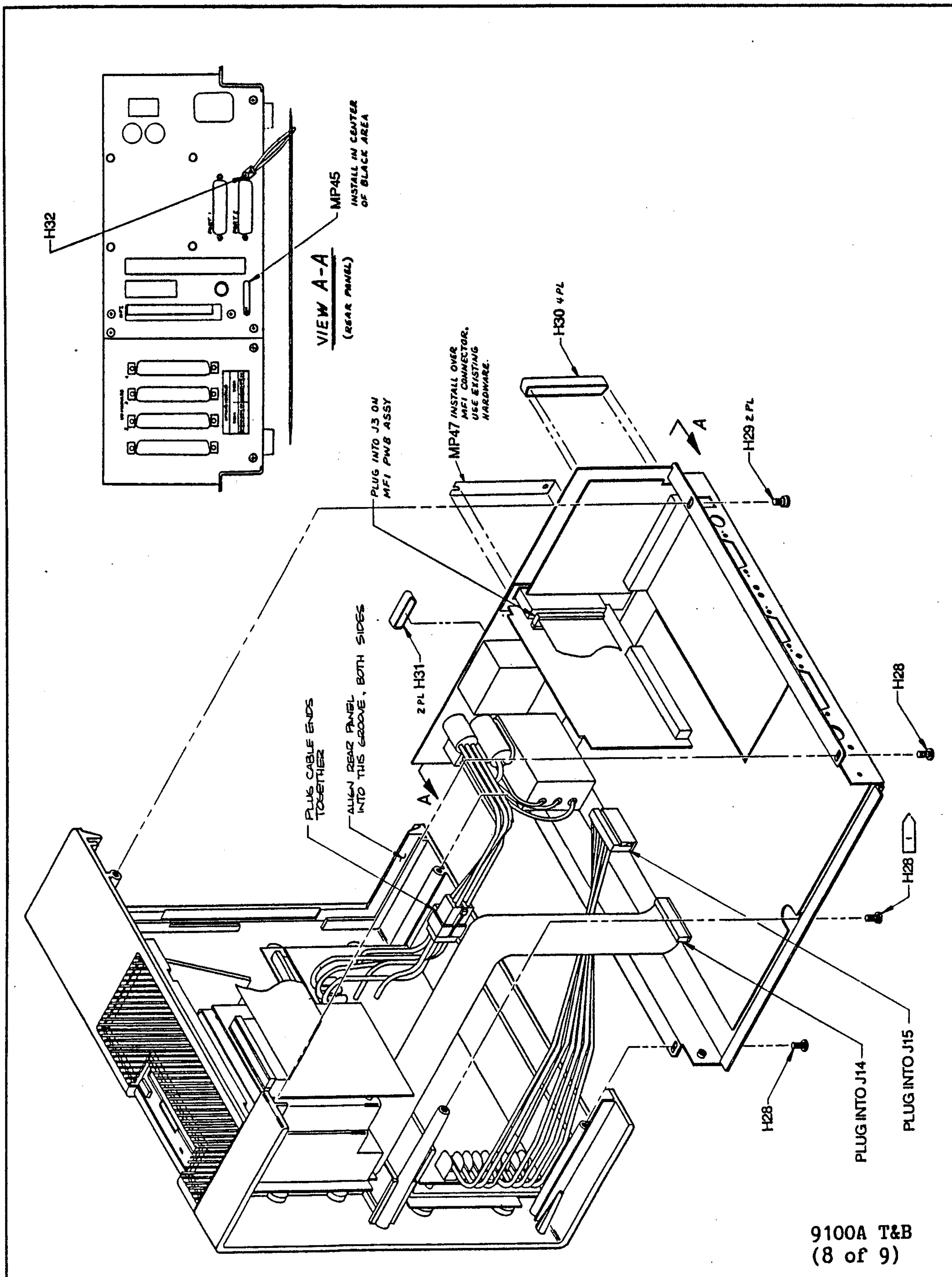
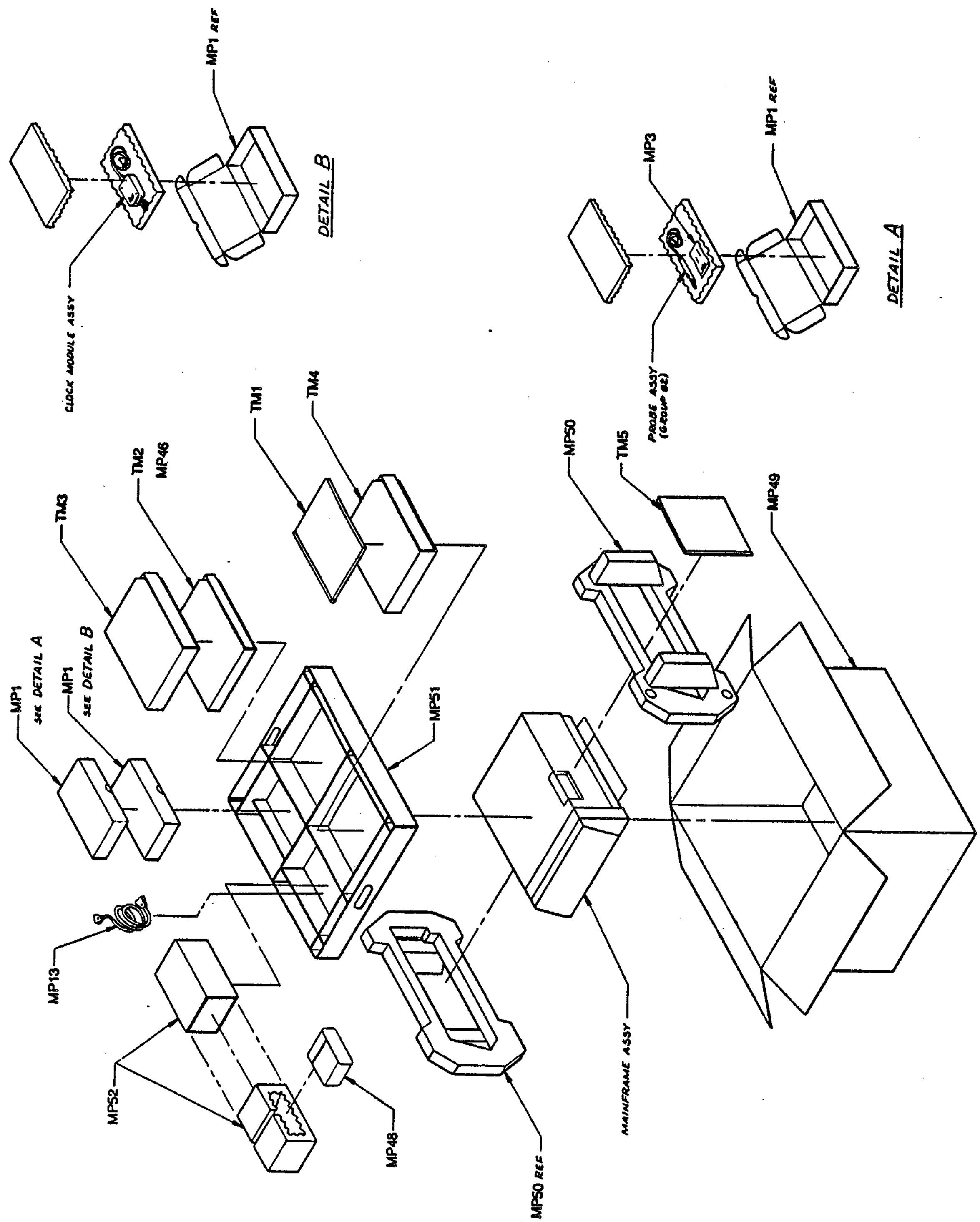


Figure 5-1. 9100 Series Final Assembly (cont.)



9100A T&B
(9 of 9)

Figure 5-1. 9100 Series Final Assembly (cont.)

Table 5-3. A1 Main PCA
(See Figure 5-2.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	--------------DESCRIPTION--------------	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C	1- 4, 6,		CAP,TA,10UF,+-20%,25V	772491	56289	195D106X0025Y2B	10		
C	23,100-103			772491					
C	5		CAP,TA,3.3UF,+-20%,25V	780486	56289	195D335X0025X2B	1	1	
C	10, 11, 18,		CAP,CER,0.01UF,+-10%,50V,X7R,1206	747261	72982	GRM426X7R103K50VPB	121		
C	19, 24,110-			747261					
C	113,120,121,			747261					
C	130,131,200-			747261					
C	288,300-310,			747261					
C	320,321,340-			747261					
C	343,360,361			747261					
C	12		CAP,CER,1000PF,+-10%,50V,COG,1206	747378	72982	GRM426COG102K50VPB	1		
C	13		CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	72982	GRM426X7R104K25VPB	1		
C	14		CAP,CER,10PF,+-10%,50V,COG,1206	747311	72982	GRM426COG100K50VPB	1		
C	16, 17, 20,		CAP,CER,47PF,+-10%,50V,COG,1206	747352	72982	GRM426COG470K50VPB	4		
C	21			747352					
C	380		CAP,CER,0.01UF,+-20%,100V,X7R,1206	742981	72982	GRM426X7R103M100VPB	1		
CR	1- 3, 6-		DIODE,SI,BV=200V,IO=10A,DUAL,SOT89	742973	25088	BAW79CE6327	6	1	
CR	8			742973					
CR	4, 5		DIODE,SI,BV=75.0V,IO=100MA,MLF	742064	73445	BAS32	2	2	
CR	9, 10		DIODE,SI,SCHOTTKY,30V,1.1A,SOT89	782573	61752	10JQ030TRRM	2	1	
F	1		FUSE, 5X20MM,FAST,0.125A,250V	573733	61935	216.125	1	5	
J	1		HEADER,1 ROW,0.100CTR,4 PIN	631184	00779	640456-4	1		
J	2, 3		HEADER,1 ROW,0.100CTR,8 PIN	520502	22526	65502-408	2		
J	4, 6		CONN,DIN41612,TYPE R,96 PIN	747808	00779	532523-1	2		
J	5		CONN,DIN41612,TYPE R,64 PIN	782094	00779	532523-2	1		
J	7, 8		HEADER,2 ROW,0.100 CTR,40 PIN	603670	00779	2-87227-0	2		
J	9		CONN,D-SUB,PWB,RT ANG,25 SCKT	782144	00779	747846-4	1		
J	10		CONN,CIRC,DIN,RT ANG,PWB,5 PIN @ 180	772178	00779	211450-1	1		
J	11		HEADER,2 ROW,0.100CTR,20 PIN	782185	00779	1-87227-0	1		
J	14		HEADER,2 ROW,0.100CTR,34 PIN	658047	00779	1-87227-7	1		
J	15		HEADER,1 ROW,0.156 CTR,10 PIN	446724	27264	09-65-1101	1		
L	1, 2		CHOKE	502138	89536	502138	2		
Q	1, 2	*	TRANSISTOR, SI, N-MOS, 1W, 4 PIN DIP	800391	17856	V11974	2	1	
R	1		RES,CHIP,CERM,56K,+-5%,0.125W,1206	746701	09969	CRCW1206563JB02	1		
R	2, 3, 6,		RES,CHIP,CERM,10K,+-5%,0.125W,1206	746610	09969	CRCW1206103JB02	42		
R	7, 11- 15,			746610					
R	27- 29, 31-			746610					
R	35, 40, 43,			746610					
R	45- 48, 56-			746610					
R	63, 67, 70,			746610					
R	75, 76, 80,			746610					
R	83- 85, 87,			746610					
R	89, 90			746610					
R	4,100-111,		RES,CHIP,CERM,10,+-5%,0.125W,1206	746214	09969	CRCW1206100JB02	14		
R	116			746214					
R	5, 8- 10,		RES,CHIP,CERM,4.7K,+-5%,0.125W,1206	740522	09969	CRCW1206472JB02	12		
R	21, 22, 30,			740522					
R	65, 69, 72,			740522					
R	82, 86			740522					
R	16, 17, 51-		RES,CHIP,CERM,1.2K,+-5%,0.125W,1206	746412	09969	CRCW1206122JB02	10		
R	55, 71, 78,			746412					
R	88			746412					
R	18, 19, 36,		RES,CHIP,CERM,39K,+-5%,0.125W,1206	746677	09969	CRCW1206393JB02	5		
R	37, 74			746677					
R	20, 38, 77		RES,CHIP,CERM,3K,+-5%,0.125W,1206	746511	09969	CRCW1206302JB02	3		
R	23, 24		RES,CHIP,CERM,390,+-5%,0.125W,1206	740498	09969	CRCW1206391JB02	2		
R	25, 26		RES,CHIP,CERM,220,+-5%,0.125W,1206	746347	09969	CRCW1206221JB02	2		
R	39, 44, 79		RES,CHIP,CERM,750,+-5%,0.125W,1206	746404	09969	CRCW1206751JB02	3		
R	41, 64, 66,		RES,CHIP,CERM,33,+-5%,0.125W,1206	746248	09969	CRCW1206330JB02	9		
R	68, 91,112-			746248					
R	115			746248					
R	42, 73		RES,CHIP,CERM,100K,+-5%,0.125W,1206	740548	09969	CRCW1206104JB02	2		
R	49, 50		RES,CHIP,CERM,510K,+-5%,0.125W,1206	746800	09969	CRCW1206514JB02	2		
R	81		RES,CHIP,CERM,2.2K,+-5%,0.125W,1206	746479	09969	CRCW1206222JB02	1		
S	1		SWITCH,PUSHBUTTON,SPST,MOMENTARY	782433	5N615	B3F-3122	1		
T	1		TRANSFORMER,CONVERTER	775932	89536	775932	1		
TP	1- 11		TERM,UNINSUL,WIRE FORM,TEST POINT	781237	27918	TP102-I	11		
U	1, 4	*	IC,BIPOLAR,DUAL RS-232 RECEIVER,SOIC	742395	01295	SN75152D	2	1	
U	2, 3	*	IC,BIPOLAR,DUAL RS-232 DRIVER,SOIC	742403	01295	SN75150DR	2	1	
U	5, 6	*	ISOLATOR,HI-SPEED DUAL	742841	28480	HCPL2531,OPTION100	2	1	

An * in 'S' column indicates a static-sensitive part.

Table 5-3. A1 Main PCA (cont.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
U	8, 35	*	IC,LSTTL,HEX INVERTER,SOIC	741017	18324	N74LS04DT	2	1	
U	9	*	IC,CMOS,OCTL LINE DRVR,SOIC	742593	18324	N74HCT244DT	1	1	
U	10	*	IC,LSTTL,8BIT P/S-IN,S-OUT SHFT,SOIC	741983	01295	SN74LS165ADR	1	1	
U	11	*	IC,NMOS,EEPROM 2444	834416	89536	834416	1	1	
U	13- 16	*	ASSEMBLY, RAM MODULE	809079	89536	809079	4		1
U	17	*	IC,ALSTTL,3-8 LINE DCDR W/ENABLE,SOIC	741686	01295	SN74ALS138DR	1	1	
U	18		OSCILLATOR,32MHZ,TTL CLOCK	742338	01537	K1100AM	1		
U	19	*	IC,FTTL,DUAL D F/F,+EDG TRG,SOIC	742163	18324	74F74DT	1	1	
U	20	*	IC,ASTTL,QUAD 2 INPUT NAND GATE,SOIC	782250	01295	SN74AS00DR	1	1	
U	21, 57	*	IC,ALSTTL,QUAD 2 INPUT AND GATE,SOIC	741827	01295	SN74ALS08DR	2	1	
U	22, 41, 82	*	IC,LSTTL,QUAD 2 INPUT OR GATE,SOIC	740878	18324	N74LS32D	3	1	
U	23, 24	*	IC,FTTL,9 BIT PARITY GEN/CHECKER,SOIC	742478	18324	N74F280ADT	2	1	
U	25, 91	*	IC,ALSTTL,QUAD 2 INPUT NAND GATE,SOIC	782268	01295	SN74ALS00ADR	2	1	
U	26	*	IC,LSTTL,8-BIT BINARY CNTR W/REG,SOIC	782243	01295	SN74LS590DR	1	1	
U	27	*	IC,LSTTL,OCTAL BUFFER INVERTED,SOIC	742627	18324	N74LS240DT	1	1	
U	28	*	IC, 16L8 LOGIC ARRAY	818203	7J696	AMPAL16L8LPC	1	1	
U	29- 31	*	IC,ASTTL,QUAD 2-INPUT MUX,SOIC	811984	01295	SN74AS257DR	3	1	
U	32	*	IC,NMOS,16 BIT MICROPROCESSOR,PLCC	742429	18324	SCN68000C8A68T	1	1	
U	33	*	IC,LSTTL,QUAD BUS,SOIC	740977	18324	N74LS125ADT	1	1	
U	34, 54	*	IC,LSTTL,DUAL 4 INPUT NAND GATE,SOIC	742528	18324	N74LS20DT	2	1	
U	36, 67, 74	*	IC,ALSTTL,QUAD 2 INPUT NOR GATE,SOIC	782284	01295	SN74ALS02DR	3	1	
U	37, 61- 63	*	IC,LSTTL,OCTAL D F/F,+EDG TRG,SOIC	741975	18324	N74LS374DT	4	1	
U	38, 89	*	IC,ALSTTL,HEX INVERTERS,SOIC	782300	01295	SN74ALSBDR	2	1	
U	39	*	IC,ALSTTL,QUAD 2 INPUT OR GATE,SOIC	742460	01295	SN74ALS32DR	1	1	
U	40, 50, 81	*	IC,LSTTL,8BIT S-IN,P-OUT R-SHFT,SOIC	742106	18324	NN74LS164DT	3	1	
U	42, 58	*	IC,LSTTL,OCTL LINE DRVR,SOIC	742122	18324	N74LS244DT	2	1	
U	43	*	IC,NMOS,FLOPPY DISK FORMTR CNTLR,PLCC	782870	53848	FDC179702LJP	1	1	
U	44	*	IC,NMOS,FLOPPY DISK INT CKT,PLCC	782888	53848	FDC9229B/TLJP	1	1	
U	46	*	PROGRAMMED 27256 V3.0	828897	89536	828897	1	1	
U	47	*	PROGRAMMED 27256 V3.0	828905	89536	828905	1	1	
U	49, 75	*	IC,LSTTL,8 TO 3 LINE ENCODER,SOIC	782326	01295	SN74LS148DR	2	1	
U	51, 64	*	IC,LSTTL,QUAD 2 INPUT NAND GATE,SOIC	741033	18324	N74LS00DT	2	1	
U	52	*	IC,LSTTL,TRIPLE 3-INPUT AND GATE,SOIC	741264	18324	N74LS10D	1	1	
U	53, 60	*	IC,LSTTL,OCTAL D F/F,+EDG TRG,SOIC	740928	18324	N74LS273DT	2	1	
U	55, 90	*	IC,ALSTTL,8 INPUT NAND GATE,SOIC	782334	01295	SN74ALSADR	2	1	
U	56, 65, 78	*	IC,LSTTL,QUAD 2 INPUT NOR GATE,SOIC	741025	18324	N74LS02DT	3	1	
U	59	*	IC,COMPARATOR,QUAD,14 PIN,SOIC	741561	18324	LM339DT	1	1	
U	66	*	IC,LSTTL,TRIPLE 3 INPUT NOR GATE,SOIC	740993	18324	N74LS27D	1	1	
U	68	*	IC,ALSTTL,DUAL 4 INPUT NAND GATE,SOIC	741645	01295	SN74ALS20ADR	1	1	
U	69	*	IC,ALSTTL,TRIPLE 3INPUT NOR GATE,SOIC	782318	01295	SN74ALS27DR	1	1	
U	70	*	IC,LSTTL,2-4 LINE DEMUX,SOIC	740951	18324	N74LS139D	1	1	
U	71	*	IC,CMOS,HEX INVERTER W/SCHT TRIG,SOIC	780965	18324	N74HCT14DT	1	1	
U	72	*	IC,TTL,HEX BUFFER W/OPEN COLL,SOIC	742387	18324	N7417DT	1	1	
U	73	*	IC,LSTTL,DUAL JK F/F,-EDG TRIG,SOIC	741256	18324	N74LS112DT	1	1	
U	76	*	IC,LSTTL,QUAD 2IN O/C NAND GATE,SOIC	782292	01295	SN74LS03DR	1	1	
U	77, 80	*	IC,LSTTL,DUAL D F/F,+EDG TRG,SOIC	740985	18324	S74LS74ADT	2	1	
U	79	*	IC,ALSTTL,DUAL D F/F,+EDG TRG,SOIC	742452	01295	SN74ALS74ADR	1	1	
U	83		SWITCH,MODULE,SPST,DIP,8 POS	414490	00779	435166-5	1		
U	84	*	IC,LSTTL,QUAD 2 INPUT AND GATE,SOIC	740860	18324	N74LS08DT	1	1	
U	85	*	IC,LSTTL,DUAL J-F F/F,+EDG TRIG,SOIC	742502	01295	SN74LS109ADT	1	1	
U	86	*	IC,LSTTL,DELAY ELEMENTS,SOIC	773077	01295	SN74LS31DR	1	1	
U	87	*	IC,VOLT SUPERVISOR,10V SENSE,SOIC	780502	01295	TL7705ACDR	1	1	
U	88	*	IC,LSTTL, MONOSTAB MULTIVB W/CLR,SOIC	742494	01295	SN74LS123DR	1	1	
XF	1		HOLDER,FUSE,5X20MM,PCB	772475	7E222	111501	2		
XU	13- 16		CONN,PWB EDGE,REC,0.100CTR,30 POS	806828	00779	821828-2	4	1	
XU	18		SPACER,DIP SOCKET,14 PIN,PLASTIC	441865	32559	814-060	1		
XU	28		SOCKET,IC,20 PIN	454421	09922	DILB20P-108	1		
XU	45- 48		SOCKET,IC,28 PIN	448217	91506	328-AG39D	4		
Y	1		CRYSTAL,3.6864MHZ,+/-50PPM,SURF.MNT.	800193	5W664	CP41A	1	1	

An * in 'S' column indicates a static-sensitive part.

NOTES:

1 - See A16 on the Final Assembly for quantities and part numbers.

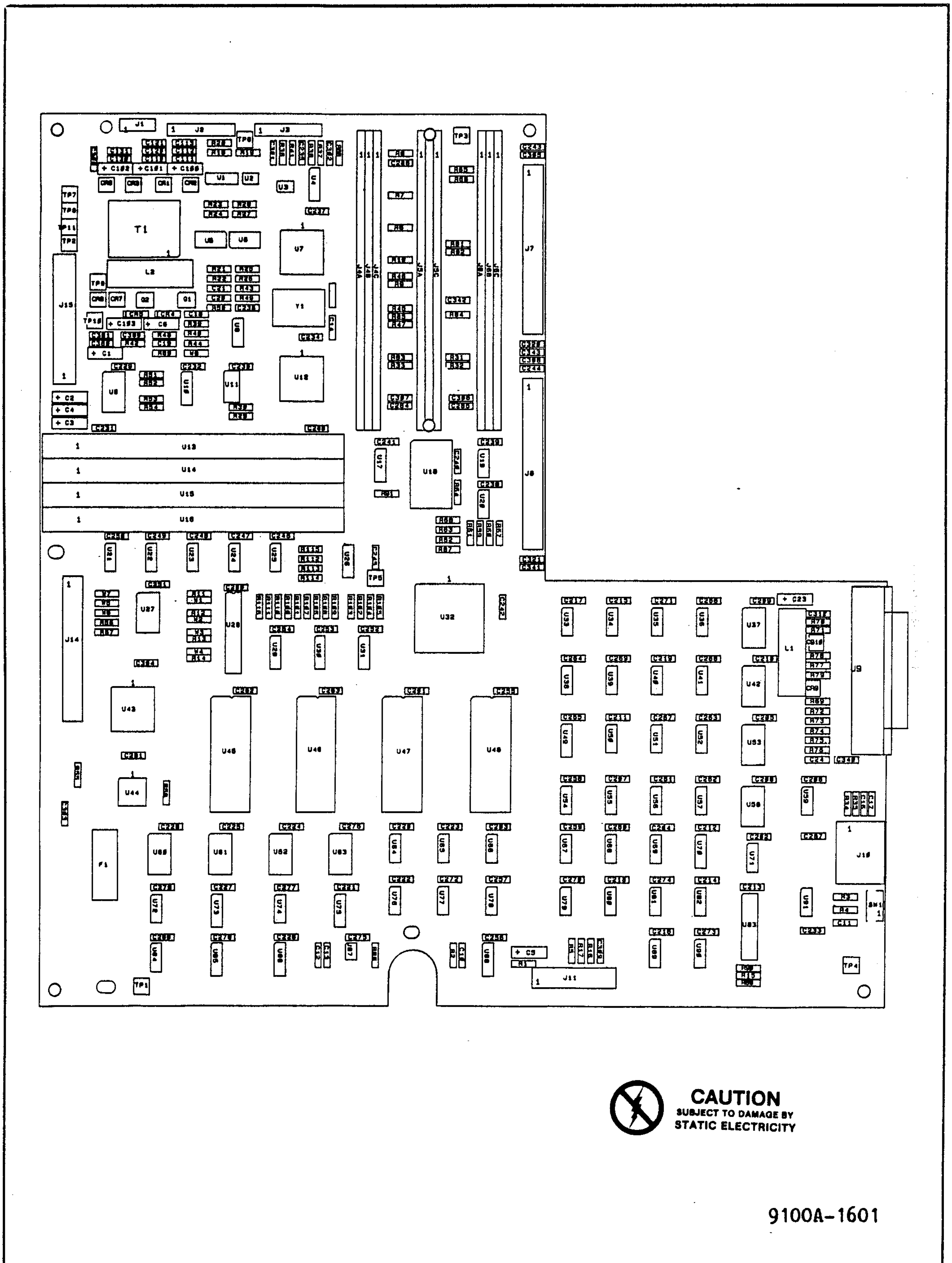
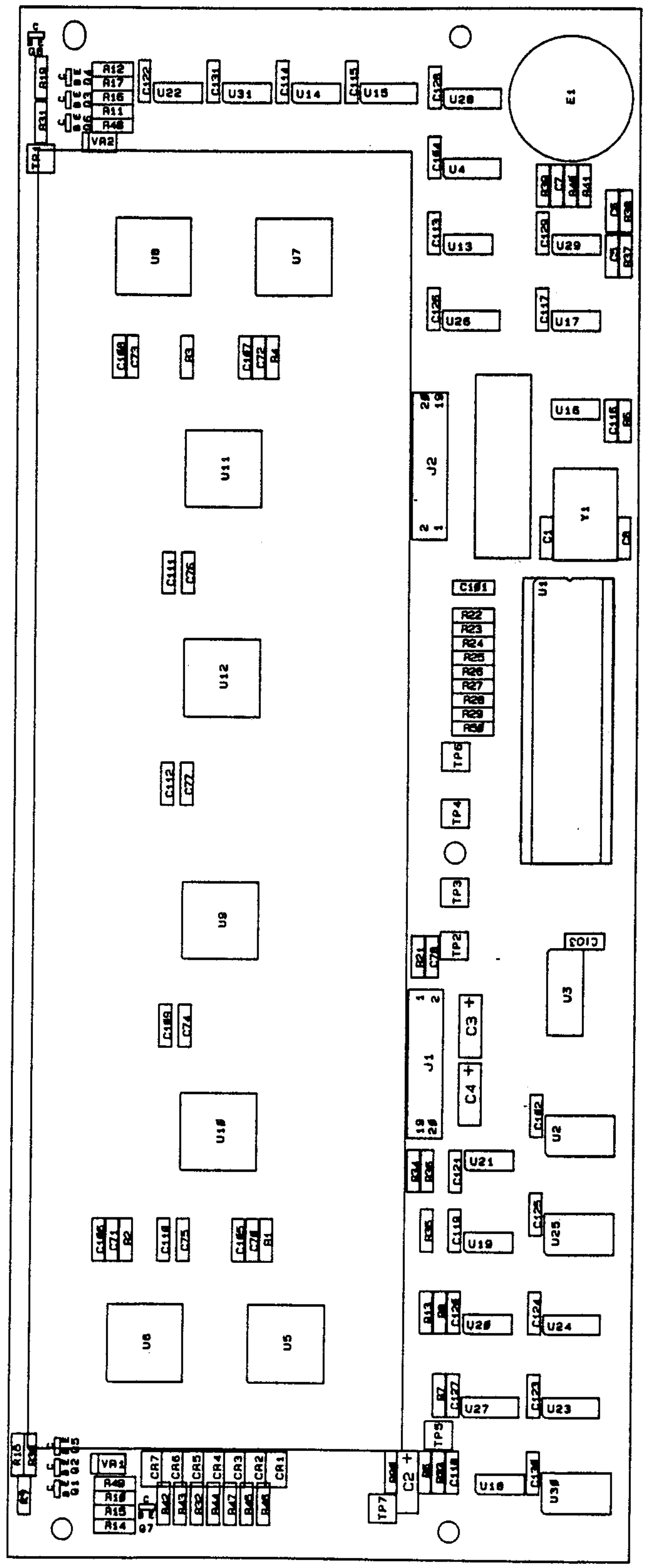


Figure 5-2. A1 Main PCA

Table 5-4. A2 Display Interface PCA
(See Figure 5-3.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	NOTE
C	1, 8		CAP,CER,5.6PF,+-10%,50V,COG,1206	782409	72982	GRM42-6COG5R6K50VPB	2		
C	2		CAP,TA,1.5UF,+-20%,50V	780478	56289	195D155X0050X2B	1	1	
C	3, 4		CAP,TA,10UF,+-20%,25V	772491	56289	195D106X0025X2B	2		
C	5, 70- 78,		CAP,CER,0.01UF,+-20%,100V,X7R,1206	742981	72982	GRM426X7R103M100VPB	41		
C	101-131			742981					
C	6, 7		CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	72982	GRM426X7R104K25VPB	2		
CR	1- 7	*	LED,RED,RECTANGLE,PCB MOUNT	504761	14936	MV57124	7	2	
E	1		AF TRANSD,PIEZO,24 MM	602490	51406	EFB-RD24C01	1		
J	1, 2		HEADER,2 ROW,0.100CTR,20 PIN	782185	00779	1087227-0	2		
MP	1		DISPLAY ALIGNMENT FIXTURE	788570	89536	788570	1		
Q	1- 4		TRANSISTOR,SI,PNP,SMALL SIGNAL,SOT23	742023	73445	BCX17TRL	4	1	
Q	5- 8		TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT23	742031	73445	BCX19TRL	4	1	
R	1- 4, 6-		RES,CHIP,CERM,1.1K,+-5%,0.125W,1206	746008	09969	CRCW1206112JB02	16		
R	13, 15, 16,			746008					
R	48, 49			746008					
R	5		RES,CHIP,CERM,100K,+-5%,0.125W,1206	740548	09969	CRCW1206104JB02	1		
R	14, 17		RES,CHIP,CERM,6.8K,+-5%,0.125W,1206	746024	09969	CRCW1206682JB02	2		
R	18, 19		RES,CHIP,CERM,620,+-5%,0.125W,1206	745984	09969	CRCW1206621JB02	2		
R	20		RES,CHIP,CERM,330,+-5%,0.125W,1206	746370	09969	CRCW1206331JB02	1		
R	21		RES,CHIP,CERM,470,+-5%,0.125W,1206	740506	09969	CRCW1206471JB02	1		
R	22- 29		RES,CHIP,CERM,10K,+-5%,0.125W,1206	746610	09969	CRCW1206103JB02	8		
R	30, 31		RES,CHIP,CERM,6.2K,+-5%,0.125W,1206	746016	09969	CRCW1206622JB02	2		
R	32, 42- 47		RES,CHIP,CERM,180,+-5%,0.125W,1206	746321	09969	CRCW1206181JB02	7		
R	33, 34, 41,		RES,CHIP,CERM,4.7K,+-5%,0.125W,1206	740522	09969	CRCW1206472JB02	4		
R	50			740522					
R	35, 36		RES,CHIP,CERM,100,+-5%,0.125W,1206	746297	09969	CRCW1206101JB02	2		
R	37		RES,CHIP,CERM,3K,+-5%,0.125W,1206	746511	09969	CRCW1206511JB02	1		
R	38		RES,CHIP,CERM,7.5K,+-5%,0.125W,1206	746586	09969	CRCW1206752JB02	1		
R	39		RES,CHIP,CERM,2K,+-5%,0.125W,1206	746461	09969	CRCW1206202JB02	1		
R	40		RES,CHIP,CERM,1.8K,+-5%,0.125W,1206	746453	09969	CRCW1206182JB02	1		
TP	1- 7		TERM, UNINSUL,WIRE FORM,TEST POINT	781237	26364	TP10201	7		
U	1	*	IC,NMOS,8 BIT MICROCOMP W/SOCKET	800607	56708	Z086132RSE	1	1	
U	1	*	PROGRAMMED 2732-2 V1.0	818187	89536	818187	1	1	
U	2	*	IC,LSTTL,OCTAL D F/F,+EDG TRG,SOIC	741975	18324	N74LS374DT	1	1	
U	3	*	IC,2K X 8 STATIC RAM,120NSEC,SOIC	742783	8V413	CXK5816M-12L	1	2	
U	4	*	IC,LSTTL,DUAL DIV BY 2, 5 CNTR,SOIC	741967	18324	N74LS390DT	1	1	
U	5- 12	*	IC,BIMOS,DISPLAY DRIVER,80V,PLCC	741231	56289	UCN5818EP-1	8	2	
U	13, 14	*	IC,LSTTL,DUAL D F/F,+EDG TRG,SOIC	740985	18324	S74LS74ADT	2	1	
U	15, 27	*	IC,ALSTTL,DUAL JK F/F,-EDG TRG,SOIC	807578	12040	DM74ALS112AM	2	1	
U	16	*	IC,LSTTL,QUAD 2 INPUT NAND GATE,SOIC	741033	18324	N74LS00DT	1	1	
U	17, 31	*	IC,LSTTL,QUAD 2 INPUT NOR GATE,SOIC	741025	18324	N74LS02DT	2	1	
U	18	*	IC,CMOS,HEX INVERTER,SOIC	742585	18324	N74HCT040	1	1	
U	19, 20	*	IC,LSTTL,TRIPLE 3-INPUT AND GATE,SOIC	741264	18324	N74LS10D	2	1	
U	21	*	IC,LSTTL,QUAD 2 INPUT OR GATE,SOIC	740878	18324	N74LS32D	1	1	
U	22	*	IC,TTL,HEX INVERTER,W/OPEN COLL,SOIC	741249	18324	N7406DT	1	1	
U	23, 24	*	IC,CMOS,8 BIT P/S-IN,S-OUT SHFT,SOIC	782904	18324	74HCT165DT	2	1	
U	25, 30	*	IC,ALSTTL,OCTL D F/F,+EDG TRG,SOIC	741769	01295	SN74ALS273DWR	2	1	
U	26	*	IC,LSTTL,BCD-DEC,DECODER/DRIVER,SOIC	742007	01295	SN74LS145DR	1	1	
U	28	*	IC,LSTTL,DIV BY 16 BINARY COUNTR,SOIC	741991	18324	N74LS163ADT	1	1	
U	29	*	IC,BPLR,DUAL TIMER,SOIC	741959	18324	NE556DT	1	1	
VF	1		TUBE,DISPLAY,VAC FLUOR,PATTERN DIS	742056	0BW21	DM256X26G	1		
VR	1- 2		ZENER,UNCOMP,3.3V,5%,76MA,1W,MLF	800599	01537	MLL4728AT1	2	1	
XU	1		SOCKET,IC,40 PIN	429282	09922	DILB40P-108	1		
Y	1		CRYSTAL,9.8304MHZ,+-50PPM,SURFACE MT.	800383	5W664	CP41A	1		

An * in 'S' column indicates a static-sensitive part.



9100A-1602

Figure 5-3. A2 Display Interface PCA

Table 5-5. A4 Video Controller PCA
(See Figure 5-4.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C	1,101-131		CAP,CER,0.01UF,+-10%,50V,X7R,1206	747261	72982	GRM42-6X7R103K50VPB	32		
C	2, 8		CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	72982	GRM42-6X7R104K25VPB	2		
C	3, 7		CAP,TA,10UF,+-20%,25V	772491	56289	195D-106X0025Y2B	2	1	
C	4- 6		CAP,CER,33PF,+-10%,50V,COG,1206	769240	72982	GRM42-6COG330K50VPB	3		
C	9, 10		CAP,CER,120PF,+-10%,50V,COG,1206	740589	72982	GRM42-6COG121K50VPB	2		
H	1		SCREW,THD CUT,PHP,S.STL,4-24X3/8	183574	COMMERCIAL		2		
J	1		CONN,DIN41612,TYPE R,RT ANG,64 SCKT	782102	00779	531796-2	1		
J	2		CONN,D-SUB,PWB,RT ANG,9 SCKT	782789	00779	205866-1	1		
Q	1		TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT23	742676	01537	MMBT3904T1	1	1	
Q	2		TRANSISTOR,SI,PNP,SMALL SIGNAL,SOT23	742684	01537	MMBT3906T1	1	1	
R	1- 5, 14,		RES,CHIP,CERM,330,+-5%,0.125W,1206	746370	09969	CRCW1206331JB02	7		
R	15			746370					
R	6, 13		RES,CHIP,CERM,510,+-5%,0.125W,1206	746388	09969	CRCW1206511JB02	2		
R	7- 11		RES,CHIP,CERM,158,+-1%,0.125W,1206	769828	09969	CRCW12061580FB02	5		
R	12		RES,CHIP,CERM,1K,+-5%,0.125W,1206	745992	09969	CRCW1206102JB02	1		
R	16		RES,CHIP,CERM,470,+-5%,0.125W,1206	740506	09969	CRCW1206471JB02	1		
R	17		RES,CHIP,CERM,47,+-5%,0.125W,1206	746263	09969	CRCW1206470JB02	1		
R	18		RES,CHIP,CERM,220,+-5%,0.125W,1206	746347	09969	CRCW1206221JB02	1		
R	19		RES,CHIP,CERM,2.4K,+-5%,0.125W,1206	746495	09969	CRCW1206242JB02	1		
R	20		RES,CHIP,CERM,1.6K,+-5%,0.125W,1206	746446	09969	CRCW1206162JB02	1		
R	21		RES,CHIP,CERM,5.1K,+-5%,0.125W,1206	746560	09969	CRCW1206512JB02	1		
R	22, 23		RES,CHIP,CERM,22,+-5%,0.125W,1206	746230	09969	CRCW1206220JB02	2		
R	24, 25		RES,CHIP,CERM,10K,+-5%,0.125W,1206	746610	09969	CRCW1206103JB02	2		
TP	1- 10		TERM,UNINSUL,WIRE FORM,TEST POINT	781237	23634	TP10201	10		
U	1	*	IC,NMOS,ADV VIDEO DISPLAY CNTRLR,PLCC	742734	18324	SCN2674BC4A44T	1	1	
U	2	*	IC,BIPOLAR,CLR/MONO ATTRI CNTRLR,PLCC	742742	18324	SCB2675BC5A44T	1	1	
U	3, 4	*	IC,2K X 8 STATIC RAM,120NSEC,SOIC	742783	8V413	CXK5816M-12L	2	1	
U	5	*	PROGRAMMED 27128-150 V1.0	818195	89536	818195	1	1	
U	6- 8	*	IC,FTTL,QUAD 2-1 LINE MUX,SOIC	773028	18324	74F157ADT	3	1	
U	9, 10	*	IC,LSTTL,OCTL LINE DRVR,SOIC	742122	18324	N74LS244DT	2	1	
U	11, 12	*	IC,LSTTL,OCTL D TRNSPRNT LATCHES,SOIC	742726	18324	N74LS373DT	2	1	
U	13	*	IC,LSTTL,OCTAL D F/F,+EDG TRG,SOIC	741975	18324	N74LS374DT	1	1	
U	14	*	IC,LSTTL,QUAD D F/F,+EDG TRG,SOIC	742619	18324	N74LS175DT	1	1	
U	15	*	IC,STTL,QUAD D F/F,+EDG TRG,SOIC	742700	18324	N74S175DT	1	1	
U	16- 19	*	IC,LSTTL,QUAD 2 INPUT NAND GATE,SOIC	741033	18324	N74LS00DT	4	1	
U	20, 21	*	IC,LSTTL,TRIPLE 3-INPUT AND GATE,SOIC	741264	18324	N74LS10D	2	1	
U	22	*	IC,LSTTL,HEX INVERTER,SOIC	741017	18324	N74LS04DT	1	1	
U	23	*	IC,LSTTL,SINGLE 8-INP. NAND GATE,SOIC	742510	18324	N74LS30D	1	1	
U	24	*	IC,ALSTTL,DUAL JK F/F,-EDG TRG,SOIC	807578	12040	DM74ALS112AM	1	1	
U	25	*	IC,STTL,QUAD 2 INPUT +OR GATE,SOIC	742692	18324	74S86D	1	1	
U	26	*	IC,LSTTL,QUAD 2 INPUT AND GATE,SOIC	740860	18324	N74LS08DT	1	1	
U	27	*	IC,LSTTL,OCTAL BUFFER INVERTED,SOIC	742627	18324	N74LS240DT	1	1	
U	28	*	ISOLATOR,OPTO,DUAL,DTL/TTL COMPATABLE	418285	28480	HCPL-2630	1	1	
U	29- 31	*	ISOLATOR, 20 MHZ OPTOCOUPLER	742817	28480	HCPL-2400	3	1	
XU	5		SOCKET,IC,28 PIN	448217	91506	328-AG39D	1		
XY	1		SPACER,DIP SOCKET,14 PIN,PLASTIC	441865	32559	814-060	1		
XZ	1, 2		SOCKET,IC,16 PIN	276535	91506	316-AG39D	2		
Y	1		OSCILLATOR,31.9399 MHZ,TTL CLOCK	800029	01537	K1100AM	1		

An * in 'S' column indicates a static-sensitive part.

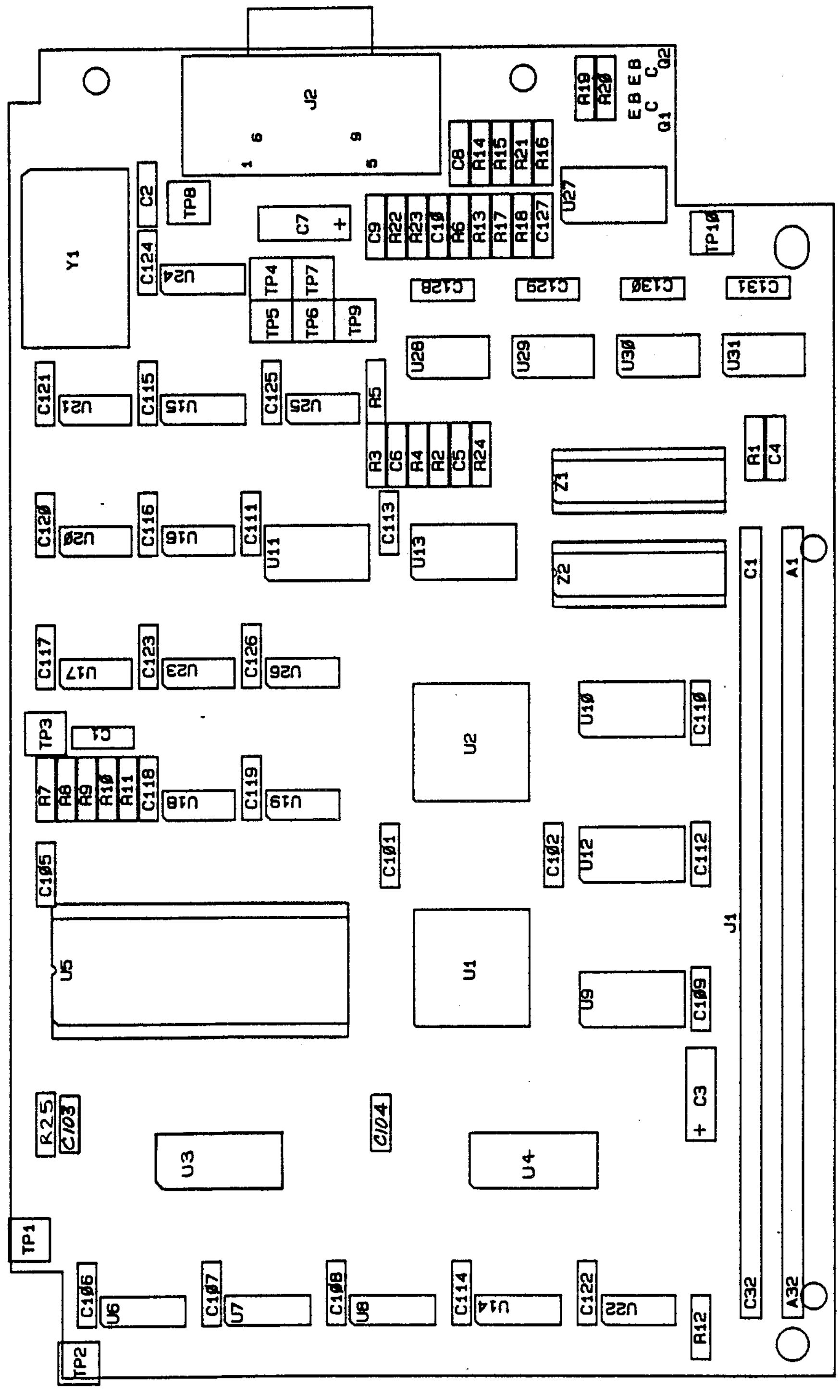


Figure 5-4. A4 Video Controller PCA

Table 5-6. A5 Probe Assembly
(See Figure 5-5.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C	1		CAP,CER,27PF,+-10%,50V,COG,1206	800508	72982	GRM426COG270K50VPB	1		
C	2, 5		CAP,CER,1000PF,+-10%,50V,COG,1206	747378	72982	GRM426COG102K50VPB	2		
C	3, 4		CAP,CER,0.22UF,+80-20%,50V,Y5V,1206	740597	72982	GRM426Y5V224250VPB	2		
C	6		CAP,CER,0.22UF,+80-20%,50V,Y5V,1206	740597	72982	GRM426Y5V224250VPB	1		
CR	1- 4		DIODE,SI,BV=75.0V,IO=100MA,MLF	742064	73445	BAS32	4	1	
CR	5		DIODE,SI,BV=75.0V,IO=100MA,MLF	742064	73445	BAS32	1	1	
L	1- 3		LAMP,SUB-MIN,5V,20MA	836239	S3774	0L-3043AS15	3	5	
MP	1		CONNECTOR,GROUND CLIP,FINISHED	788026	89536	788026	1	1	
MP	2		COVER,PROBE	773309	89536	773309	1		
MP	3		KEYTOP	773333	89536	773333	1		
MP	4		BODY,PROBE	773317	89536	773317	1		
MP	5		DECAL,PROBE CONNECTOR	773929	89536	773929	1		
Q	1, 2		TRANSISTOR,SI,PNP,SMALL SIGNAL,SOT23	742023	73445	BCX17TRL	2	1	
Q	3, 4		TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT23	742031	73445	BCX19TRL	2	1	
R	1		RES,CHIP,CERM,220,+-5%,0.125W,1206	746347	09969	CRCW1206221JB02	1		
R	2		RES,CHIP,CERM,100K,+-1%,0.125W,1206	769802	09969	CRCW12061003FB02	1	1	
R	3, 8, 10		RES,CHIP,CERM,200,+-5%,0.125W,1206	746339	09969	CRCW1206201JB02	3		
R	4		RES,CHIP,CERM,330,+-5%,0.125W,1206	746370	09969	CRCW1206331JB02	1		
R	5, 7		RES,CHIP,CERM,470,+-5%,0.125W,1206	740506	09969	CRCW1206471JB02	2		
R	6		RES,CHIP,CERM,470,+-5%,0.125W,1206	740506	09969	CRCW1206471JB02	1		
R	9		RES,CHIP,CERM,205K,+-1%,0.125W,1206	769836	09969	CRCW12062053FB02	1	1	
R	11- 13		RES,CHIP,CERM,1K,+-5%,0.125W,1206	745992	09969	CRCW1206102JB02	3		
S	1		SWITCH,PUSHBUTTON,SPST,MOMENTARY	782656	5N615	B3F-1022	1	3	
U	1	*	IC,FTTL,HEX INVERT W/SCHMT TRIG,SOIC	742825	18324	N74F14D	1	1	
W	1		WIRE,TEF,E,28AWG,STRN,BLU	558320	89536	558320	1		
W	2		CABLE ASSY, PROBE	783951	89536	783951	1		

An * in 'S' column indicates a static-sensitive part.

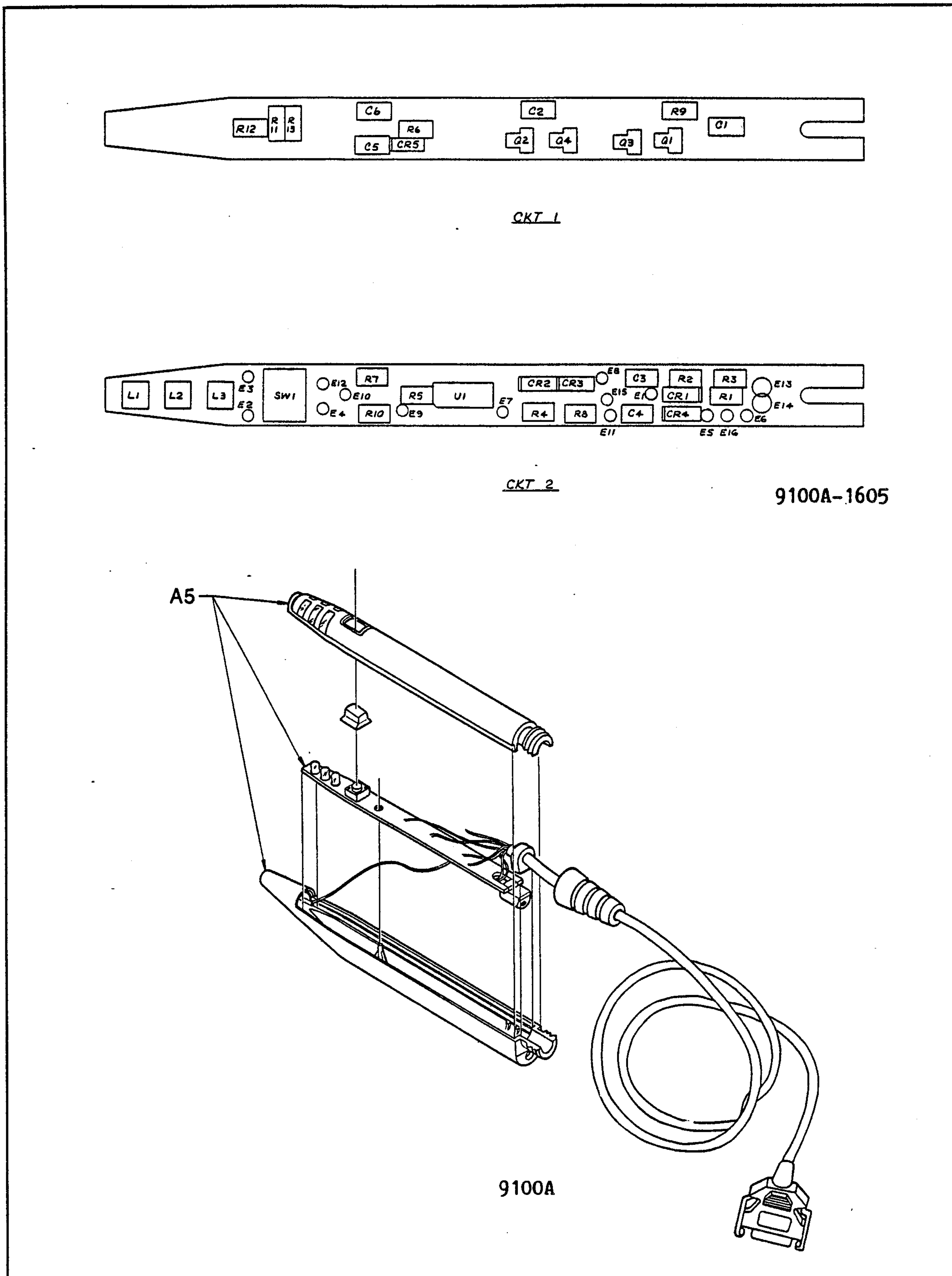


Figure 5-5. A5 Probe PCA

Table 5-7. A6 Clock Module PCA
(See Figure 5-6.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	----DESCRIPTION----	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C 1- 4		CAP,CER,8.2PF,+-10%,50V,COG,1206	747303	72982	GRM426COG8R2K50VPB	4		
C 5- 12, 14		CAP,CER,0.01UF,+-10%,50V,X7R,1206	747261	72982	GRM426X7R103K50VPB	9		
C 13		CAP,TA,10UF,+-20%,25V	772491	56289	195D106X0025Y2B	1		
CR 1- 4		DIODE,SI,BV=70.0V,IO=50MA,DUAL,SOT23	742320	73445	BAV99	4		
F 1		FUSE,1/4X1-1/4,FAST,0.25A,250V	109314	71400	AGC1-4	1	5	
F 1		FUSE,5X20MM,FAST,0.25A,250V	543504	71400	GMA1-4	1	5	
J 1- 5		PIN,SINGLE,PWB,0.058 DIA	233411	00779	60599-3	5		
J 6		HEADER,2 ROW,0.100CTR,RT ANG,16 PIN	417030	00779	87230-8	1		
MP 1		FUSE CAP, 1/4 X 1-1/4	460238	61935	031.1666	1		
MP 1		FUSE CAP, 5 X 20 MM	461020	61935	031.1663	1		
R 1- 8		RES,CHIP,CERM,22K,+-5%,0.125W,1206	746651	09969	CRCW1206273JB02	8		
R 9- 12		RES,CHIP,CERM,11K,+-5%,0.125W,1206	769752	09969	CRCW1206113JB02	4		
R 13, 24- 27		RES,CHIP,CERM,100,+-5%,0.125W,1206	746297	09969	CRCW1206101JB02	5	1	
R 14		RES,CHIP,CERM,16K,+-5%,0.125W,1206	769745	09969	CRCW1206163JB02	1		
R 15- 22		RES,CHIP,CERM,330,+-5%,0.125W,1206	746370	09969	CRCW1206331JB02	8		
R 23		RES,CHIP,CERM,10K,+-5%,0.125W,1206	746610	09969	CRCW1206103JB02	1		
U 1, 2	*	IC,COMPRTR,DUAL,HI-SPEED,16 PIN DIP	782219	7J696	AM687ADL	2	1	
XF 1		HLDR PART,FUSE,BODY,PWB MT	602763	61935	FAU031.3573	1		
XU 1, 2		SOCKET,IC,16 PIN	276535	91506	316-AG39D	2		

An * in 'S' column indicates a static-sensitive part.

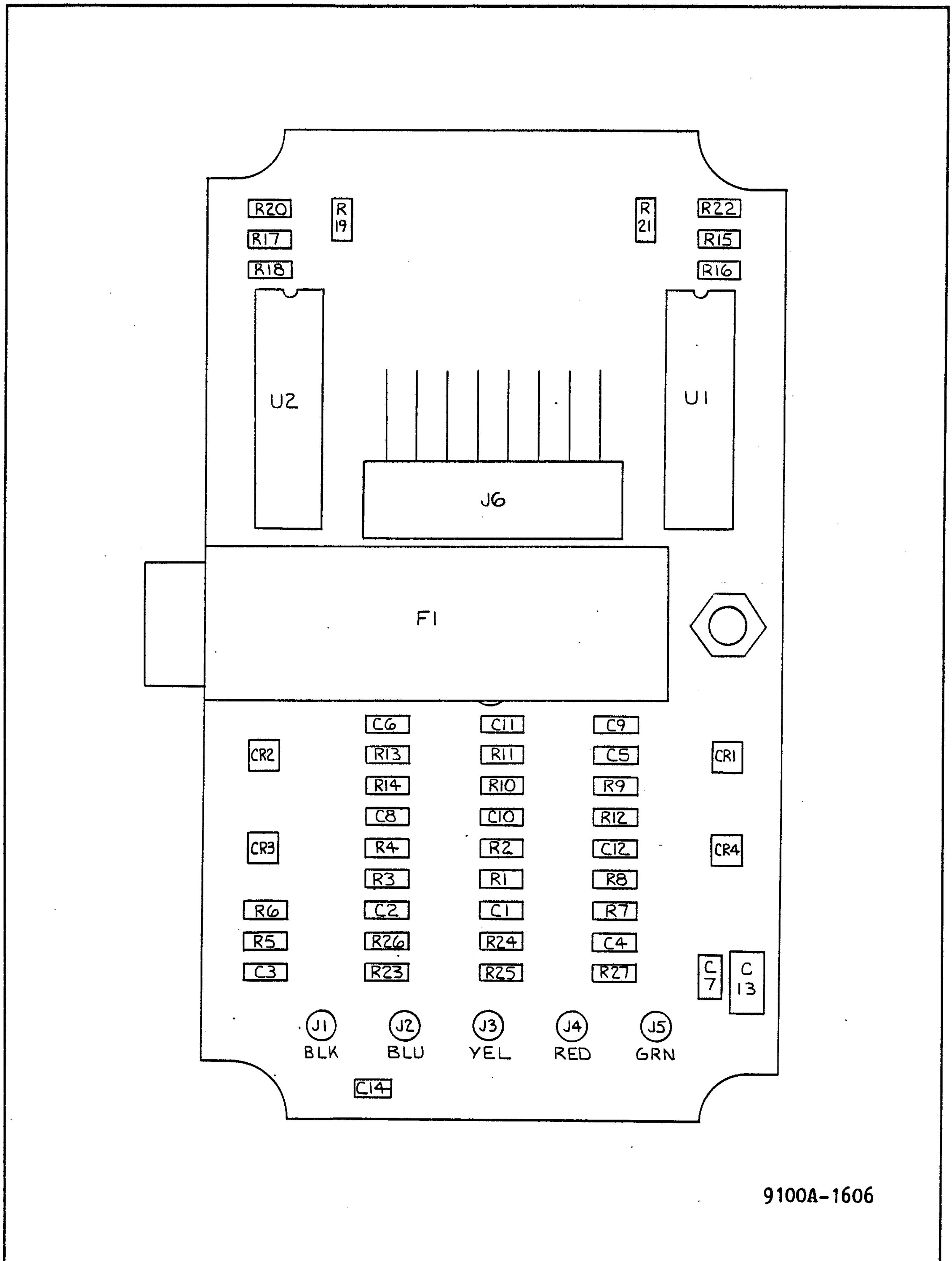


Figure 5-6. A6 Clock Module PCA

Table 5-8. A7 I/O Module Main PCA
(See Figure 5-7.)

REFERENCE DESIGNATOR -A>-	-NUMERICS---->	S	---------------DESCRIPTION---------------	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C	1, 2, 9-		CAP,TA,10UF,+-20%,25V	772491	56289	195D106X0025Y2B	27		
C	24, 27, 37,			772491					
C	42- 44, 61,			772491					
C	62, 67, 68			772491					
C	3- 7, 28-		CAP,CER,0.01UF,+-10%,50V,X7R,1206	747261	72982	GRM426X7R103K50VPB	31		
C	36, 38, 39,			747261					
C	46- 60			747261					
C	45		CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	72982	GRM426X7R104K25VPB	1		
CR	1- 4, 7,		DIODE,SI,BV=70.0V,IO=50MA,DUAL,SOT23	742320	73445	BAV99	85	5	
CR	100-179			742320					
CR	5, 6		DIODE,SI,BV=75.0V,IO=100MA,MLF	742064	73445	BAS32	2	1	
CR	8		DIODE,SI,SCHOTTKY,30V,1.1A,SOT89	782573	61752	10JQ030TRRM	1	1	
E	1- 5		PIN,SINGLE,PWB,0.058 DIA	233411	00779	60599-3	5		
F	1		FUSE,1/4 X 1-1/4,SLOW,1.0A,250V	109272	75915	313/1.25	1	5	
F	1		FUSE,5X20MM,SLOW,1A,250V	808055	61935	034.3117	1	5	
H	1		SCREW,MACH,PHP SEMS,STL,6-32X1/4	178533	COMMERCIAL		1		
J	1		HEADER,2 ROW,0.100CTR,RT ANG,38 PIN	782748	00779	1-87320-9	1		
J	2, 3		SOCKET,2 ROW,PWB,0.100CTR,30 POS	783795	00779	1-86418-0	2		
MP	1		SPACER,HEX,ALUM,6-32X0.625	104448	89536	104448	1		
P	1		HEADER,1 ROW,0.150CTR,RT ANG,6 PIN	783803	22526	65598-106	1		
Q	1, 2		TRANSISTOR,SI,PNP,SMALL SIGNAL,SOT23	742684	01537	MMBT3906T1	2	1	
R	1, 2		RES,CHIP,CERM,100,+-5%,0.125W,1206	746297	51406	RX39110G101JBA	2		
R	3, 5, 6,		RES,CHIP,CERM,10K,+-1%,0.125W,1206	769794	09969	CRCW12061002FB02	4		
R	10			769794					
R	4, 9		RES,CHIP,CERM,42.2K,+-1%,0.125W,1206	769851	09969	CRCW12064222FB02	2		
R	7		RES,CHIP,CERM,7.5K,+-1%,0.125W,1206	811463	09969	CRCW12067501FB02	1		
R	8		RES,CHIP,CERM,825,+-1%,0.125W,1206	811455	09969	CRCW12068250FB02	1		
R	13, 14		RES,CHIP,CERM,9.1K,+-5%,0.125W,1206	746602	09969	CRCW1206912JB02	2		
R	15, 17		RES,CHIP,CERM,43K,+-5%,0.125W,1206	769299	09969	CRCW1206433JB02	2		
R	16, 18		RES,CHIP,CERM,910,+-5%,0.125W,1206	769257	09969	CRCW1206911JB02	2		
R	19, 20, 23-		RES,CHIP,CERM,4.7K,+-5%,0.125W,1206	740522	09969	CRCW1206472JB02	10		
R	30			740522					
R	21, 22, 31,		RES,CHIP,CERM,1K,+-5%,0.125W,1206	745992	09969	CRCW1206102JB02	7		
R	33, 34, 39,			745992					
R	40			745992					
R	32		RES,CHIP,CERM,11K,+-5%,0.125W,1206	769752	09969	CRCW1206113JB02	1		
TP	1- 8		TERM,UNINSUL,WIRE FORM,TEST POINT	781237	26364	TP10201	8		
U	1		OSCILLATOR,1 MHZ,TTL CLOCK	634113	01537	RASCO-3	1		
U	2	*	IC,OP AMP,QUAD,LOW POWER,SOIC	742569	18324	LM324D	1	1	
U	3, 5	*	IC,LSTTL,QUAD 2 INPUT AND GATE,SOIC	740860	18324	N74LS08DT	2	1	
U	4	*	IC,CMOS,HEX INVERTER,SOIC	742585	18324	N74HCT040	1	1	
U	6	*	IC,LSTTL,3-8 LINE DCDR W/ENABLE,SOIC	740969	18324	N74LS138DT	1	1	
U	7	*	IC,LSTTL,OCTL D TRNSPRNT LATCHES,SOIC	742726	18324	N74LS373DT	1	1	
U	8	*	IC,CMOS,OCTAL BUS TRANSCEIVER,SOIC	742577	18324	N74HCT245DT	1	1	
U	9	*	IC,ECL,QUAD ECL-TTL TRANSLATOR	801274	04713	MC10H125P	1	1	
U	10	*	IC,LSTTL,QUAD 2 INPUT OR GATE,SOIC	740878	18324	N74LS32D	1	1	
U	11, 12	*	IC,LSTTL,DUAL JK F/F,-EDG TRIG,SOIC	741256	18324	N74LS112DT	2	1	
U	13, 16, 17	*	IC,CMOS,OCTL LINE DRVR,SOIC	742593	18324	N74HCT244DT	3	2	
U	14	*	IC,LSTTL,OCTAL D F/F,+EDG TRG,SOIC	740928	18324	N74LS273DT	1	1	
U	15	*	IC,LSTTL,SINGLE 8-INP. NAND GATE,SOIC	742510	18324	N74LS30D	1	1	
U	18	*	IC,CMOS,DUAL 4-1 SELECT/MUX,SOIC	780767	18324	74HCT153DT	1	1	
U	100,110,120,	*	IC CMOS QUEST 9000 CHIP CERAMIC TEST	760785	89536	760785	5	1	
U	130,140	*		760785					
U	101,103,111,	*	TRANSISTOR,SI,P-DMOS,POWER FET,14 PIN	800185	59640	VP0204N6	10	2	
U	113,121,123,	*		800185					
U	131,133,141,	*		800185					
U	143	*		800185					
U	102,104,112,	*	TRANS,SI,N-DMOS PWR FET,QUAD	782557	59640	VN0104N6	10	2	
U	114,122,124,	*		782557					
U	132,134,142,	*		782557					
U	144	*		782557					
U	105,106,115,	*	IC,CMOS,OCTL LINE DRVR,SOIC	801043	18324	74HCT2440T	10	1	
U	116,125,126,	*		801043					
U	135,136,145,	*		801043					
U	146	*		801043					
XF	1		HLDR PART,FUSE,BODY,PWB MT	602763	61935	FAU031.3573	1		
XY	1		SPACER,DIP SOCKET,14 PIN,PLASTIC	441865	32559	814-060	1		
Z	1,100,110,		RES,NET,DIP,16PIN,8RES,100,+-5%	780460	09969	MDP1603101J	6	1	
Z	120,130,140			780460					

An * in 'S' column indicates a static-sensitive part.

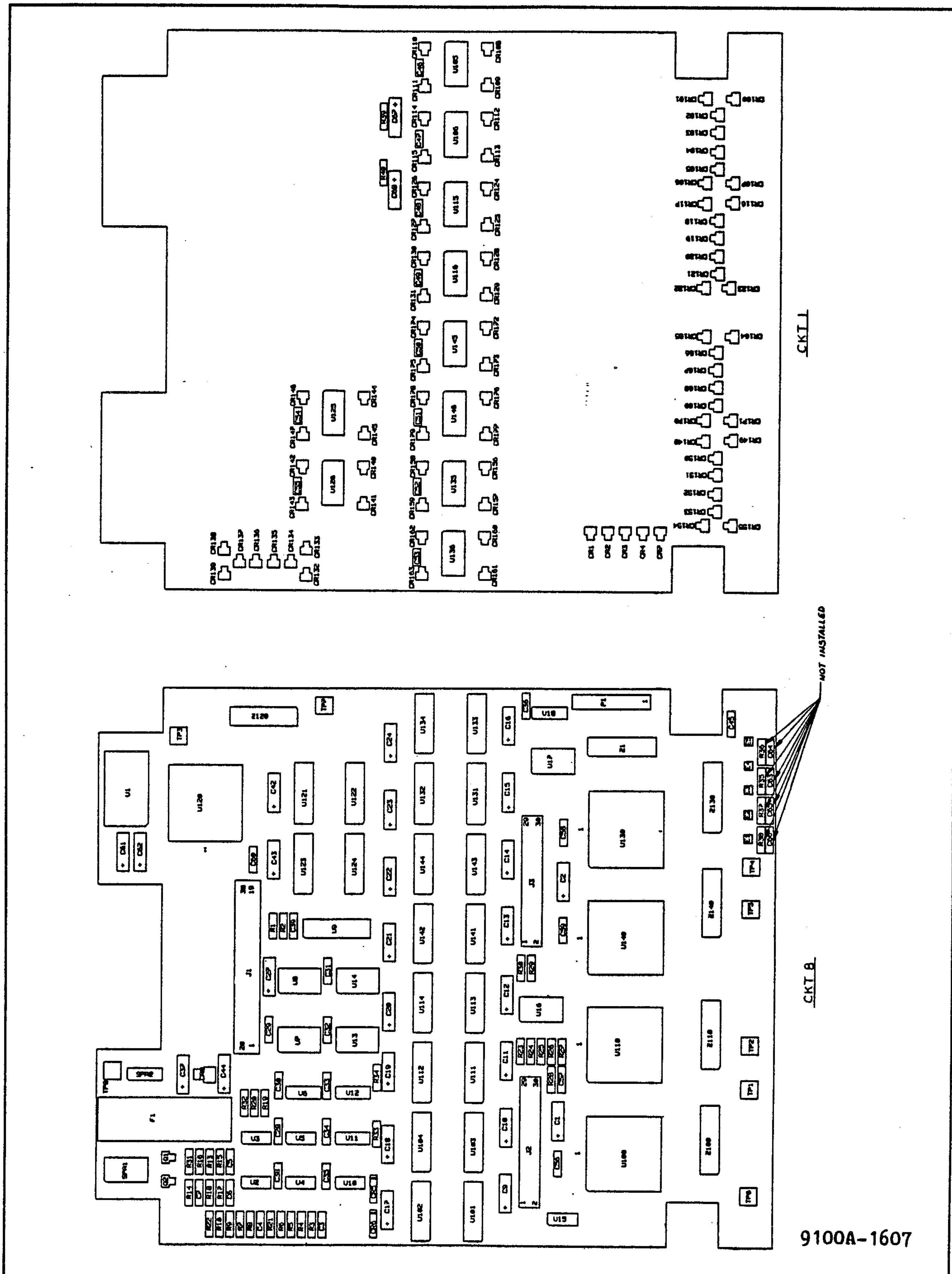


Figure 5-7. A7 I/O Module (Main) PCA

Table 5-9. A8 I/O Module (Top) PCA
(See Figure 5-8.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C	1- 4		CAP,AL,4700UF,+-20%,16V,SOLV PROOF	800904	62643	SME16T472M18X40LL	4	1	
CR	1- 4	*	DIODE,SI,100 PIV,1.0 AMP	343491	01295	1N4002	4	1	
H	1		SCREW,MACH,PHP SEMS,STL,6-32X1/4	178533	COMMERCIAL		2		
H	2		SCREW,MACH,PHP SEMS,STL,4-40X3/16	732750	COMMERCIAL		4		
J	1, 4		HEADER,2 ROW,0.100CTR,30 PIN	801233	22526	68464-630	2		
J	2, 3		CONN,RECT,PWB,REC,33 POS	800672	50541	KA33/127BPF021TAHF6	2		
MP	1		COVER, SHIELD I/O MODULE	768036	89536	768036	1		
MP	2		SPACER,SWAGED,RND,BRASS,6-32X0.590	811224	9W423	9538B-B-0632	5		
MP	3		SPACER,SWAGED,RND,BRASS,6-32X0.250	446351	9W423	9533B-B-0440	2		
P	1- 4		GUIDE SOCKET	805648	89536	805648	4		

An * in 'S' column indicates a static-sensitive part.

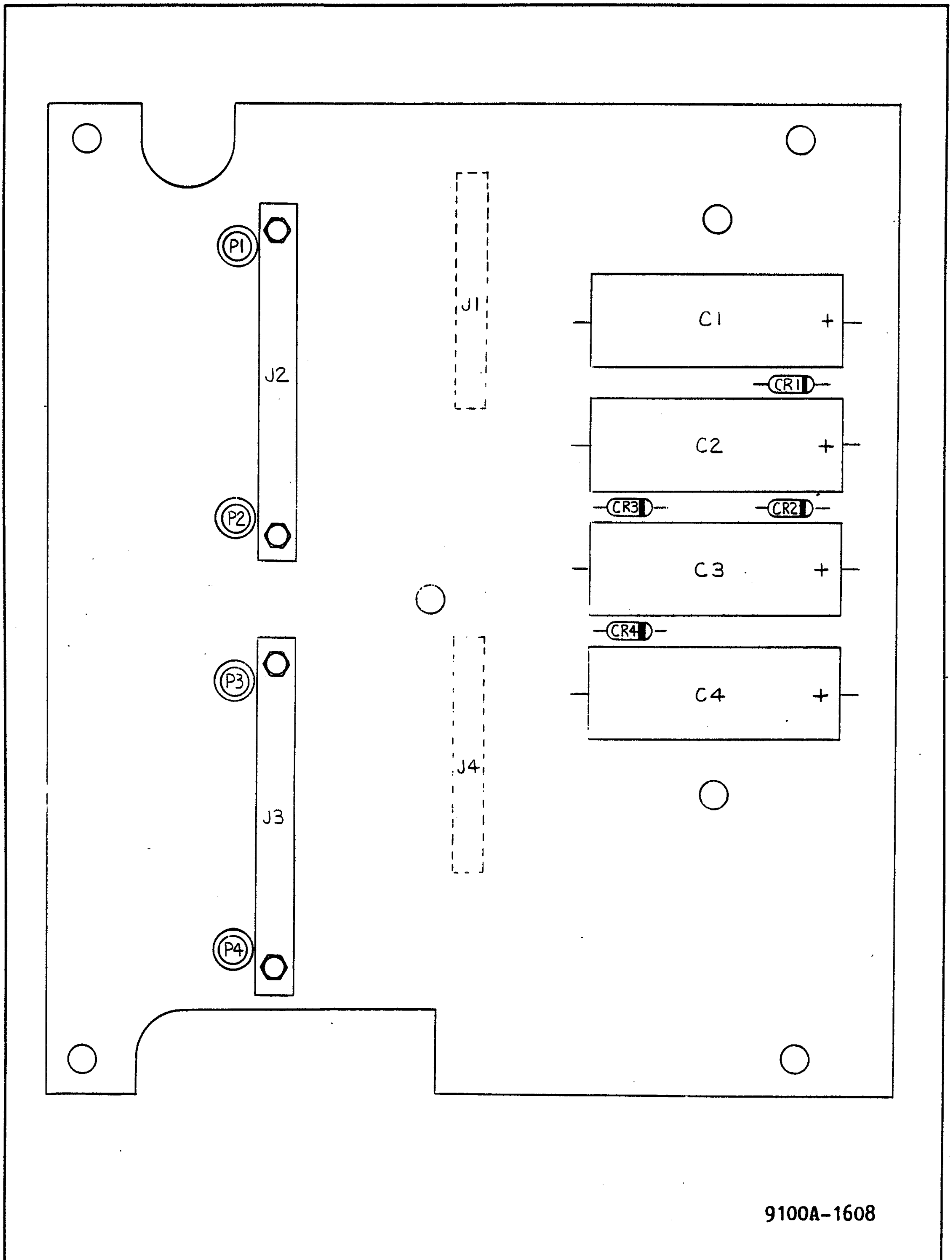


Figure 5-8. A8 I/O Module (Top) PCA

Table 5-10. A9 Probe I/O Interface PCA
(See Figure 5-9.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	---------------DESCRIPTION---------------	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C	1, 3, 4,		CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	72982	GRM42-6X7R104K25VPB	23		
C	8- 11, 16,			747287					
C	17, 19, 21,			747287					
C	23, 25- 33,			747287					
C	39, 40			747287					
C	2		CAP,VAR,6-50PF,50V,CER	714618	72982	TZ03Z500YR-174	1		
C	5, 7, 20,		CAP,TA,10UF,+-20%,25V	772491	56289	195D106X0025Y2B	6		
C	22, 24, 35			772491					
C	6, 14, 18		CAP,TA,1.5UF,+-20%,50V	780478	56289	195D155X0050X2B	3		
C	12		CAP,CER,180PF,+-10%,50V,COG,1206	769778	72982	GRM42-6COG181K50VPB	1		
C	13		CAP,CER,33PF,+-10%,50V,COG,1206	769240	72982	GRM42-6COG330K50VPB	1		
C	15		CAP,CER,0.022UF,+-10%,50V,X7R,1206	747279	72982	GRM42-6X7R223K50VPB	1		
C	34		CAP,CER,1500PF,+-10%,50V,COG,1206	781203	72982	GRM42-6COG152K50VPB	1		
C	36		CAP,CER,470PF,+-10%,50V,COG,1206	747360	72982	GRM42-6COG471K50VPB	1		
C	37, 38		CAP,CER,0.01UF,+-10%,50V,X7R,1206	747261	72982	GRM42-6X7R103K50VPB	2		
C	41, 42		CAP,TA,47UF,+-20%,20V	348516	56289	199D476X0020EA4	2		
CR	1- 6, 8,		DIODE,SI,BV=75.0V,IO=100MA,MLF	742064	73445	BAS32	8	1	
CR	11			742064					
CR	7, 9, 10		DIODE,SI,BV=70.0V,IO=50MA,DUAL,SOT23	742320	73445	BAV99	3	2	
CR	12		DIODE,SI,SCHOTTKY,30V,1.1A,SOT89	782573	61752	10JQ030TRRM	1	1	
F	1		FUSE,1/4X1-1/4,FAST,0.25A,250V	109314	71400	AGC1-4	1	5	
F	1		FUSE,5X20MM,FAST,0.25A,250V	543504	71400	GMA1-4	1	5	
J	1		CONN,D-SUB,PWB,RT ANG,15 SCKT	782169	00779	747845-4	1		
J	2		CONN,DIN41612,TYPE R,64 PIN	782094	00779	532523-2	1		
J	3		CONN,D-SUB,PWB,RT ANG,15 PIN	782151	00779	747841-4	1		
J	4		HEADER,1 ROW,0.100CTR,RT ANG,6 PIN	714154	22526	65521-106	1		
J	5		JACK,PWB,RT ANG,4 POS	782086	00779	520949-2	1		
J	6, 7		HEADER,2 ROW,0.100 CTR,40 PIN	603670	00779	2-87227-0	2		
MP	1		FUSE CAP 1/4X1-1/4	460238	61935	031.1666	1		
MP	1		FUSE CAP 5 X 20 MM	461020	61935	031.1663	1		
Q	1	*	TRANSISTOR,SI,N-JFET,DUAL,TO-78	478370	13327	FD1838	1	1	
Q	2, 6, 7,		TRANSISTOR,SI,PNP,SMALL SIGNAL,SOT23	742023	73445	BCX17TRL	4	1	
Q	9			742023					
Q	3, 4, 5,		TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT23	742031	73445	BCX19TRL	4	1	
Q	8			742031					
Q	10, 11	*	TRANSISTOR,SI,BV= 45V, 30W,TO-220	325761	09214	D44C5	2	1	
R	1		RES,CHIP,CERM,33,+-5%,0.125W,1206	746248	09969	CRCW1206330JB02	1		
R	2		RES,CHIP,CERM,3.6K,+-5%,0.125W,1206	746537	09969	CRCW1206362JB02	1		
R	3- 6, 48,		RES,CHIP,CERM,330,+-5%,0.125W,1206	746370	09969	CRCW1206330JB02	6		
R	49			746370					
R	7		RES,CHIP,CERM,150,+-5%,0.125W,1206	746313	09969	CRCW1206151JB02	1		
R	8		RES,CHIP,CERM,15K,+-1%,0.125W,1206	769810	09969	CRCW12061502FB02	1		
R	9		RES,CHIP,CERM,22,+-5%,0.125W,1206	746230	09969	CRCW1206220JB02	1		
R	10- 12, 14,		RES,CHIP,CERM,470,+-5%,0.125W,1206	740506	09969	CRCW1206471JB02	6		
R	21, 28			740506					
R	13, 15		RES,CHIP,CERM,200,+-5%,0.125W,1206	746339	09969	CRCW1206201JB02	2		
R	16, 46, 51,		RES,CHIP,CERM,511,+-1%,0.125W,1206	769869	09969	CRCW12065110FB02	4		
R	59			769869					
R	17, 20, 26,		RES,CHIP,CERM,1K,+-5%,0.125W,1206	745992	09969	CRCW1206102JB02	8		
R	31, 36, 41,			745992					
R	54, 78			745992					
R	18, 22, 23,		RES,CHIP,CERM,4.7K,+-5%,0.125W,1206	740522	09969	CRCW1206472JB02	23		
R	27, 32- 34,			740522					
R	37, 38, 42,			740522					
R	52, 53, 55,			740522					
R	56, 58, 61-			740522					
R	63, 67, 72,			740522					
R	80, 82, 86			740522					
R	19, 35, 84,		RES,CHIP,CERM,47K,+-5%,0.125W,1206	746685	09969	CRCW1206473JB02	4		
R	85			746685					
R	24, 29, 30		RES,CHIP,CERM,9.1K,+-5%,0.125W,1206	746602	09969	CRCW1206912JB02	3		
R	25		RES,CHIP,CERM,3.9K,+-5%,0.125W,1206	746545	09969	CRCW1206392JB02	1		
R	39		RES,CHIP,CERM,470K,+-5%,0.125W,1206	746792	09969	CRCW1206471JB02	1		
R	40, 43, 45,		RES,CHIP,CERM,100,+-5%,0.125W,1206	746297	09969	CRCW1206101JB02	6		
R	47, 79, 81			746297					
R	44		RES,CHIP,CERM,300K,+-5%,0.125W,1206	746768	09969	CRCW1206301JB02	1		
R	50, 57		RES,CHIP,CERM,1.15K,+-1%,0.125W,1206	780981	09969	CRCW12061151FB02	2		
R	60		RES,CHIP,CERM,4.02K,+-1%,0.125W,1206	783266	09969	CRCW12064021FB02	1		
R	64		RES,CHIP,CERM,750,+-5%,0.125W,1206	746404	09969	CRCW1206751JB02	1		
R	65		RES,CHIP,CERM,39K,+-5%,0.125W,1206	746677	09969	CRCW1206393JB02	1		

An * in 'S' column indicates a static-sensitive part.

Table 5-10. A9 Probe I/O Interface PCA (cont.)

REFERENCE DESIGNATOR -A>-	-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
R	68, 75		RES,CHIP,CERM,30.1K,+-1%,0.125W,1206	801258	09969	CRCW12063012FB02	2		
R	69		RES,CHIP,CERM,47,+-5%,0.125W,1206	746263	09969	CRCW1206470JB02	1		
R	70		RES,CHIP,CERM,3.4K,+-1%,0.125W,1206	769844	09969	CRCW12063401FB02	1		
R	71, 74, 76,		RES,CHIP,CERM,10K,+-1%,0.125W,1206	769794	09969	CRCW12061002FB02	4		
R	77			769794					
R	73		RES,CHIP,CERM,620,+-5%,0.125W,1206	745984	09969	CRCW1206621JB02	1		
R	83		RES,CF,2.2,+-5%,0.25W	354944	80031	CR251-4-5P2E2	1	1	
R	87		RES,CHIP,CERM,1.30K,+-1%,0.125W,1206	780999	09969	CRCW12061301FB02	1		
R	88		RES,CHIP,CERM,243,+-1%,0.125W,1206	810606	09969	CRCW12062430FB02	1	1	
R	90		RES,CHIP,CERM,22,+-5%,0.125W,1206	746230	09969	CRCW1206220JB02	1		
TP	1- 7		TERM,UNINSUL,WIRE FORM,TEST POINT	781237	26364	TP-102-01	7		
U	1		ISOLATOR, 20 MHZ OPTOCOUPLER	742817	28480	HCPL-2400,OPTION100	1	1	
U	2	*	IC,FTTL,QUAD 2 INPUT XOR GATE,SOIC	742171	18324	N74F86DT	1	1	
U	3	*	IC,LSTTL,QUAD 2 INPUT NOR GATE,SOIC	741025	18324	N74LS02DT	1	1	
U	4, 12	*	IC,FTTL,HEX INVERTER,SOIC	742148	18324	N74F04DT	2	1	
U	5	*	IC,FTTL,QUAD DUAL AND GATE,SOIC	780957	18324	N7410DT	1	1	
U	6	*	IC,CMOS,HEX INVERTER W/SCHT TRIG,SOIC	780965	18324	N74HCT14DT	1	1	
U	7, 13	*	IC,LSTTL,QUAD 2 INPUT OR GATE,SOIC	740878	18324	N74LS32D	2	1	
U	8	*	IC,LSTTL,2-4 LINE DEMUX,SOIC	740951	18324	N74LS139D	1	1	
U	9	*	IC,FTTL,QUAD 2-1 LINE MUX,SOIC	773028	18324	74F157ADT	1	1	
U	10	*	IC,FTTL,DUAL D F/F,+EDG TRG,SOIC	742163	18324	74F74DT	1	1	
U	11	*	IC,FTTL,QUAD 2 INPUT OR GATE,SOIC	743237	18324	N74F32DT	1	1	
U	14, 15	*	IC,LSTTL,OCTL LINE DRVR,SOIC	742122	18324	N74LS244DT	2	1	
U	16	*	IC,FTTL,DUAL 4-1 LINE MUX,SOIC	772806	18324	74F153D	1	1	
U	17	*	IC,LSTTL,QUAD D F/F,+EDG TRG,SOIC	742619	18324	N74LS175DT	1	1	
U	18	*	IC,STTL,600 GATE ARY,9100A-99100,PLCC	741546	61271	MB113T306	1	1	
U	19	*	IC,STTL,600 GATE ARY,9100A-99101,PLCC	741553	61271	MB113T306	1	1	
U	20, 23	*	IC,BIPOLAR,8-BIT DAL,UP-COMPATIBLE	743112	24355	AD558JN	2	1	
U	21, 22	*	IC,LSTTL,8-BIT BINARY CNTR W/REG,SOIC	782243	01295	SN74LS590DR	2	1	
U	24, 37	*	IC,COMPARATOR,QUAD,14 PIN,SOIC	741561	18324	LM339DT	2	1	
U	25	*	IC,LSTTL,QUAD BUS,SOIC	740977	18324	N74LS125ADT	1	1	
U	26, 32, 33	*	IC,LSTTL, 4 BIT UP/DOWN CNTR,SOIC	742114	18324	N74LS191DT	3	1	
U	27	*	IC,LSTTL,DUAL D F/F,+EDG TRG,SOIC	740985	18324	S74LS74ADT	1	1	
U	28, 29	*	IC,ECL,QUAD ECL-TTL TRANSLATOR	801274	04713	MC10H12SP	2	1	
U	30	*	IC,COMPRTR,DUAL,HI-SPEED,16 PIN DIP	782219	00718	AM687ADL	1	1	
U	31	*	IC,FTTL,QUAD D F/F,+EDG TRG,SOIC	801399	18324	74F175DT	1	1	
U	34	*	IC,FTTL, 4 BIT UP/DOWN COUNTER	782235	07263	74F191DC	1	1	
U	35, 36, 39	*	IC,LSTTL,OCTL BUS TRNSCVR W/3-ST,SOIC	781195	18324	N74LS245D	3	1	
U	38	*	IC,FTTL,DUAL 4 INPUT NAND GATE,SOIC	742155	18324	N74F20DT	1	1	
U	40	*	IC,VOLT REG,FIXED,+5 VOLTS,0.1 AMPS	429910	07263	uA78L05AWC	1	1	
U	41	*	IC,OP AMP,QUAD,LOW POWER,SOIC	742569	18324	LM324D	1	1	
XF	1		HLDR PART,FUSE,BODY,PWB MT	602763	61935	FAU031.3573	1		

An * in 'S' column indicates a static-sensitive part.

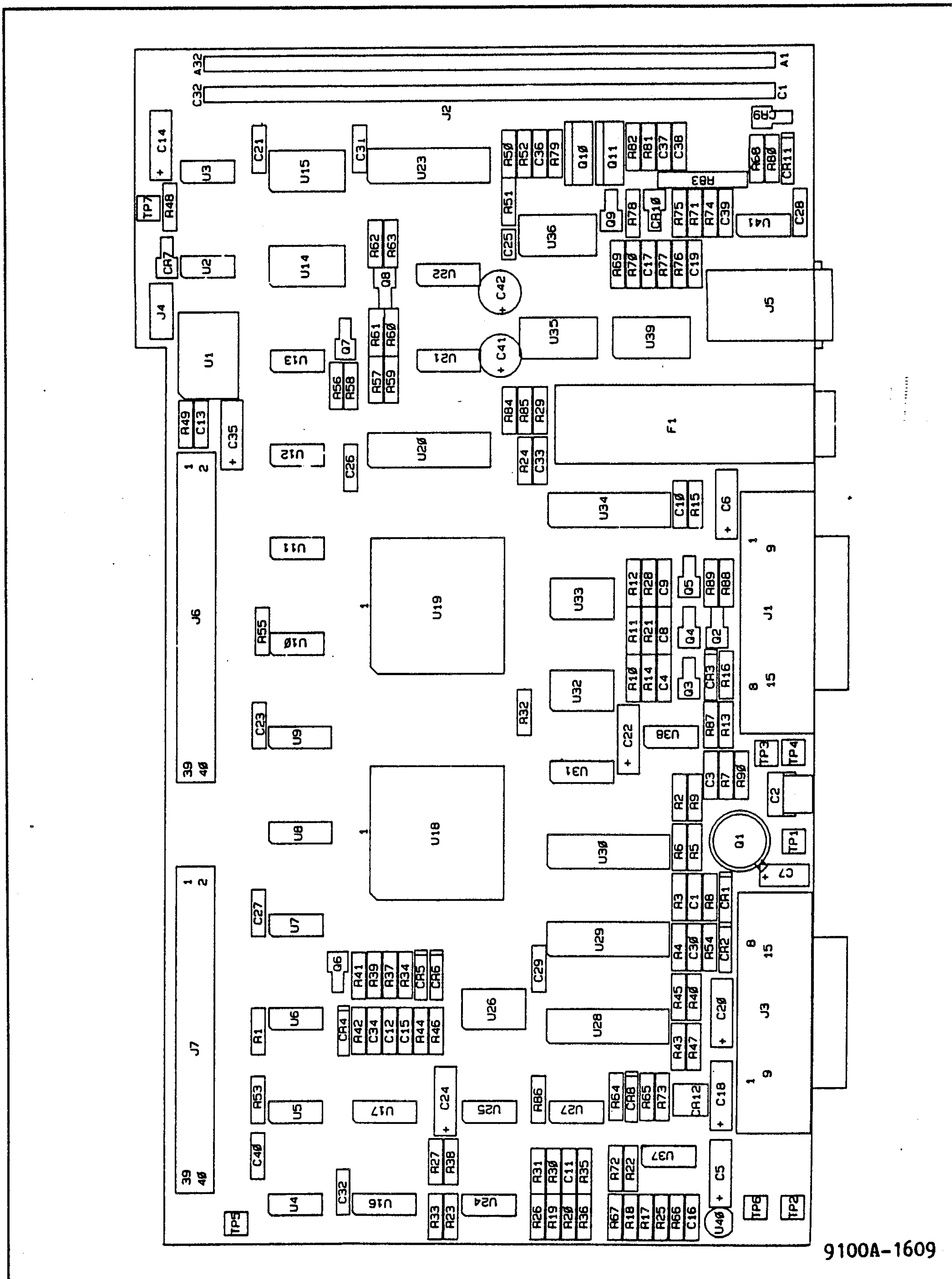


Figure 5-9. A9 Probe I/O Interface PCA

Table 5-11. A10 Multi-Function Interface PCA
(See Figure 5-10.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-	TOT QTY-	R S -Q	N O T -E-
B 1		BATTERY,LITHIUM,3.5V,0.75AH	782953	50120	LTC-7P	1	1	
C 1, 2		CAP,CER,15PF,+-2%,100V,COG	369074	80031	2222-631-10159	2	1	
C 3, 10- 21		CAP,CER,0.01UF,+-20%,100V,X7R	407361	72982	8121-A100-W5R-103M	13		
CR 1	*	DIODE,SI,BV= 75.0V,IO=150MA,500 MW	203323	07910	1N4448	1	1	
H 1		SCREW,THD CUT,PHP,S.STL.4-24X3/8	183574	COMMERCIAL		2		
H 2		RIVET,POP,DOME,AL,0.125X0.316	423616	COMMERCIAL		2		
J 1		CONN,DIN41614,TYPE R,RT ANG,96 SCKT	747816	00779	531796-1	1		
J 2		HEADER,2 ROW,0.100 CTR,RT ANG,50 PIN	783464	00779	1-103311-0	1		
J 3		HEADER,2 ROW,0.100CTR,50 PIN	782201	00779	2-87227-5	1		
MP 1		SCSI CONNECTOR BRACKET	768663	89536	768663	1		
Q 1	*	TRANSISTOR,SI,PNP,SMALL SIGNAL	195974	64713	2N3906	1	1	
Q 2	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	218396	04713	2N3904	1	1	
R 1- 3, 6,		RES,CF,10K,+-5%,0.25W	348839	80031	CR251-4-5P10K	7		
R 7, 9, 12			348839					
R 4		RES,CC,22M,+-5%,0.25W	221986	01121	CB2265	1		
R 5		RES,CF,51K,+-5%,0.25W	376434	80031	CR251-4-5P51K	1		
R 8, 10		RES,CF,200K,+-5%,0.25W	441485	80031	CR251-4-5P200K	2		
RN 1, 2		RES,NET,SIP,10PIN,9RES,220,+-2%	769356	09969	CSC10A01221G	2		
RN 3, 4		RES,NET,SIP,10PIN,9RES,330,+-2%	769364	09969	CSC10A01331G	2		
RN 5		RES,NET,SIP,10PIN,9RES,10K,+-2%	414003	80031	95081002CL	1		
TP 1- 3		TERM,UNINSUL,WIRE FORM,TEST POINT	781237	26364	TP10201	3		
U 2	*	IC,NMOS,SMALL COMPTR SYS INT	742858	00718	AM5380PC	1	1	
U 3	*	IC,20L8, PROGRAMMED LOGIC ARRAY	818211	89536	818211	1	1	
U 9	*	IC,CMOS,PARALLEL,I/O CALENDER & CLOCK	604181	12040	MM58167N	1	1	
U 10	*	IC,LSTTL,8BIT S-IN, P-OUT R-SHIFT RGS	408732	01295	SN74LS164N	1	1	
U 11	*	IC,CMOS,HEX INVERTERS	799924	18324	74HCT04N	1	1	
U 12	*	IC,CMOS,QUAD 2-INPUT NAND GATE	741280	54590	C074HCT00	1	1	
XU 2		SOCKET,IC,40 PIN	429282	09922	DILB40P-108	1		
XU 3		SOCKET,IC,24 PIN,	643999	51398	3852324-02	1		
XU 9		SOCKET,IC,24 PIN	376236	91506	324-AG39D	1		
Y 1	*	CRYSTAL,32.768KHZ,+-0.003%	501817	87516	861T32.768	1	1	

An * in 'S' column indicates a static-sensitive part.

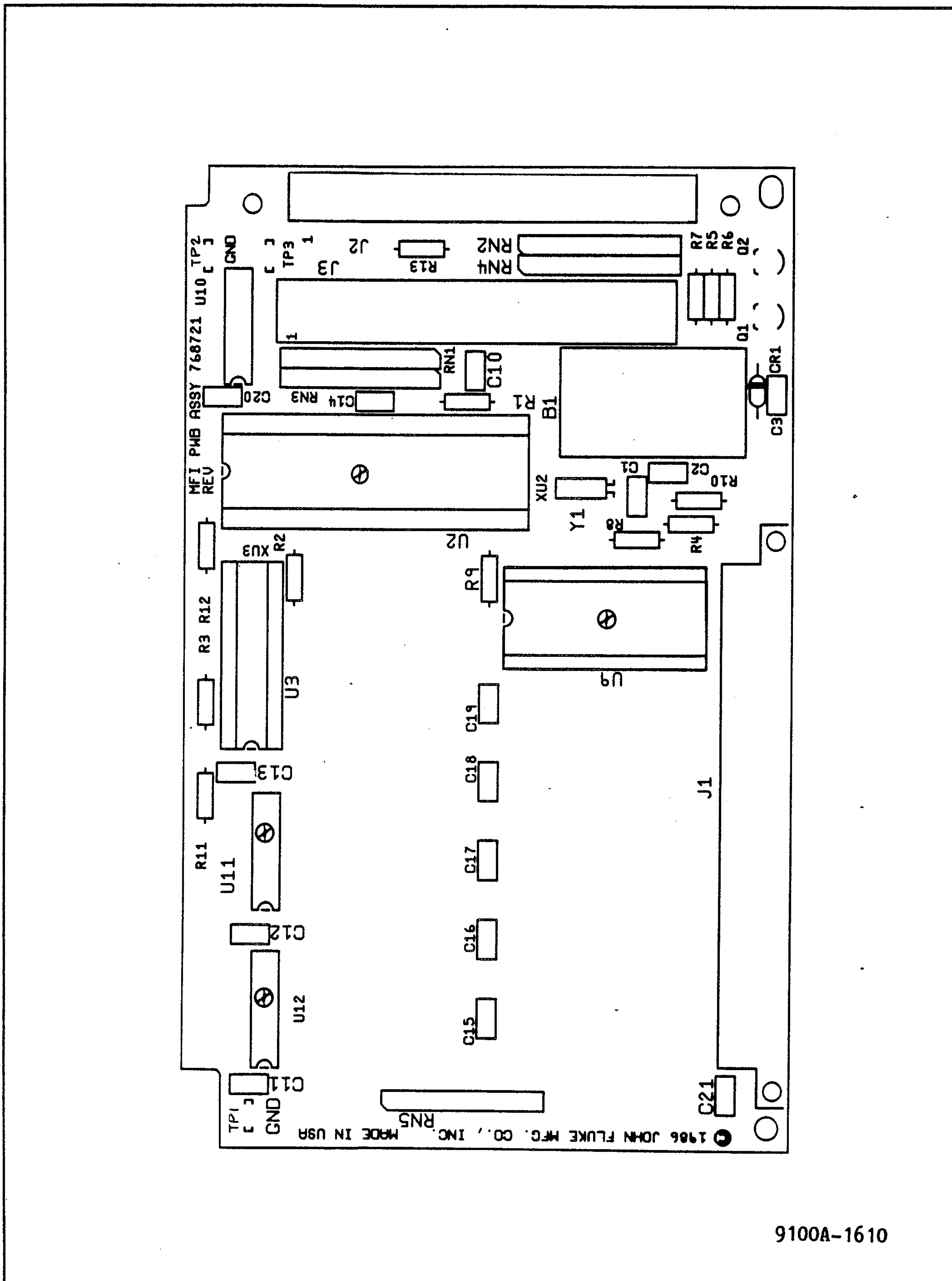
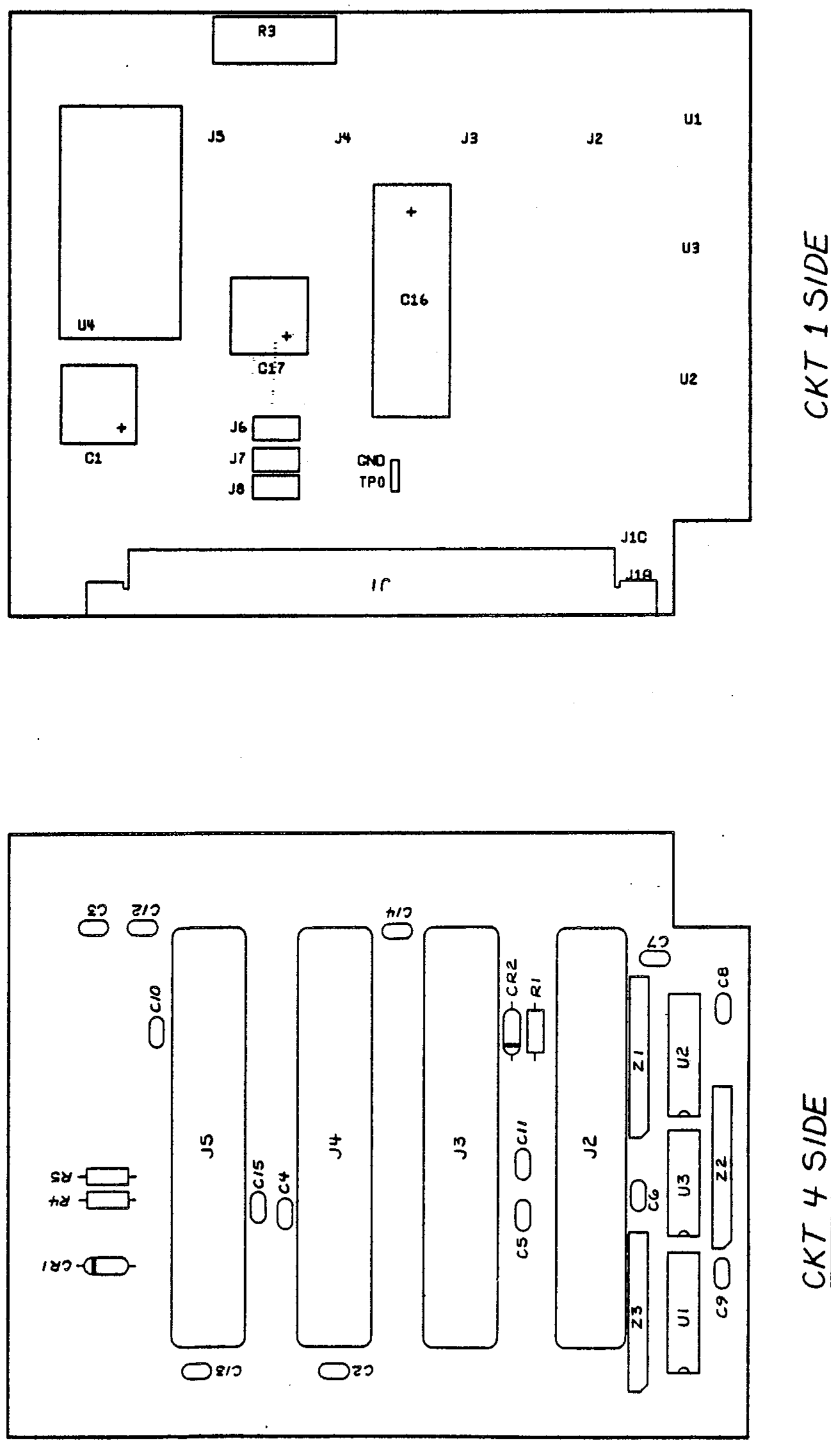


Figure 5-10. A10 Multi-Function Interface PCA

Table 5-12. All I/O Connector PCA
(See Figure 5-11.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C 1, 17		CAP,AL,1000UF,+50-20%,35V	641217	57640	SM35VB-1000	2		
C 2- 15		CAP,CER,0.01UF,+-20%,100V,X7R	407361	72982	8121-A100-W5R-103M	14	1	
C 16		CAP,AL,10000UF,+-20%,6.3V,SOLV PROOF	800045	62643	SME6.3T103M16X40LL	1		
CR 1, 2	*	DIODE,SI,100 PIV,1.0 AMP	343491	01295	1N4002	2	1	
H 1		SCREW,MACH,PH,P,STL,6-32X0.250	152140	COMMERCIAL		2		
H 2		SCREW,THD CUT,PHP,S.STL,4-24X3/8	183574	COMMERCIAL		2		
J 1		CONN,DIN41612,TYPE R,RT ANG,64 SCKT	782102	00779	531796-2	1		
J 2- 5		CONN,D-SUB,PWB,37 SCKT	782177	00779	2-747709-0	4		
MP 1		HEAT DISSIPATOR,1.000,FOR TO-66	799965	30161	ER5758B	1		
R 1		RES,CF,10K,+-5%,0.25W	348839	80031	CR251-4-5P10K	1		
R 3		RES,WW,0.47,+-5%,2W	219360	23237	SPH247-5	1	1	
R 4		RES,MF,243,+-0.1%,0.125W,50PPM	512228	09969	CMF55-2430-B-T2	1		
R 5		RES,MF,732,+-1%,0.125W,100PPM	294884	81349	RNC60H7320F	1		
TP 1		TERM,UNINSUL,WIRE FORM,TEST POINT	781237	26364	TP102-01	1		
U 1, 2	*	IC,ECL,QUAD TTL-ECL TRANSLATOR	801266	04713	MC10H124P	2	1	
U 3	*	IC,LSTTL,DUAL 4 INPUT NAND GATE	393280	01295	SN74LS20N	1	1	
U 4	*	IC,VOLT REG,ADJ,1.2 TO 32 V,5 AMP OUT	585497	12040	LM338K	1	1	
Z 1, 3		RES,NET,SIP,10PIN,9RES,330,+-2%	769364	04713	SN74LS20N	2		
Z 2		RES,NET,SIP,10PIN,9RES,4.7K,+-2%	484063	80031	95081002CL	1		

An * in 'S' column indicates a static-sensitive part.



9100A-1611

Figure 5-11. A11 I/O Connector PCA

Table 5-13. A12 Half-Width Clip Modules

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C	1		CAP,CER,0.1UF,+-20%,50V,Z5U	597575	72982	RPE110Z5U104M50V	1		
C	2		CAP,CER,0.01UF,+-20%,100V,X7R	407361	72982	8121-A100-W5R-103M	1		
H	1		SCREW, MACH, PHP, STL, 4-40 X 5/8	800656	COMMERCIAL		4		
J	1		CONN,RECT,PWB,PLUG,33 POS	800680	50541	KA33/127BPMD11T	1	1	
J	2, 3		CONNECTOR ASSY		89536		2		1
MP	1		CLIP,TEST,IC		89536		1	2	1
MP	2		CLIP,HOOK,W/0.025 PIN INTERFACE,BLACK	757500	05276	4521-0	1	2	
MP	3		BUTTON, SWITCH	773895	89536	773895	1		
MP	4		MODULE BOTTOM, SINGLE	768697	89536	768697	1		
MP	5		MODULE TOP, SINGLE	774034	89536	774034	1		
MP	6		KEY		89536		2		1
MP	7		MODULE DECAL		89536		1		1
P	1, 2		BANANA PLUG,PWB,SOLDER OR SWAGE TYPE	800698	88245	1781B-1	2		
S	1		SWITCH,PUSHBUTTON,SPST,MOMENTARY	782433	5N615	B3F-3122	1	1	
S	2		SWITCH,DIP,SPST,4 POS	408559	00779	435166-2	1		
W	1		CABLE SET ASSY		89536		1		1
W	2		WIRE ASSY, GROUND CLIP	801704	89536	801704	1	1	

An * in 'S' column indicates a static-sensitive part.

NOTES:

1 = Refer to the table below for appropriate part numbers for each type of Clip Module:

	MODULE -14D	-14S	-16D	-16S	-18D	-20D	-20S	-24D	-24S
MP1	800052	817429	800060	817437	800078	800086	817445	800094	817478
W1	801639	801639	801647	801647	801654	801662	801662	801670	801670
J2,3	801878	801878	801886	801886	801894	801902	801902	801910	801910
MP6	-	-	-	-	773952	773952	773952	767954	767954
MP7	802140	819631	802157	819649	802165	802173	819656	802181	819664

Table 5-14. A13 Full-Width Clip Modules

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C	1, 4		CAP,CER,0.01UF,+-20%,100V,X7R	407361	72982	8121-A100-W5R-103M	2		
C	2, 3		CAP,CER,0.1UF,+-20%,50V,Z5U	597575	72982	RPE110Z5U104M50V	2		
H	1		SCREW, MACH, PHP, STL, 4-40 X 5/8	800656	COMMERCIAL		4		
J	1, 2		CONN,RECT,PWB,PLUG,33 POS	800680	50541	KA33/127BPMD11T	2	1	
J	3, 4		CONNECTOR ASSY, 20 PIN		89536		2		1
MP	1		CLIP,TEST,IC		89536		1	2	1
MP	2		CLIP,HOOK,W/0.025 PIN INTERFACE,BLACK	757500	05276	4521-0	1	2	
MP	3		BUTTON, SWITCH	773895	89536	773895	1		
MP	4		MODULE BOTTOM, DOUBLE	802132	89536	802132	1		
MP	5		MODULE TOP, DOUBLE	802124	89536	802124	1		
MP	6		KEY, EXTENDED	767954	89536	767954	2		
MP	7		MODULE DECAL		89536		1		1
P	1- 4		BANANA PLUG,PWB,SOLDER OR SWAGE TYPE	800698	88245	1781B-1	2		
S	1		SWITCH,PUSHBUTTON,SPST,MOMENTARY	782433	5N615	B3F-3122	1	1	
S	2		SWITCH,DIP,SPST,8 POS	408559	00779	435166-2	1		
W	1		CABLE SET ASSY		89536		1		1
W	2		WIRE ASSY, GROUND CLIP	801704	89536	801704	1	1	

An * in 'S' column indicates a static-sensitive part.

NOTES:

1 - Refer to the table below for appropriate part numbers for each type of Clip Module:

	MODULE -28D	-28S	-40D
MP1	800102	821975	800110
W1	801688	801688	801696
J3,4	801928	801928	801936
MP7	802199	819672	802207

Table 5-15. A14 Calibration Module

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-	TOT QTY-	R S -Q	N O T -E-
H	1		SCREW, MACH, PHP, STL, 4-40 X 5/8	800656	COMMERCIAL		7		
J	1, 2		CONN,RECT,PWB,PLUG,33 POS	800680	50541	KA33/127BPMD11T	2	1	
MP	2		TEST LEAD,CLIP-TO-CLIP,BLK,20AWG	801050	05276	E11395-36-0	1	1	
MP	3		CABLE TIE,4"L,0.100"W,0.75 DIA	172080	06383	SST1M	2		
MP	4		BUTTON, SWITCH	773895	89536	773895	1		
MP	5		MODULE BOTTOM, DOUBLE	802132	89536	802132	1		
MP	6		MODULE TOP, DOUBLE	802124	89536	802124	1		
MP	7		KEY, EXTENDED	767954	89536	767954	2		
MP	8		MODULE DECAL, CALIBRATION	802223	89536	802223	1		
P	1- 4		BANANA PLUG,PWB,SOLDER OR SWAGE TYPE	800698	88245	1781B-1	2		
S	1		SWITCH,PUSHBUTTON,SPST,MOMENTARY	782433	5N615	B3F-3122	1	1	

An * in 'S' column indicates a static-sensitive part.

Table 5-16. A15 Flying Lead Module

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C 1		CAP,CER,0.1UF,+-20%,50V,Z5U	597575	72982	RPE110Z5U104M50V	1		
C 2		CAP,CER,0.01UF,+-20%,100V,X7R	407361	72982	8121-A100-W5R-103M	1		
H 1		SCREW, MACH, PHP, STL, 4-40 X 5/8	800656	COMMERCIAL		4		
J 1		CONN,RECT,PWB,PLUG,33 POS	800680	50541	KA33/127BPMD11T	1	1	
MP 1		BUTTON, SWITCH	773895	89536	773895	1		
MP 2		MODULE BOTTOM, SINGLE	768697	89536	768697	1		
MP 3		MODULE TOP, SINGLE	774034	89536	774034	1		
MP 4		KEY	773952	89536	773952	2		
MP 5		MODULE DECAL	802215	89536	802215	1		
MP 6		CLIP, HOOK	757500	05276	4521-0	25	10	
P 1, 2		BANANA PLUG,PWB,SOLDER OR SWAGE TYPE	800698	88245	1781B-1	2		
S 1		SWITCH,PUSHBUTTON,SPST,MOMENTARY	782433	5N615	B3F-3122	1	1	
S 2		SWITCH,DIP,SPST,4 POS	408559	00779	435166-2	1		
W 1		CABLE ASSY, 10 PAIR, POS 1-10	801712	89536	801712	1		
W 2		CABLE ASSY, 10 PAIR, POS 1-10	801720	89536	801720	1		

An * in 'S' column indicates a static-sensitive part.

Table 5-17. A16 512K RAM Module
(See Figure 5-12.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	----DESCRIPTION----	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C 1- 22		CAP,CER,0.1UF,+/-10%,25V,X7R,1206	747287	72982	GRM42-6X7R104K25VPB	22		
C 23		CAP,CER,47PF,+-10%,50V,COG,1206	747352	72982	GRM42-6COG470K50VPB	1		
U 1- 9, 11-	*	IC, NMOS, 256K X 1 DRAM, 120NSEC, PLC	808212	01295	TM4256-12FML	18	1	
U 19	*		808212					
U 10	*	IC,ALSTTL,OCTAL BUS TRANSCEIVER,SOIC	799593	01295	SN74ALS245ADWR	1	1	
U 20	*	IC,ALSTTL,QUAD 2 INPUT NAND GATE,SOIC	782268	01295	SN74ALS00ADR	1	1	
U 21	*	IC,ALSTTL,QUAD 2 INPUT OR GATE,SOIC	742460	01295	SN74ALS32DR	1	1	
U 22	*	IC,ALSTTL,DUAL JK F/F,-EDG TRG,SOIC	807578	01295	SN74ALS112ADR	1	1	

An * in 'S' column indicates a static-sensitive part.

NOTE

The 9105A-007 uses two A16 512K RAM Modules.

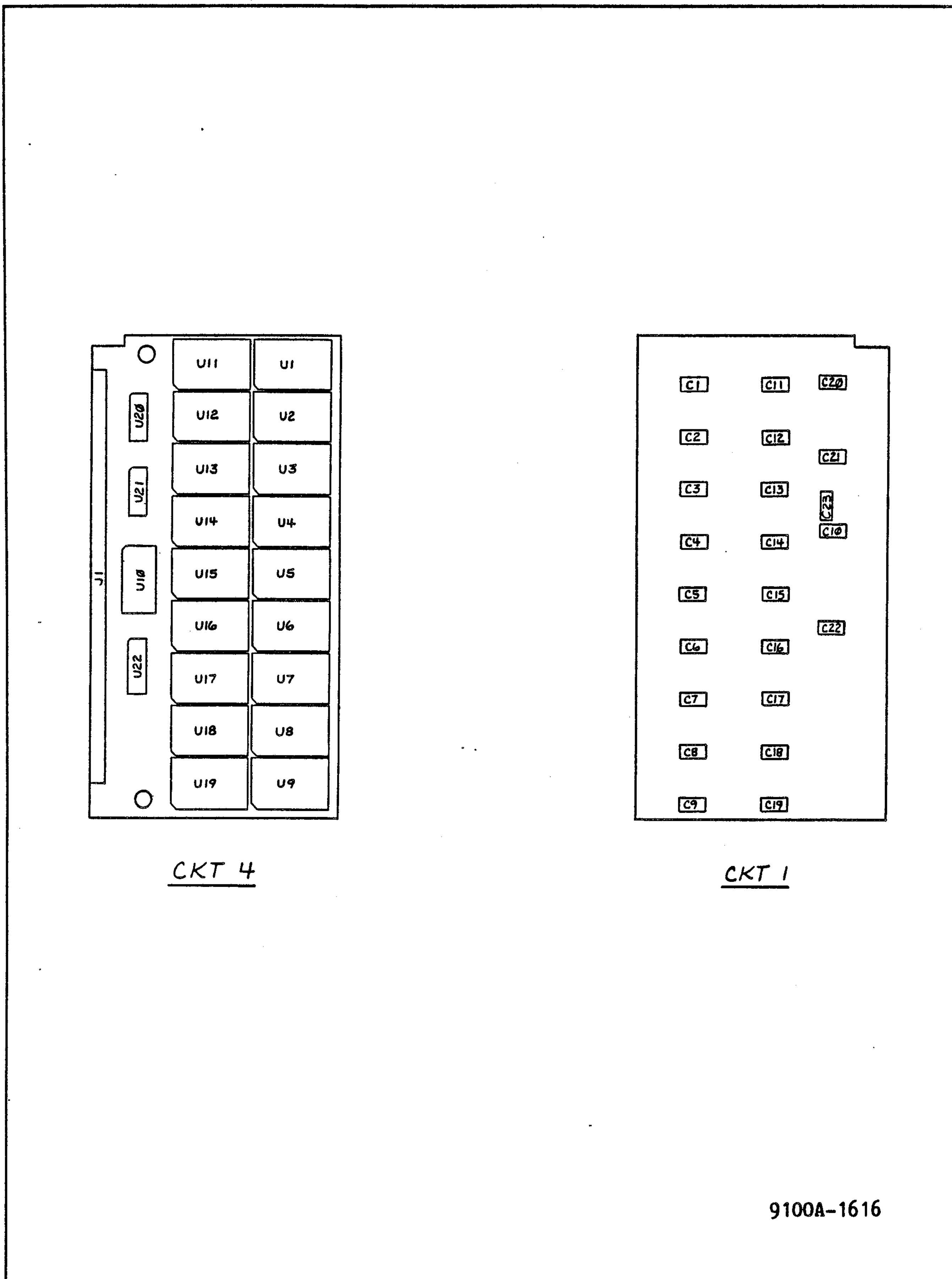


Figure 5-12. A16 512K RAM Module

Table 5-18. A19 Monochrome Monitor

REFERENCE DESIGNATOR -A-	-NUMERICS-	S	DESCRIPTION	FLUKE STOCK -NO-	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-	TOT QTY	R S -Q	N O T -E-
BT	1		POWER SUP,40W,+5@3.5A,+12@2A,-12@1A	769406	61852	XL40-3621	1		
H	1		SCREW,MACH,PH,P,STL,10-32X0.375	114314	73734	19084	4		
H	2		WASHER,FLAT,STEEL,0.203X0.434X0.031	110262	COMMERCIAL		3		
H	3		WASHER,FLAT,STL,.149,.375,.031	110270	COMMERCIAL		8		
H	4		SCREW,MACH,PH,P,STL,6-32X0.375	152165	COMMERCIAL		8		
H	5		SCREW,MACH,SEMS,PH,P,STL,6-32X0.375	177022	COMMERCIAL		3		
H	6		SCREW,MACH,SEMS,PH,P,STL,6-32X0.375	177022	COMMERCIAL		5		
H	7		SCREW,MACH,PHP SEMS,STL,4-40X1/4	185918	COMMERCIAL		6		
H	8		CONN ACC,D-SUB,LATCH BLOCK,SHORT,4-40	783480	00779	745403-9	2		
H	9		SCREW,MACH,PH,P,STL,6-32X1.000	114215	COMMERCIAL		3		
H	10		WASHER,FLAT,STL,.149,.375,.031	110270	88044	AN960-6	3		
H	11		SCREW,MACH,SEMS,PH,P,STL,6-32X0.375	177022	COMMERCIAL		4		
MP	1		BRACKET,CRT,FINISHED	794149	89536	794149	4	1	
MP	2		LABEL,BAR-CODE,9.4 CPI,0.245X1.25	807099	89536	807099	2		
MP	3		CHASSIS,FINISHED	794156	89536	794156	1		
MP	4		SPACER,PWB,NYL,.312	780619	30838	215-150913-01	3		
MP	5		BEZEL ASSY,9100	792903	89536	792903	1		
MP	6		GASKET,TOUCH PANEL,DUST	843250	89536	843250	1		
MP	7		NAMEPLATE	787275	89536	787275	1		
MP	8		COVER,CHASSIS,9100,FINISHED	794198	89536	794198	1		
MP	9		DAMPER, VIBRATION	805085	89536	805085	4		
MP	10		CABLE TIE ANCHOR,ADHSV,0.160"TIE	407908	06383	ABMM-A-C	5		
MP	11		CABLE TIE,4"L,0.100"W,0.75 DIA	172080	06383	SST2M	8		
MP	12		DECAL,COVER,9100	792911	89536	792911	1		
MP	13		DECAL, FAN PANEL	785493	89536	785493	1		
MP	14		BRACKET,POT MOUNTING,FINISHED	794131	89536	794131	1		
MP	15		THUMBWHEEL, POTENTIOMETER	787358	89536	787358	1		
MP	16		SHIPPING BOX	776435	89536	776435	1		
MP	17		SHIPPING INSERT	777045	89536	777045	1		
MP	18		OPTION TRAY	801613	89536	801613	1		
MP	19		SHIPPING CARRIER/INSERT	777052	89536	777052	1		
MP	20		INSERT,OPTION TRAY	809616	89536	809616	1		
MP	21		ENCLOSURE W/GRILLS	802454	89536	802454	1		
MP	22		COVER, FAN	787366	89536	787366	1		
MP	23		DECAL,CAUTION	787242	89536	787242	1		
MP	24		BASE	747972	89536	747972	1		
MP	25		RETAINER, NUT	749655	89536	749655	1		
MP	26		BUSHING COVER RF OUTPUT	802553	89536	802553	1		
MP	27		SHOULDER WASHER	792861	89536	792861	2		
MP	28		RETAINER PIN	802520	89536	802520	1		
MP	29		BASE, MOUNTING PLATE	747998	89536	747998	1		
MP	30		FOOT,RUBBER,SELF-ADHESIVE,BLACK	513820	28213	SJ5012	4		
MP	31		PIN,MECHANICAL,CLEVIS,5/16 X 1-3/4	800524	96652	11-099	1		
MP	32		SPRING,COIL,COMP,SQUARED END,M WIRE	800532	83553	C1100-125-0880M	1		
MP	33		BUMPER,STEM,BUNA-S,0.500X0.125	800839	59000	6171	4		
MP	34		ASSY, AC POWER PANEL	776377	89536	776377	1		
MP	35		DISPLAY, MONITOR GREEN	785444	89536	785444	1		
MP	36		CONTRAST OVERLAY	819987	89536	819987	0	1	1
W	1		CORD,LINE,5-15/IEC,3-18AWG,SVT	284174	70903	17239	1		
W	2		CABLE ASSY,9100	778613	89536	778613	1		

An * in 'S' column indicates a static-sensitive part.

NOTE 1 - Contrast overlay is part of the bezel assembly..

Table 5-19. Option -003 Parallel I/O Module
(See Figure 5-13.)

REFERENCE DESIGNATOR -A>-NUMERICS---->		S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
A	7	*	I/O MODULE (MAIN) PCA	768838	89536	768838	1		
A	8	*	I/O MODULE (TOP) PCA	755611	89536	755611	1		
A	14		CALIBRATION MODULE	813980	89536	813980	1		
A	15		FLYING LEAD MODULE, 20 LEAD SET, TSTD	819763	89536	819763	1		
F	1		FUSE,1/4 X 1-1/4,SLOW,1.0A,250V	109272	71400	MDL1A	1	5	
F	1		FUSE,5X20MM,SLOW,1A,250V	808055	61935	034.3117	1	5	
H	1		SCREW,MACH,PHP,STL,6-32 X 7/8	801241	COMMERCIAL		4		
H	2		SCREW,MACH,PHP SEMS,STL,6-32X1/4	178533	COMMERCIAL		9		
MP	1		HLDR PART,FUSE,CAP,1/4X1-1/4	460238	61935	031.1666	1		
MP	2		HLDR PART,FUSE,CAP,5X20MM	461020	61935	031.1663	1		
MP	3		CASE TOP, I/O MODULE	773291	89536	773291	1		
MP	4		CASE BOTTOM, I/O MODULE	773283	89536	773283	1		
MP	5		DECAL, CASE TOP, I/O MODULE	805630	89536	805630	1		
MP	6		DECAL, CASE BOTTOM, I/O MODULE	773382	89536	773382	1		
MP	7		SHIELD, I/O MODULE	775866	89536	775866	1		
MP	8		FOOT, NON-SKID	774000	89536	774000	4		
MP	9		NAMEPLATE, SERIAL -REAR PANEL-	472795	89536	472795	1		
MP	10		CARTON KEYBOARD, I/O	805804	89536	805804	1		
MP	11		FOAM INSERT, KEYBOARD-I/O	805812	89536	805812	1		
MP	12		CONVOLUTED FOAM, KEYBOARD-I/O	805820	89536	805820	1		
W	1		CABLE ASSEMBLY, EXTERNAL EVENT	773945	89536	773945	1	1	
W	2		CABLE ASSY, I/O MODULE	783977	89536	783977	1		
W	3		WIRE,SHIELD CONTACT	803122	89536	803122	1		

An * in 'S' column indicates a static-sensitive part.

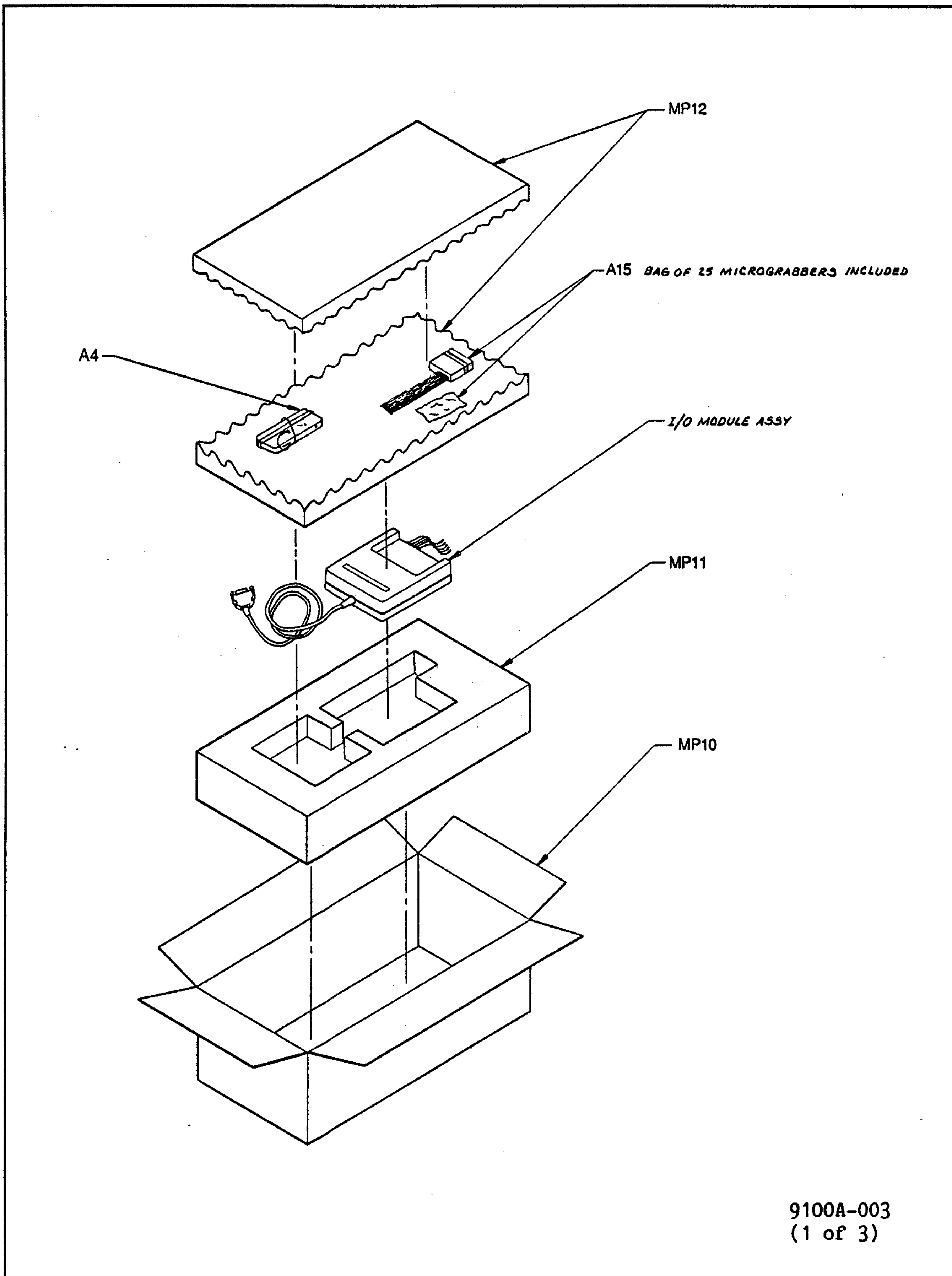


Figure 5-13. Option -003 Parallel I/O Module

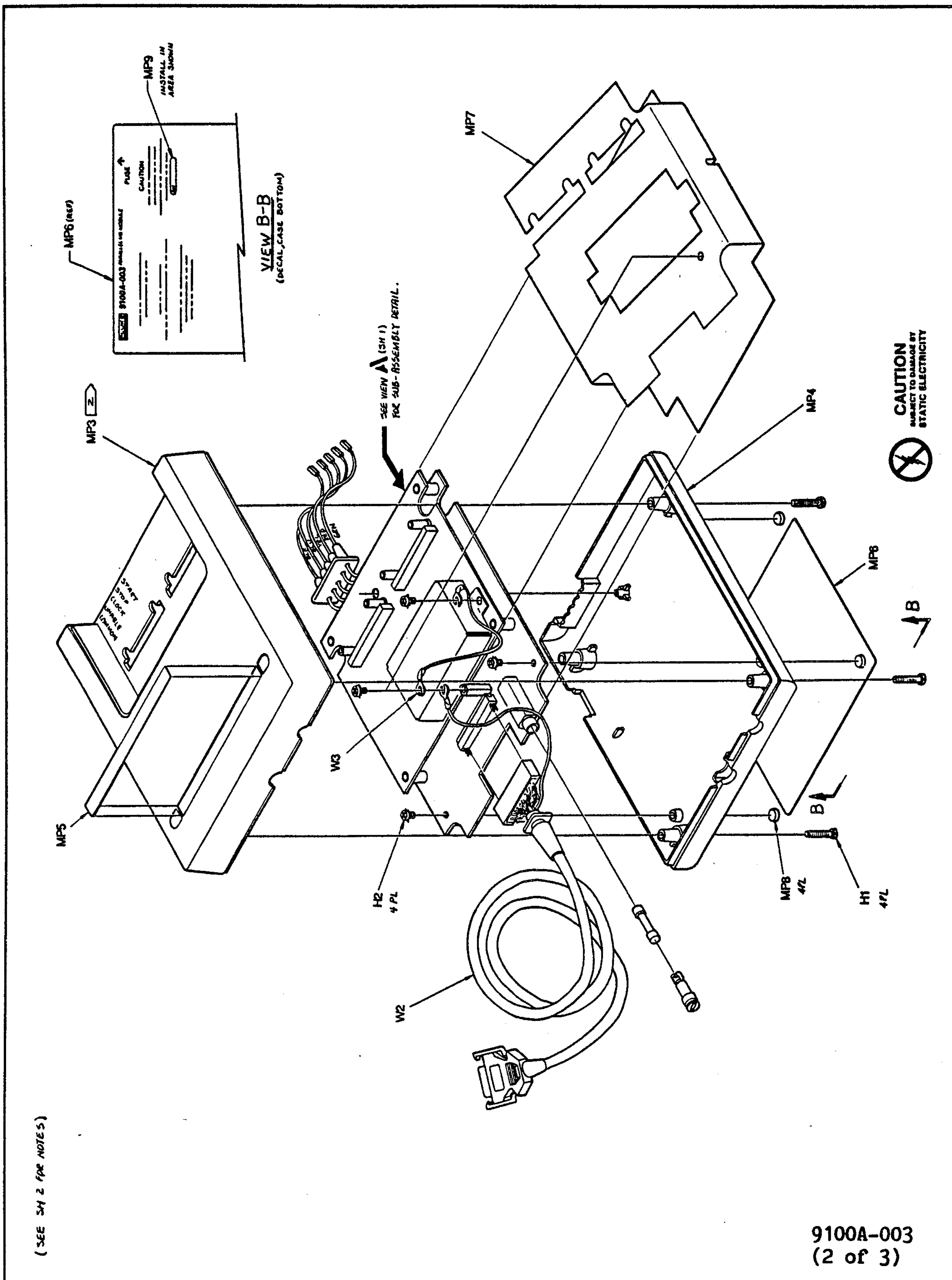
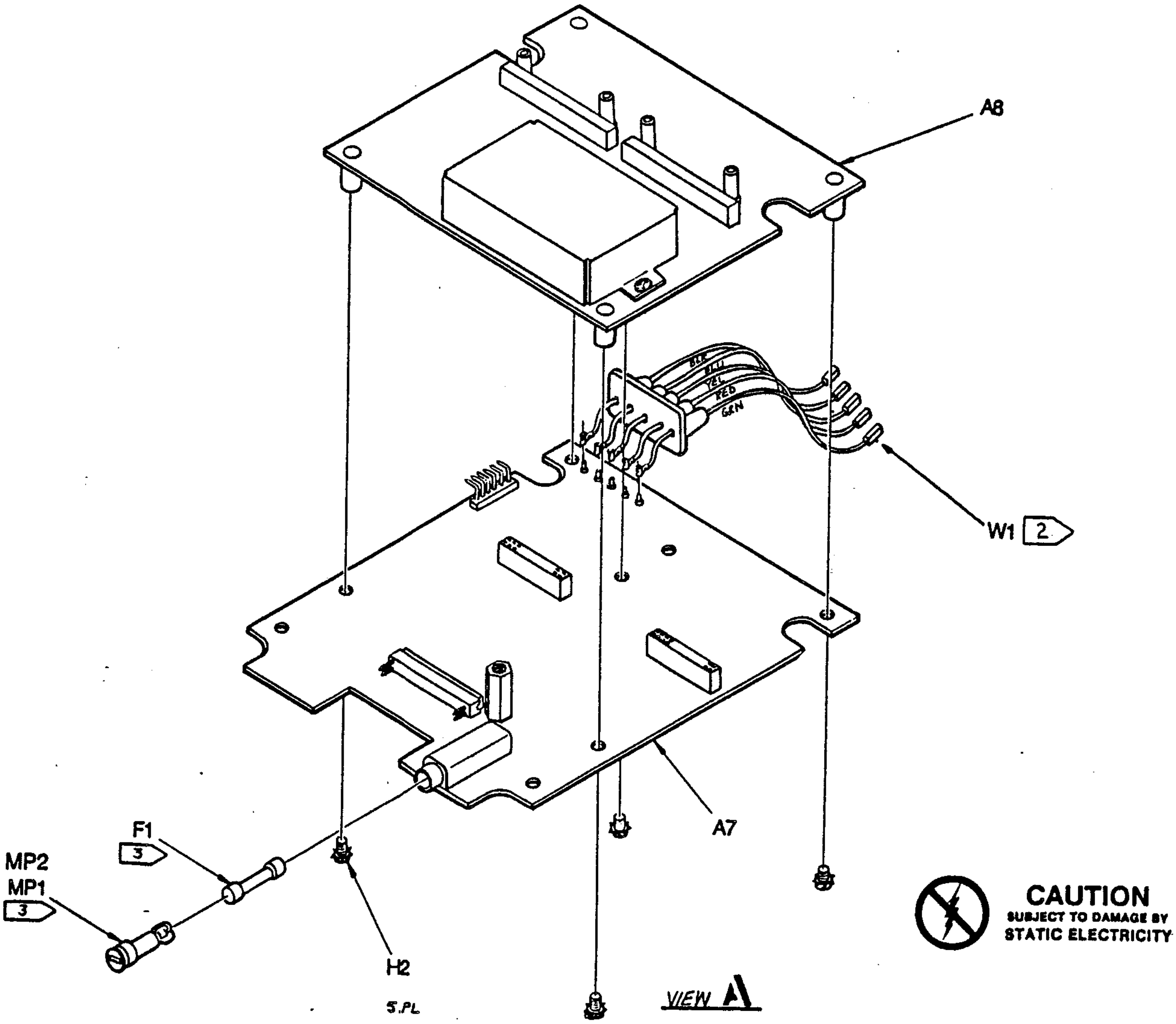


Figure 5-13. Option -003 Parallel I/O Module (cont.)



NOTES: UNLESS OTHERWISE SPECIFIED.

1. **WARNING:** Ⓢ INDICATES USAGE OF MOS DEVICE(S) WHICH MAY BE DAMAGED BY STATIC DISCHARGE. USE SPECIAL HANDLING PER S.O.P. 19.1

2. CABLE NOMENCLATURE ON MP3 CASE TOP SHALL MATCH UP WITH COLORS OF W1 AS NOTED:
   COMMON - BLACK WIRE
   UNABLE - BLUE WIRE
   CLOCK - YELLOW WIRE
   STOP - RED WIRE
   START - GREEN WIRE

3. FUSE & FUSE CAP VARY FOR DIFFERENT VOLTAGE CONFIGURATIONS: SEE FUSE CHART FOR FUSE & CAP PART NO.S.

FUSE CHART 3			CONFIGURATION	
VOLTAGE	FUSE	CAP		
100/120V	109272	460238	115V	763649
220/240V	808055	461020	230V	763656

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Figure 5-13. Option -003 Parallel I/O Module (cont.)

Table 5-20. Option -004 Programmer's Station, Monochrome
(See Figure 5-14.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	---------------DESCRIPTION---------------	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
A	4	*	VIDEO CONTROLLER PCA	768762	89536	768762	1		
A	19		MONOCHROME MONITOR	826362	89536	826362	1		
A	103		KEYBOARD,ASYNC ASCII, 1200 BAUD	757120	76854	5-64995-131	1		1
H	1		RIVET,POP,DOME,AL,0.125X0.316	423616	COMMERCIAL		2		
MP	2		VIDEO CONNECTOR BRACKET	768648	89536	768648	1		
MP	3		NAMEPLATE, SERIAL -REAR PANEL-	472795	89536	472795	1		
MP	4		PROGRAMMER SOFTWARE SYSTEM, SLEEVED		89536		1		2
MP	5		CARTON KEYBOARD, I/O	805804	89536	805804	1		
MP	6		CONVOLUTED FOAM, KEYBOARD-I/O	805820	89536	805820	1		
MP	7		PROGRAM COPY PROTECTION SHEET	847066	89536	847066	1		
TM	1		9100A TL/1 REFERENCE MANUAL	818047	89536	818047	1		
TM	2		9100A PROGRAMMERS MANUAL	813857	89536	813857	1		
U	5	*	PROGRAMMED 27128-150	818195	89536	818195	1		
W	1		CABLE, MONITOR	787903	89536	787903	1		
Z	1		JUMPER,DIP,0.300CTR,PROGRAM,16 POS	783183	51167	16-680-191T	1		

An * in 'S' column indicates a static-sensitive part.

NOTES:

1 - See 9100A-013 option for replacement parts breakdown for A103.

2 - This software available only for 9100A's with Programmer's Station installed. Contact the factory if replacement is needed.

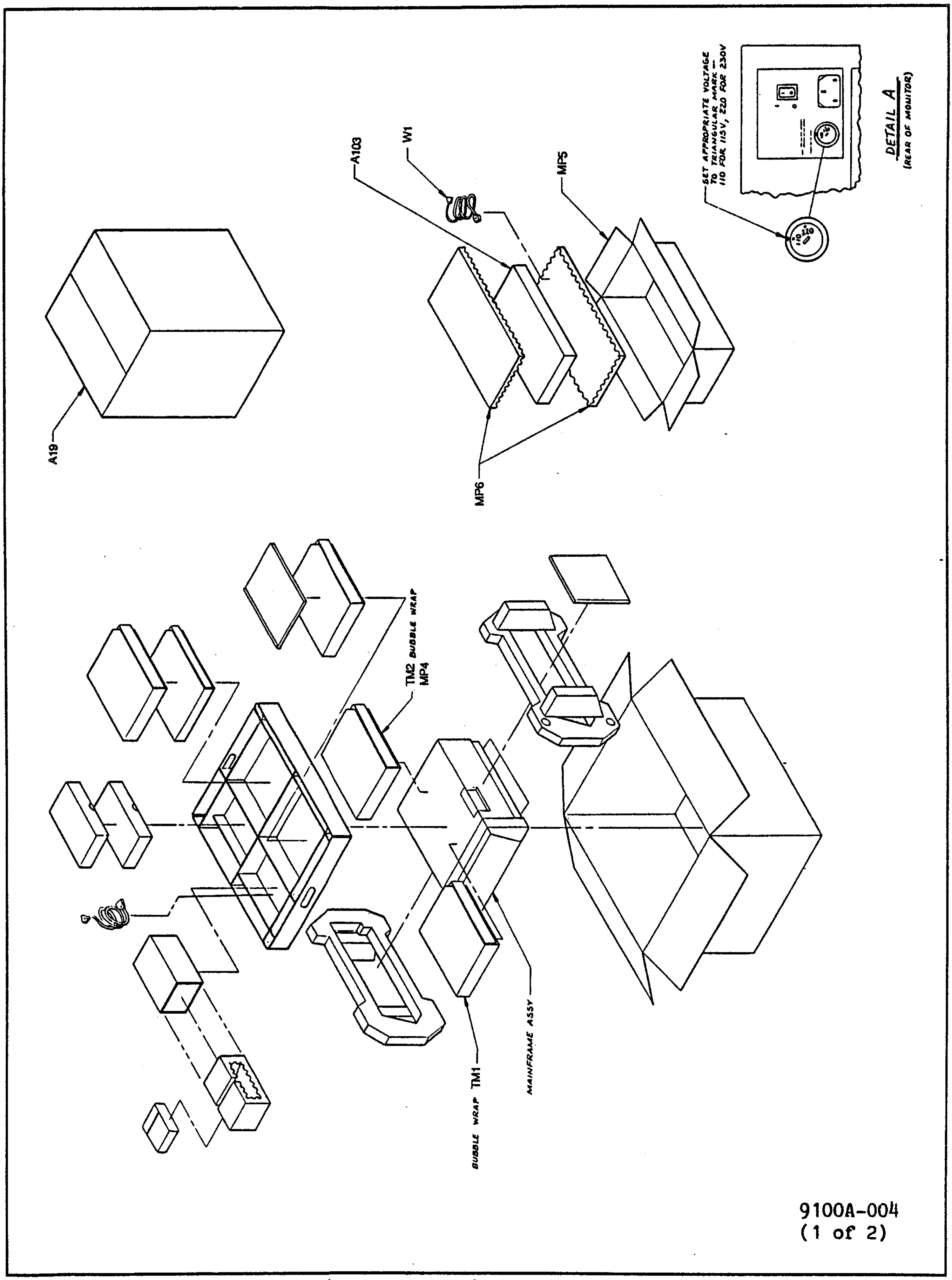

Figure 5-14. Option -004 Programmer's Station, Mono

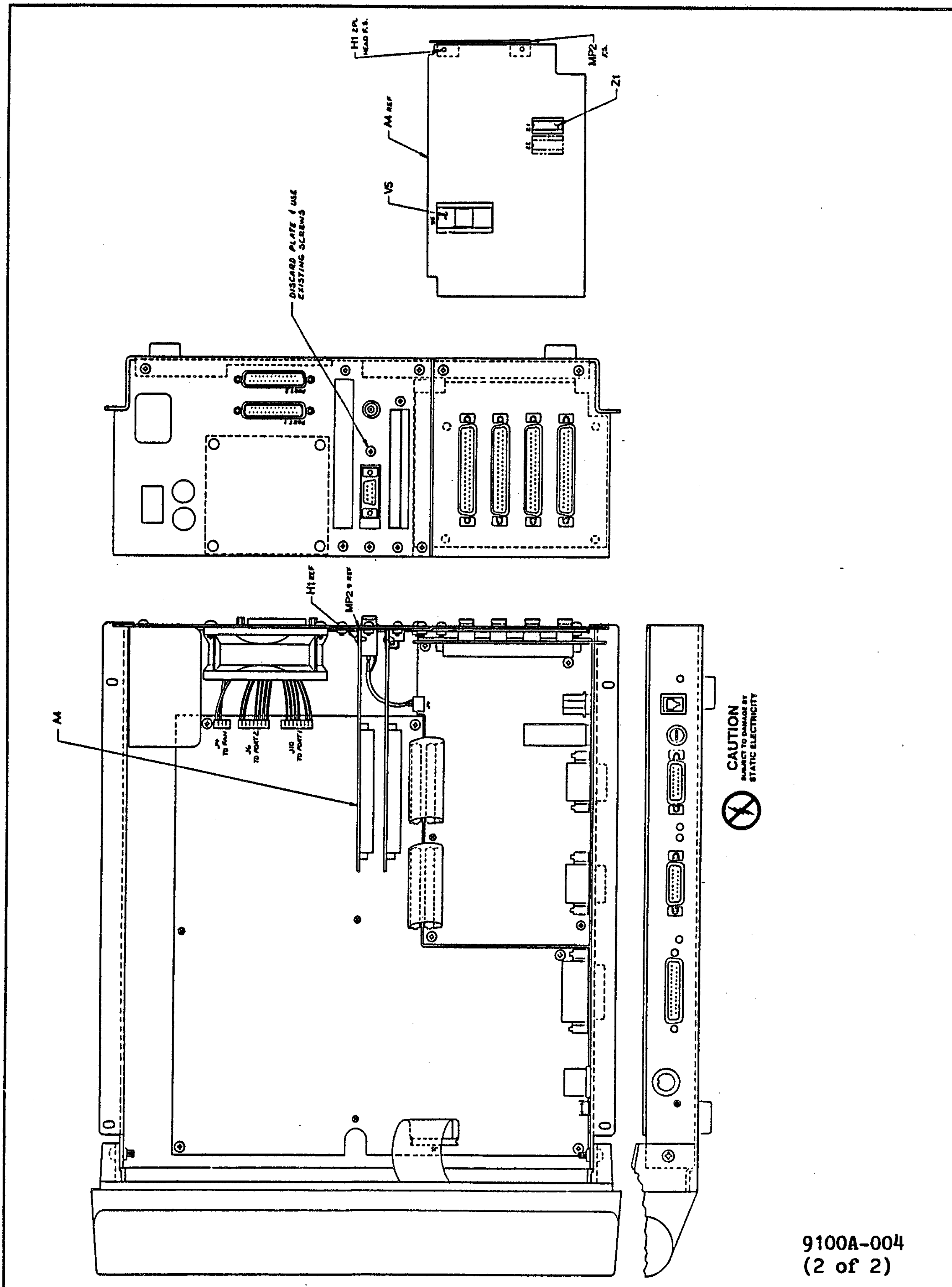

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Figure 5-14. Option -004 Programmer's Station, Mono (cont.)

Table 5-21. Option -005 Programmer's Station, Color
(See Figure 5-15.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
A	4	*	VIDEO CONTROLLER PCA	768762	89536	768762	1		
A	103		KEYBOARD,ASYNC ASCII,1200 BAUD	757120	76854	5-64995-131	1		1
H	1		RIVET,POP,DOME,STL,0.250X0.720	187625	COMMERCIAL		2		
MP	2		VIDEO CONNECTOR BRACKET	768648	89536	768648	1		
MP	3		PROGRAMMER SOFTWARE SYSTEM, SLEEVED		89536		1		2
MP	4		CARTON KEYBOARD, I/O	805804	89536	805804	1		
MP	5		CONVOLUTED FOAM, KEYBOARD-I/O	805820	89536	805820	1		
MP	6		PROGRAM COPY PROTECTION SHEET	847066	89536	847066	1		
TM	1		9100A TL/1 REFERENCE MANUAL	818047	89536	818047	1		
TM	2		9100A PROGRAMMERS MANUAL	813857	89536	813857	1		
U	5	*	PROGRAMMED 27128-150	818195	89536	818195	1		
Z	2		JUMPER,DIP,0.300CTR,PROGRAM,16 POS	783183	51167	16-680-191T	1		

An * in 'S' column indicates a static-sensitive part.

NOTES:

1 = See 9100A-013 option for replacement parts breakdown for A103.

2 = This software available only for 9100A's with Programmer's Station installed. Contact the factory if replacement is needed.

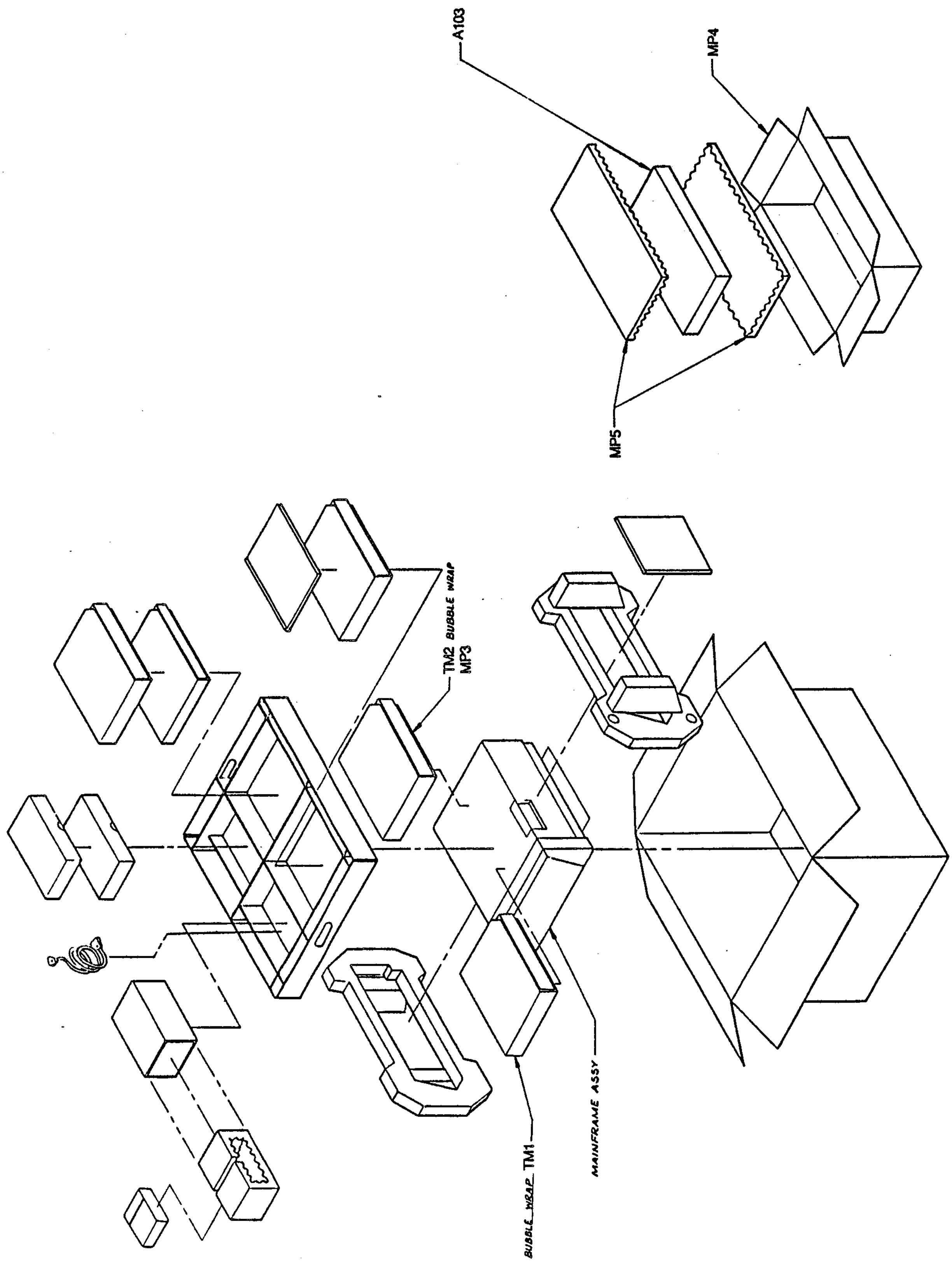

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Figure 5-15. Option -005 Programmer's Station, Color

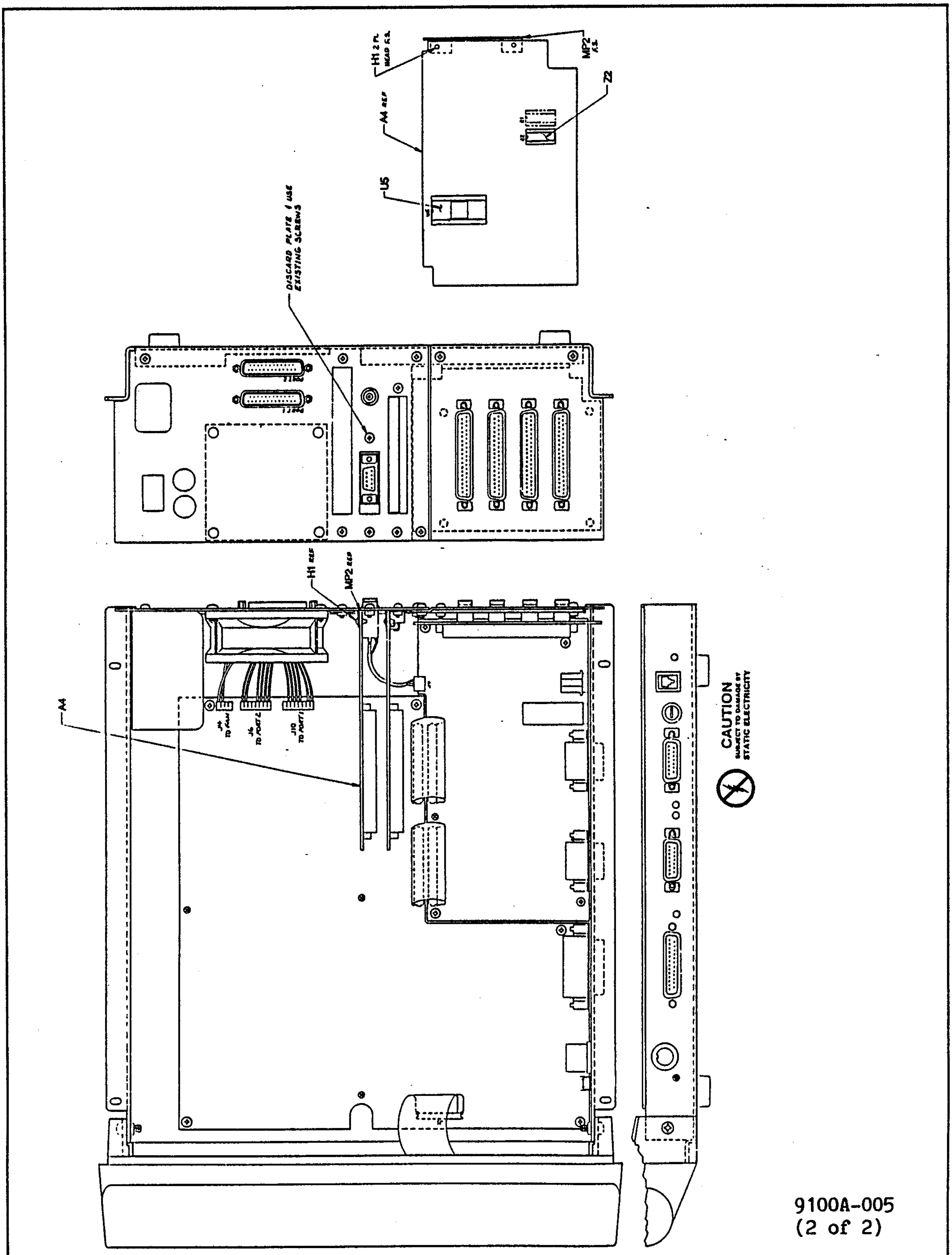

Figure 5-15. Option -005 Programmer's Station, Color (cont.)

Table 5-23. Option -009 Video, Monochrome
(See Figure 5-17.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	NOTE -E-
A	4	*	VIDEO CONTROLLER PCA	768762	89536	768762	1		
A	19		MONOCHROME MONITOR	826362	89536	826362	1		
H	1		RIVET,POP,DOME,AL,0.125X0.316	423616	COMMERCIAL		2		
MP	2		VIDEO CONNECTOR BRACKET	768648	89536	768648	1		
MP	3		NAMEPLATE, SERIAL -REAR PANEL-	472795	89536	472795	1		
U	5	*	PROGRAMMED 27128-150	818195	89536	818195	1		
W	1		CABLE, MONITOR	787903	89536	787903	1		
Z	1		JUMPER,DIP,0.300CTR,PROGRAM,16 POS	783183	51167	16-680-191T	1		

An * in 'S' column indicates a static-sensitive part.

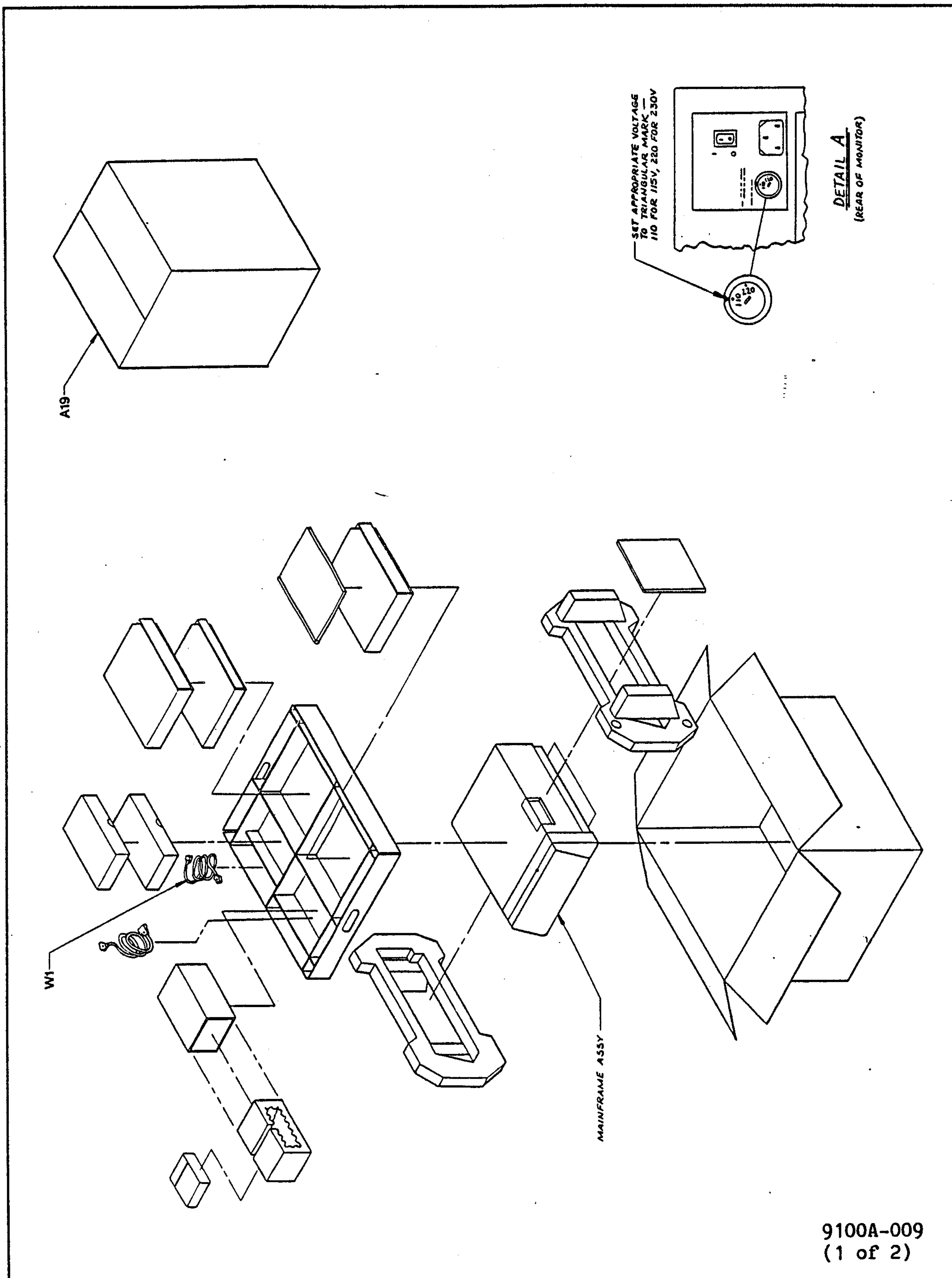

Figure 5-17. Option -009 Video, Monochrome

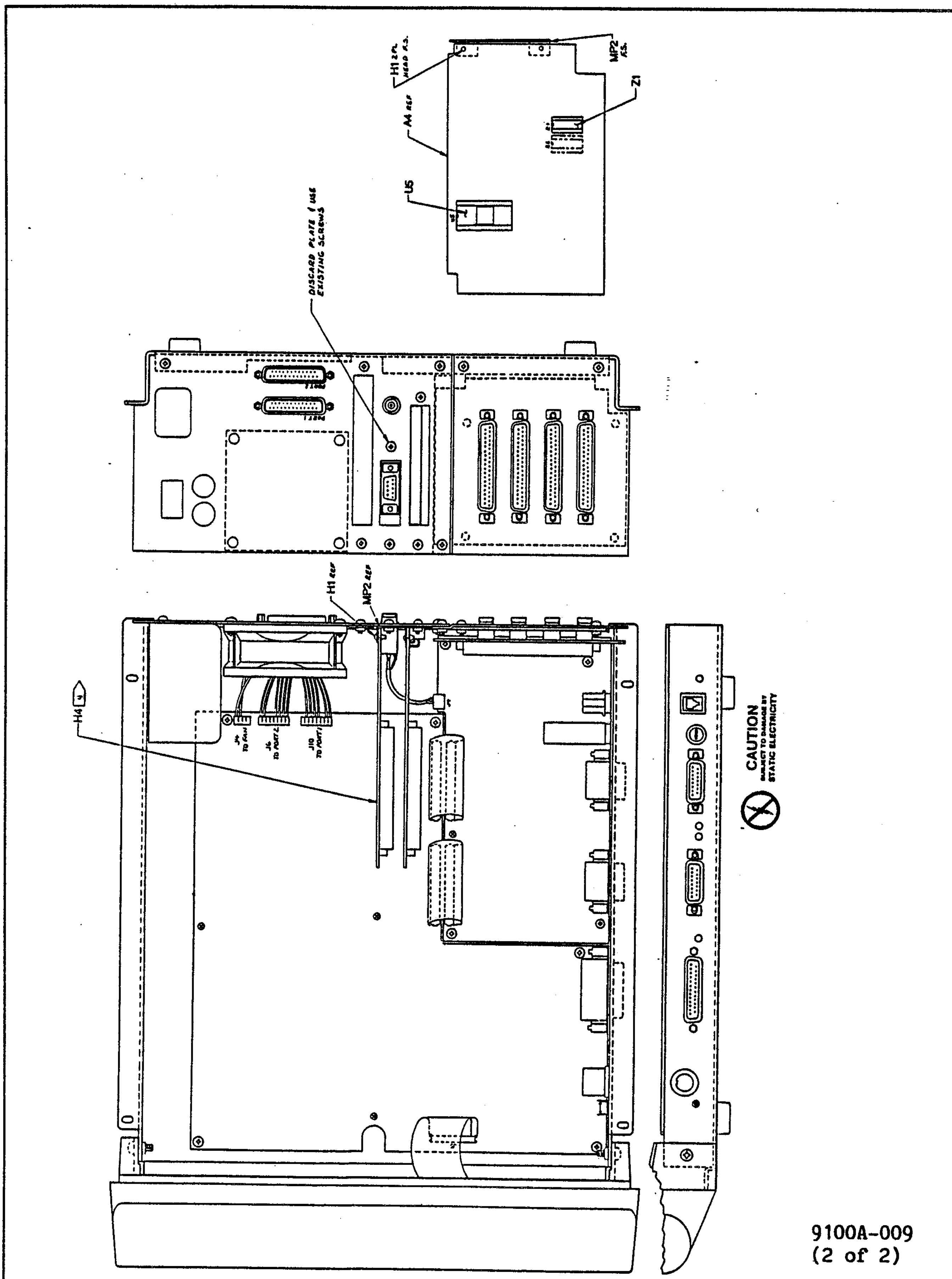

Figure 5-17. Option -009 Video, Monochrome (cont.)

Table 5-24. Option -011 Video, Color
(See Figure 5-18.)

REFERENCE DESIGNATOR -A>-NUMERICS---->		S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE	TOT QTY	R S -Q	N O T -E-
A	4	*	VIDEO CONTROLLER PCA	768762	89536	768762	1		
H	1		RIVET,POP,DOME,AL,0.125X0.316	423616	COMMERCIAL		2		
MP	2		VIDEO CONNECTOR BRACKET	768648	89536	768646	1		
U	5	*	PROGRAMMED 27128-150	818195	89536	818195	1		
Z	2		JUMPER,DIP,0.300CTR,PROGRAM,16 POS	783183	51167	16-680-191T	1		

An * in 'S' column indicates a static-sensitive part.

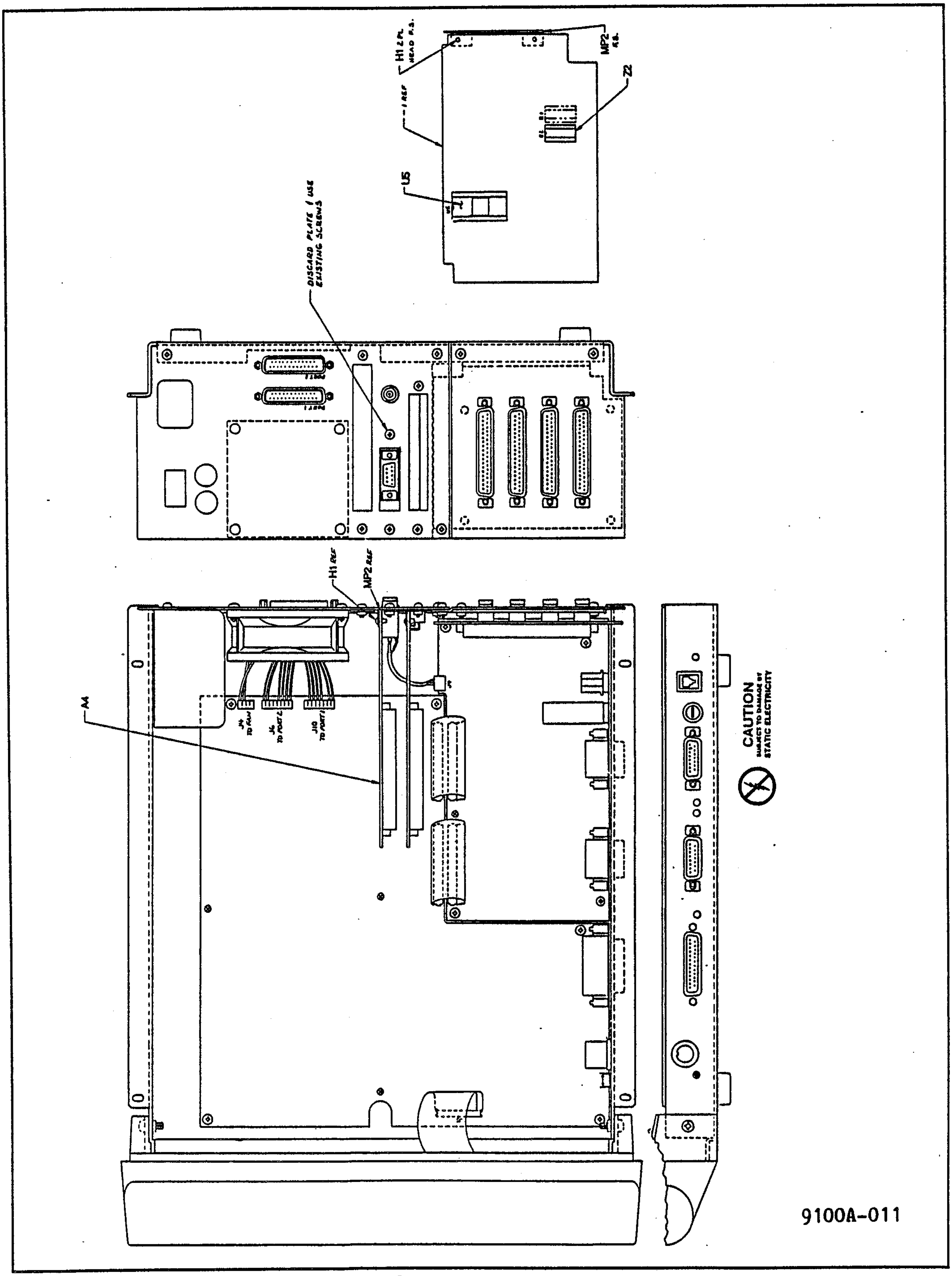

Figure 5-18. Option -011 Video, Color

Table 5-25. Option -013 Programmer's Keyboard

REFERENCE DESIGNATOR -A>-NUMERICS---->		S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE	TOT QTY	R S -Q	N O T -E-
MP	1	*	ENCODER ASSEMBLY	783092	76854	4-6474-003	1		
MP	2	*	MEMBRANE SWITCH ASSEMBLY	783076	76854	5-64955-100	1		
MP	3		KEYCAP SET	783118	76854	5-68585-115	1		
MP	4		TOP CASE	783035	76854	3-8779-524	1		
MP	5		BASE	783084	76854	3-3314-762	1		
W	1		CABLE	783043	76854	4-6378-008	1		

An * in 'S' column indicates a static-sensitive part.

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Section 3. Theory of Operation (cont.)

Section 3. Theory of Operation (cont.)

Section 4. Maintenance

Section 4. Maintenance (cont.)

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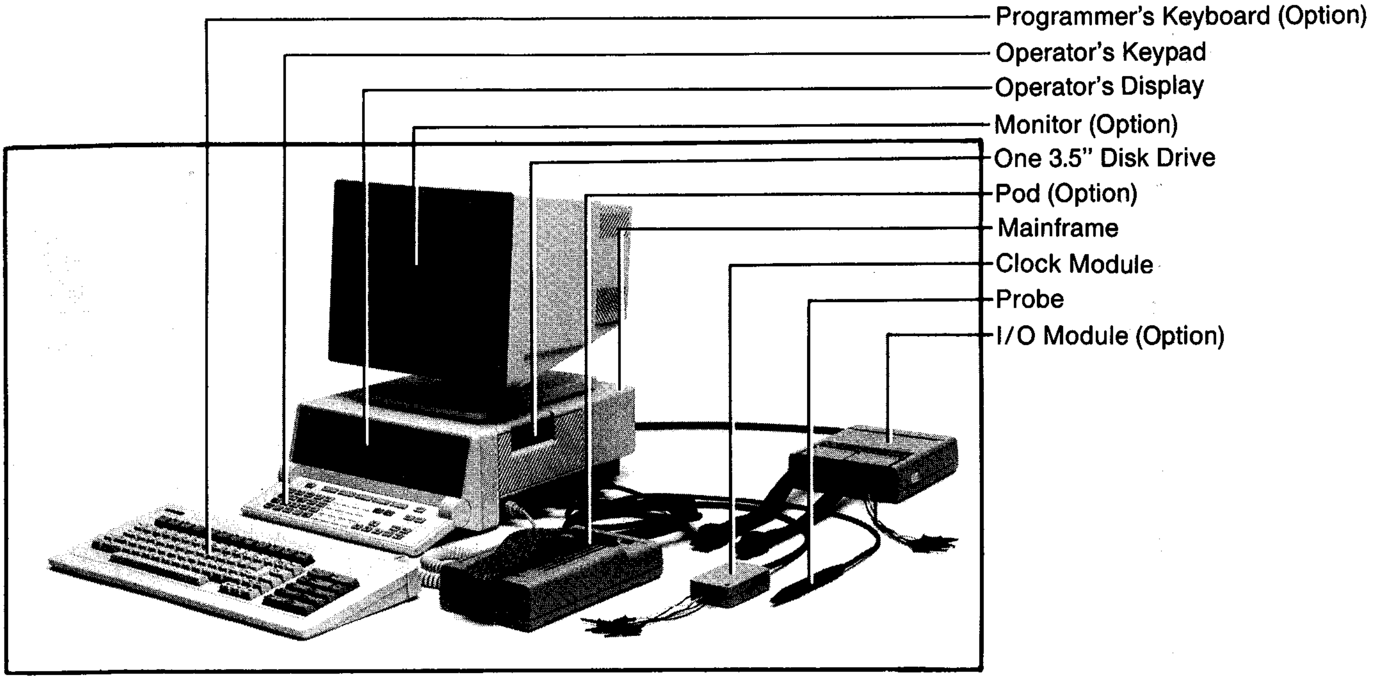
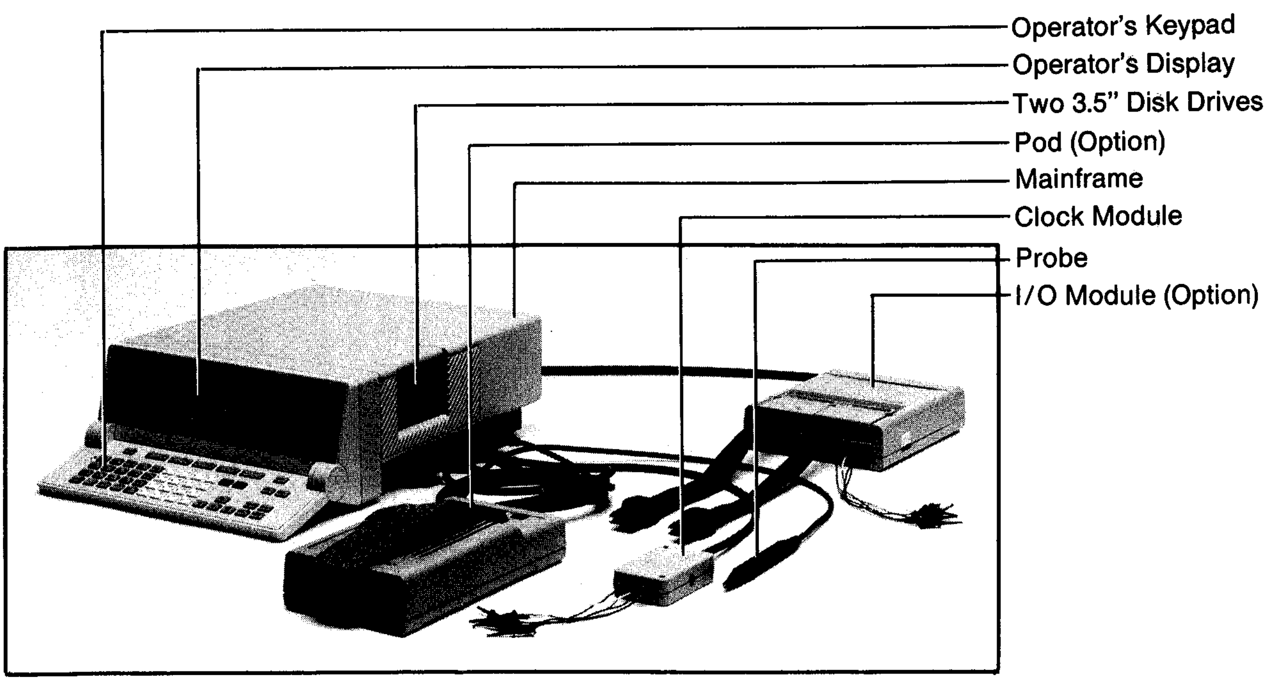


9100A System



9105A System

Section 2
General Information

CONTENTS

DESCRIPTION

Information brought together in this section serves as a one-source reference for servicing the 9100A, 9105A, and related options. The 9100A/9105A instruments are fully described elsewhere in the manual set. Specifically, Getting Started and the Technical User's Manual can be consulted for hardware and capabilities information.

Power Requirements

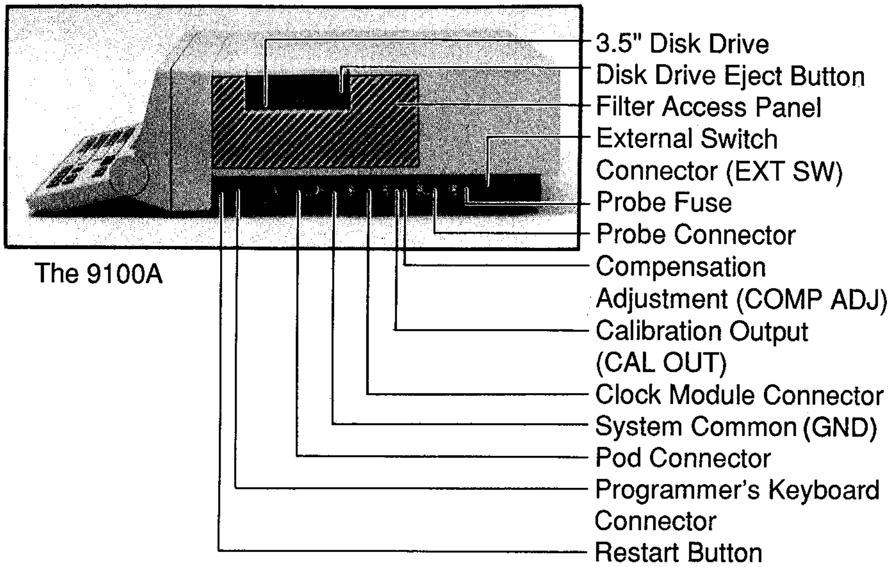
Power requirements for the 9100A/9105A are presented in Table 2-1. The 9100A/9105A mainframe uses a maximum of 150 watts. In addition, the Monitor uses 50 watts maximum.

Table 2-1. Power Requirements

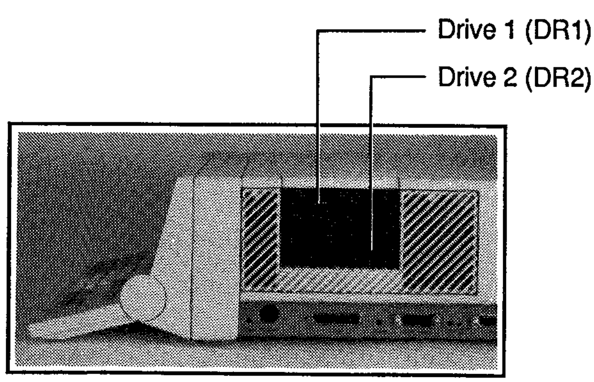
VOLTAGE SWITCH SETTING	LINE VOLTAGE RANGE	FREQUENCY	FUSE
110V	90-130V ac	47 to 440 Hz	2A Slow Blow
220V	180-264V ac	47 to 63 Hz	1A Slow Blow

External Connections

Servicing the 9100A/9105A may require disconnection of system components. For ease of reassembly, full connection information is presented here. Figure 2-1 identifies connections and other features found along the right side of either instrument. Figure 2-2 shows rear panel features.



The 9100A



The 9105A, showing its different disk drive arrangement.

Figure 2-1. Side Features

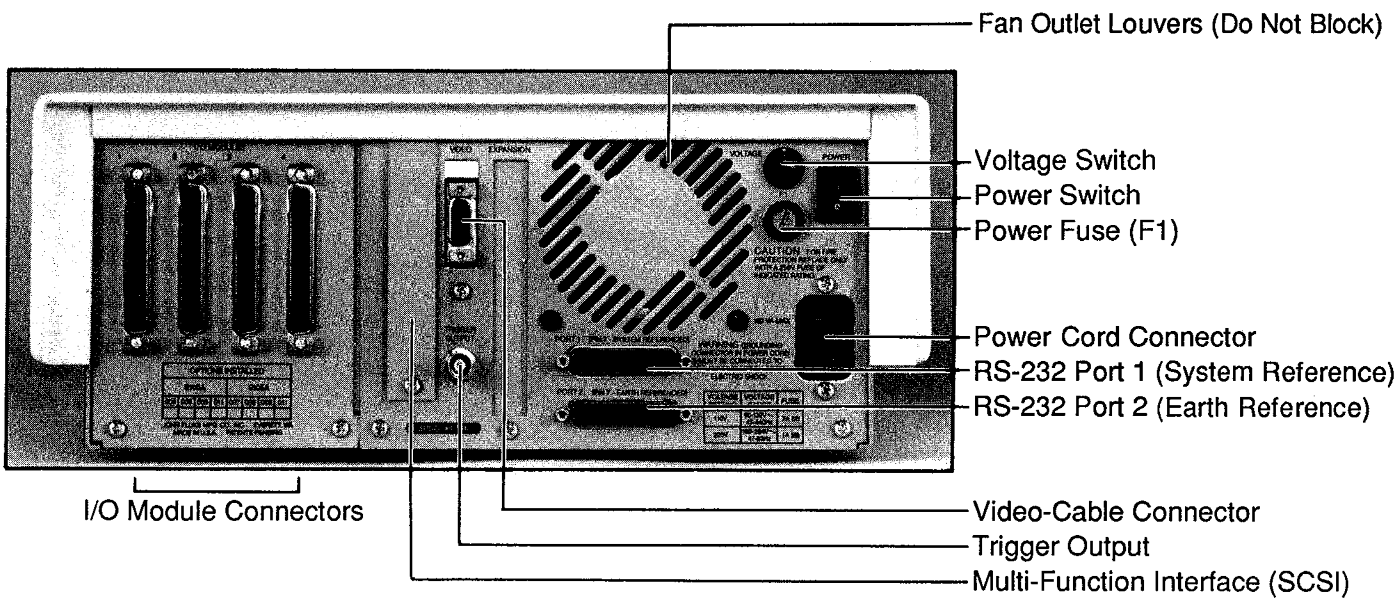


Figure 2-2. Rear Panel Features

SYSTEM COMPONENTS

Theories of operation, maintenance instructions, and schematic diagrams in this manual cover all 9100A/9105A system components. Refer to other manuals in the 9100A/9105A manual set for complete descriptions and usage instructions. The Getting Started manual provides a good overview of system components. These are listed and categorized in the following paragraphs, with references to coverage within this manual.

9100A Systems

The 9100A Digital Test System constitutes the mainframe, probe, and clock module documented in this manual.

The 9100/SYS Digital Test Programming System includes 9100A Test System components, along with the 9100A-003 Parallel I/O Module, the 9100A-004 Programmer's Station, and the Y9100A-DCS DIP Clip Set accessory described in this manual.

9105A System

The 9105A Test Station includes the mainframe, probe, and clock module described in this manual.

Options

The 9100A-004 Programmer's Station applies to the 9100A only. Its monochrome monitor, monochrome video controller, and keyboard are documented in this manual.

The 9100A-005 Programmer's Station is also available for the 9100A only and provides the color video controller and keyboard described in this manual.

Option 9105A-008, Real-Time Clock and Option 9105A-007, 512K Expansion Memory, are available for the 9105A only and are documented in this manual.

Finally, the following options are available for either the 9100A or the 9105A and are separately documented in this manual:

- Parallel I/O Module, Option 9100A-003, includes a Y9100A-20L Flying Lead Module and a Calibration Module.
- Video (Monochrome), Option 9100A-009, includes a Video Controller and a Monochrome Monitor.
- Video Controller (Color), Option 9100A-011.
- Keyboard, Option 9100A-013

Accessories

All hardware accessories for the 9100A/9105A are documented in this manual. These include:

- o Half-Width Clip Modules, Accessories Y9100A-14D, -14S, -16D, -16S, -18D, 20D, 20S, -24D, and 24S.
- o Full-Width Clip Modules, Accessories Y9100A-28D, -28S, and -40D.
- o Y9100A-DCS DIP Clip Set, including Y9100A-14D, -16D, -18D, -20D, -24D, -28D, and -40D.
- o Flying Lead Module, Accessory Y9100A-20L

Interface Pods

Interface pods can be used with a wide range of microprocessors. Each pod is documented in its own manual, none of which are included with 9100A/9105A Manual Set. No pod information is provided in this service manual.

REQUIRED TEST EQUIPMENT

Tools and test equipment required in servicing the 9100A or 9105A are listed in Table 2-2.

SHIPPING INFORMATION

When you receive the instrument, inspect the shipping container for any possible shipping damage. Special instructions for inspection and claims are included on the shipping container.

If it is necessary to reship the instrument, use the original container. If the original container is not available, a new one can be obtained from the John Fluke Manufacturing Co., Inc. upon request.

SERVICE INFORMATION

The 9100A/9105A is warranted for a period of 90 days upon delivery to the original purchaser. The warranty is located in the front of this manual, following the title page.

Factory calibration and service for each Fluke product is available at various locations worldwide. A complete list of these service centers is given in the appendices of this manual. If requested, an estimate will be provided to the customer before any work is begun on an instrument whose warranty period has expired.

Maintenance plans are available to maintain the 9100A/9105A at your site, to supplement the normal warranty period, or to do both. For specific information, contact your nearest Fluke Technical Service Center or Sales Representative.

Table 2-2. Required Tools and Test Equipment

EQUIPMENT REQUIRED FOR GENERAL SERVICING

EQUIPMENT	RECOMMENDED MODEL	FUNCTION/COMMENTS
Digital Multimeter	Fluke Model 77	
Oscilloscope	Philips Model PM 3065 (or equivalent)	
Adjustment Tool	P/N 800540	
Flat Blade Screwdriver		1/8-inch (3 mm) blade
Flat Blade Screwdriver		1/4-inch (6 mm) blade
Phillips Screwdriver		#2, blade 4 inches (10 cm) or longer
Hex Driver		3/16-inch (5 mm)
Hex Driver		5/16-inch (8 mm)
Wrench		3/16-inch (5 mm) or adjustable

REQUIRED EQUIPMENT FOR COMPONENT LEVEL REPAIR

EQUIPMENT	RECOMMENDED MODEL	FUNCTION/COMMENTS
9100A Service Kit	P/N 818948	
Digital Test Station, with I/O Module	Fluke Model 9105A (or 9100A) with 9100A-003 Option	Runs programs supplied with Service Kit
68000 Interface Pod	Fluke Model 9000A-68000	Used with Service Kit
Surface Mount Repair tools		See Table 4-6

Table 2-2. Required Tools and Test Equipment (cont.)

REQUIRED EQUIPMENT FOR MONOCHROME MONITOR MAINTENANCE

EQUIPMENT	RECOMMENDED MODEL	FUNCTION/COMMENTS
Hex Adjustment Tool	P/N 572321	Horizontal Size/Linearity
Alignment Template	P/N 777144	Use with Monitor Pattern Program
Long-Nose Pliers		
Flat-Blade Screwdriver		1/4-inch (6 mm) blade, plastic handle with blade at least 5 inches (12.5 cm) long.
Phillips Screwdriver		#2, plastic handle with blade at least 3 inches (7.5 cm) long.
Phillips Screwdriver		#2, non-magnetic tip blade, plastic handle, with blade at least 12 inches (30 cm) long, for crt replacement.
Torque Hex Driver		3/16-inch (5 mm).
Soft Pad (foam or quilted)		Approximately 8 x 10 inches (20 x 25 cm).
1 Megohm, 1W Resistor	P/N 109793	To discharge crt anode.
Clip Leads (2)		For connecting resistor to chassis and screwdriver shaft.
Safety Gloves		Mid-forearm length, soft leather.
Full Face Shield (preferred) or Safety Goggles		
Lab Smock with Zipper		Plastic zipper. Metal parts should not come in contact with the crt.

SPECIFICATIONS

Specifications for the 9100A/9105A are presented in Table 2-3.

Table 2-3. Specifications

ELECTRICAL SPECIFICATIONS

Probe

Input Threshold

Logic Level	TTL Voltage	CMOS Voltage	RS-232 Voltage
1	2.6 to 5.0V	3.7 to 5.0V	3.2 to 30V
1 or X	2.2 to 2.6V	3.3 to 3.7V	2.8 to 3.2V
X	1.0 to 2.2V	1.2 to 3.3V	-2.8 to 2.8V
X or 0	0.6 to 1.0V	0.8 to 1.2V	-3.2 to -2.8V
0	0.0 to 0.6V	0.0 to 0.8V	-30 to -3.2V

Input Impedance — 70 kilohm shunted by less than 33 pF

Data Timing for Synchronous Measurements

Maximum frequency	40 MHz
Minimum pulse width	
High or low	12.5 ns
3-state	20.0 ns
Setup times	
Data to Clock	5 ns
Start, Stop, or Enable to Clock	10 ns
Hold time	
Clock to Enable	10 ns
Clock to Start or Stop	0 ns

Data Timing for Asynchronous Measurements

Maximum frequency	40 MHz
Minimum pulse width	
High or low	12.5 ns
Invalid (X)	
TTL or CMOS	100 ns ±20 ns
RS-232	2000 ns ±400 ns

Table 2-3. Specifications (cont)

Transition Counting	
Maximum frequency	at least 40 MHz
Maximum count	16777215 (+overflow)
Maximum stop count	65535 clocks
Frequency Measurement	
Maximum frequency	at least 40 MHz
Resolution	20 Hz
Accuracy	±250 ppm ±20 Hz
Output Pulser	
High	>3.5V @200 mA for less than 10 us @ 1% duty cycle >4.0V @ 4 mA continuously
Low	<0.8V @ 200 mA for less than 10 us @ 1% duty cycle <0.4V @ 5 mA continuously
Clock Module	
Input Thresholds (all lines)	1.6V ±0.2V
Input Impedance	50 kilohm shunted by less than 10 pF
Clock, Start, Stop, and Enable Input Speed	
Maximum repetition rate	40 MHz
Minimum pulse width	12.5 ns

Table 2-3. Specifications (cont)

RS-232 Interfaces

One connector isolated (system-referenced), the other connector non-isolated (earth-referenced).

Baud rates	110, 134, 300, 600, 1200, 1800, 2400, 4800, 9600, 19200
Parity	Odd, even, or none
Data bits	5, 6, 7, or 8
Stop bits	1, 1.5, or 2
XON/XOFF (Ctrl-S/Ctrl-Q)	Disable/Enable
Clear-to-Send	Disable/Enable
New line	Carriage Return and Line Feed (CRLF) or Carriage Return (CR)

I/O Module

Data Output

Current (>10 ms)	$\pm$200 mA $\pm$10%
Current (<10 ms)	$\pm$2A $\pm$10%
Pattern rate (one module driven)	Approximately 35 kHz
Pattern depth (one module driven during 10 ms high current pattern drive mode)	256 patterns
Maximum current (at Vout>=2V) (per pin, driving high)	275 mA
Maximum current (at Vout<=0.8V) (per pin, driving low)	150 mA

Table 2-3. Specifications (cont)

Input Thresholds

Logic Level	TTL Voltages	CMOS Voltages
1	2.6 to 5.0V	3.4 to 5.0V
1 or X	2.1 to 2.6V	2.9 to 3.4V
X	1.0 to 2.1V	1.2 to 2.9V
X or 0	0.6 to 1.0V	0.8 to 1.2V
0	0.0 to 0.6V	0.0 to 0.8V

Input Impedance	50 kilohm minimum, shunted by less than 80 pF
Clock, Start, Stop, and Enable Inputs	
Logic Thresholds	
Low	0.8V maximum
High	2.0V minimum
Input Current	±1 uA
Input/Output Overvoltage Protection	
	±15V for one minute maximum, any pin, one at a time
Transition Counting	
Maximum frequency	at least 10 MHz
Maximum count (transition mode)	8388607 counts (+overflow)
Frequency accuracy (frequency mode)	±250 ppm ±2 Hz
Stop Counter	
Maximum frequency	10 MHz
Maximum count	65535 clocks
Clock	
Maximum frequency	10 MHz
Minimum pulse width	50 ns

Table 2-3. Specifications (cont)

Data Timing for Synchronous Measurements	
Maximum frequency of clock	10 MHz
Maximum frequency of data	5 MHz
Data setup time	30 ns
Data hold time	30 ns
Minimum pulse width (data)	75 ns
Minimum pulse width (Start, Stop, Enable, Clock)	50 ns
Start edge setup time (before clock edge, for clock edge to be recognized)	0 ns
Stop edge hold time (after clock edge, for clock edge to be recognized)	10 ns
Enable setup time (before clock edge, for clock edge to be recognized)	0 ns
Enable hold time (after clock edge, for clock edge to be recognized)	10 ns
Data Timing for Asynchronous Measurements	
Maximum frequency	10 MHz
Minimum pulse width (high or low)	50 ns
Minimum pulse width (3-state)	150 ns
Data Compare Equal (DCE)	
Minimum pulse width (Data and Enable)	75 ns

Table 2-3. Specifications (cont)

GENERAL SPECIFICATIONS

Line Voltage	90 to 132V ac, 47 to 440 Hz 180 to 264V ac, 47 to 63 Hz
Power Consumption	
Mainframe	150W maximum
Monitor	50W maximum

Safety

Designed to meet ANSI/UL 478, IEC 348, IEC 435, and CSA 556B standards.

PHYSICAL SPECIFICATIONS

Operating Temperature

5° to 27°C, 95% RH maximum (noncondensing)

27° to 40°C, RH decreasing linearly from 95% to 50% (noncondensing)

Programmer's Station

24-line by 80-column crt monitor with video controller installed in mainframe. 87-key keyboard with separate cursor control, and hardkey and softkey function keys.

Storage/Shipping Temperature

-20° to 60°C, 8% to 80% RH (noncondensing). Micro-floppy media limited from 5° to 60°C, 8% to 80% RH (noncondensing).

Size	
Mainframe	14.0 x 34.3 x 50.8 cm (H x W x D) (5.5 x 13.5 x 20.0 in)
Monitor	30.5 x 33.5 x 33.0 cm (H x W x D) (12.0 x 13.2 x 13.0 in)
ASCII Keyboard	5.1 x 21.2 x 47.2 cm (H x W x D) (2.0 x 8.3 x 18.6)
Weight	
Mainframe	8.3 kg (18.2 lb)
Monitor	11.1 kg (24.5 lb)
ASCII Keyboard	1.6 kg (3.5 lb)

CONTENTS

OVERVIEW

This overview of the Fluke 9100A/9105A explains the general relationships of the unit blocks contained in the 9100A Block Diagram, Figure 3-1, and the 9105A Block Diagram, Figure 3-2. Wherever a block performs the same function for both instruments, an identical block name is used for ease of reference later in this section.

Main PCA

The Main Printed Circuit Assembly contains the following functional blocks:

- 68000 Microprocessor
- Read/Write (RAM) Memory
- Read-Only ROM Memory,
- Floppy Disk Drive Controller
- Pod Interface
- Power Supplies for the RS-232 ports, operator's display, and video.

The PCA contains the interfaces for expansion cards, serial ports, and the keyboards. There are connections for the Floppy Disk Drive, the Monitor, the Hard Disk Controller, the Probe I/O Module Interface, the microprocessor Pod, and the switching Power Supply.

RS-232 Ports

Two RS-232-C serial ports are available on the 9100A. These ports allow data transfer to and from the tester. One is system-referenced (isolated from earth) and is used with the UUT. The other is a non-isolated port and is used for connection to another tester, computer, or printer. The Serial Port connectors are located at the rear of the Chassis.

Micro Floppy Disk System

The Floppy Disk System uses 3.5-inch double-sided, double-density disks. A disk has a formatted capacity of 640K bytes. The 9100A uses one disk drive, and the 9105A uses two disk drives. The floppy drive is connected through J14 on the Main PCA.

Hard Disk System

The 9100A contains a 20M byte, 3.5-inch Hard Disk to store the operating software, user programs, and data. The Hard Disk interfaces to the Hard Disk Controller via the ST412 interface standard. The Hard Disk Controller interfaces to the Multi-Function Interface (MFI) PCA, which implements the SCSI interface standard. The MFI PCA, which plugs into the Main PCA at J6, also includes the battery-powered back-up clock for the 9100A.

Power Supply

The Power Supply for the 9100A/9105A is an OEM (original equipment manufacturer) switching power supply. Input voltage is switchable for either 90 to 132V ac or 180 to 264V ac operation. This functional block supplies one +5V, one -5V, and two +12V outputs to the system.

Operator's Display

The Operator's Display is a vacuum-fluorescent display, 254 pixels wide by 26 pixels deep, allowing for 42 characters per line. The Display is located above the Operator's Keypad on the Main Chassis. The Display Interface PCA is connected to J11 on the Main PCA.

Operator's Keypad

The Operator Keypad is a part of the Main Chassis unit that, when folded down, faces the operator. It is connected to J2 on the Display Interface PCA. It contains all of the keys needed by the operator to run pre-programmed tests used in the immediate troubleshooting mode.

Probe/Pulser

The Probe is a single-point, hand-held instrument that can measure signals up to 40 MHz. The Probe also acts as a pulser. The Probe is useful for portions of the board that cannot be accessed with the I/O Module or Pod. The Probe plugs into a connector on the side of the Chassis and is wired to J1 on the Probe I/O PCA.

Clock Module

The Clock Module is an external unit connected to the Main Chassis through J3 on the Probe I/O PCA. The Clock Module provides connections to external clock signals for troubleshooting signals asynchronous to the UUT microprocessor.

Monitor

The Monitor displays programming information entered from the Programmer's Keyboard. The Monitor can also assume Operator Keypad functions by displaying procedural information. The Monitor is connected to a Video Controller Card, which is plugged into the Main PCA.

Programmer's Keyboard

The Programmer's Keyboard is used for program development. It is also available as an option for data input to user programs. The Keyboard is connected to J10 on the Main PCA.

I/O Module

The I/O Module is an external unit used for data stimulus and response of up to 40 channels at one time. An assortment of clip modules is available for interface to the UUT. The 9100A can accommodate four I/O Modules at once, allowing for testing of 160 pins at a time. The 9100A has the capability to take CRCs (cyclic redundancy checks), measure frequency, take event counts, record logic levels, and drive output patterns on each pin. The I/O Modules plug into the I/O Connector PCA, which plugs into the Probe I/O PCA.

MAIN PCA (MC68000 MICROPROCESSOR)

Overview

The 9100A/9105A uses an MC68000 main processor(U32). The 16-bit MC68000 contains 17 32-bit registers, a 16-bit status register, and a 32-bit program counter. Of the 17 registers, 8 are data registers, 7 are address registers, and 2 registers are used as stack pointers. The MC68000 (U32) is located on the Main PCA of the mainframe.

The 68000 theory of operation covers the following:

- Signal and pin description
- Address/data operation
- Modes of processing including interrupts
- Asynchronous/synchronous execution
- Reset signal description and generation

Signal and Pin Description

The following paragraphs describe the meaning of each signal produced by the 68000 and show how these signals are organized per function. A table helps to explain the mnemonics used on the schematic, and indicates whether the signal is an input or an output. Figure 3-3 shows the 68000 pin configuration for the 68-pin plastic leaded chip carrier (PLCC) package.

SIGNAL DESCRIPTION

Table 3-1 describes the 68000 microprocessor signals.

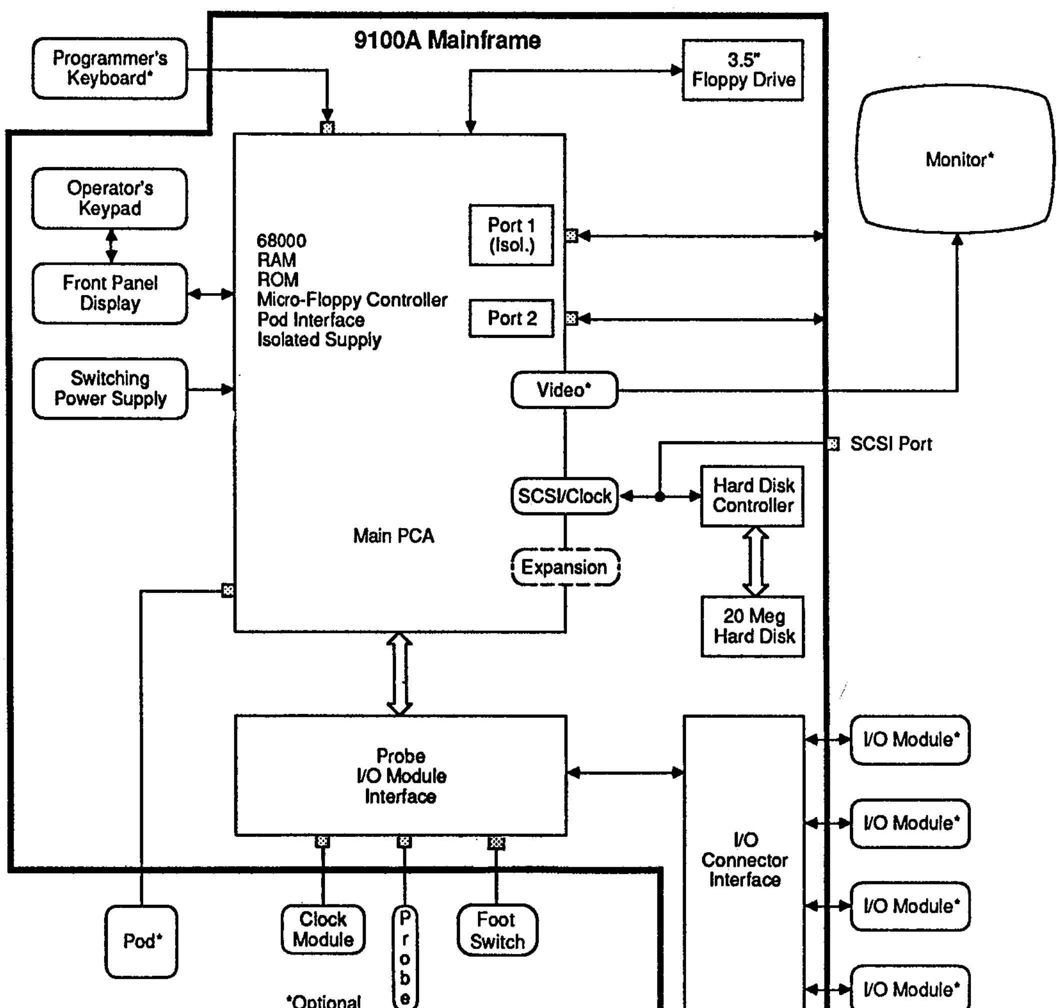


Figure 3-1. 9100A Block Diagram

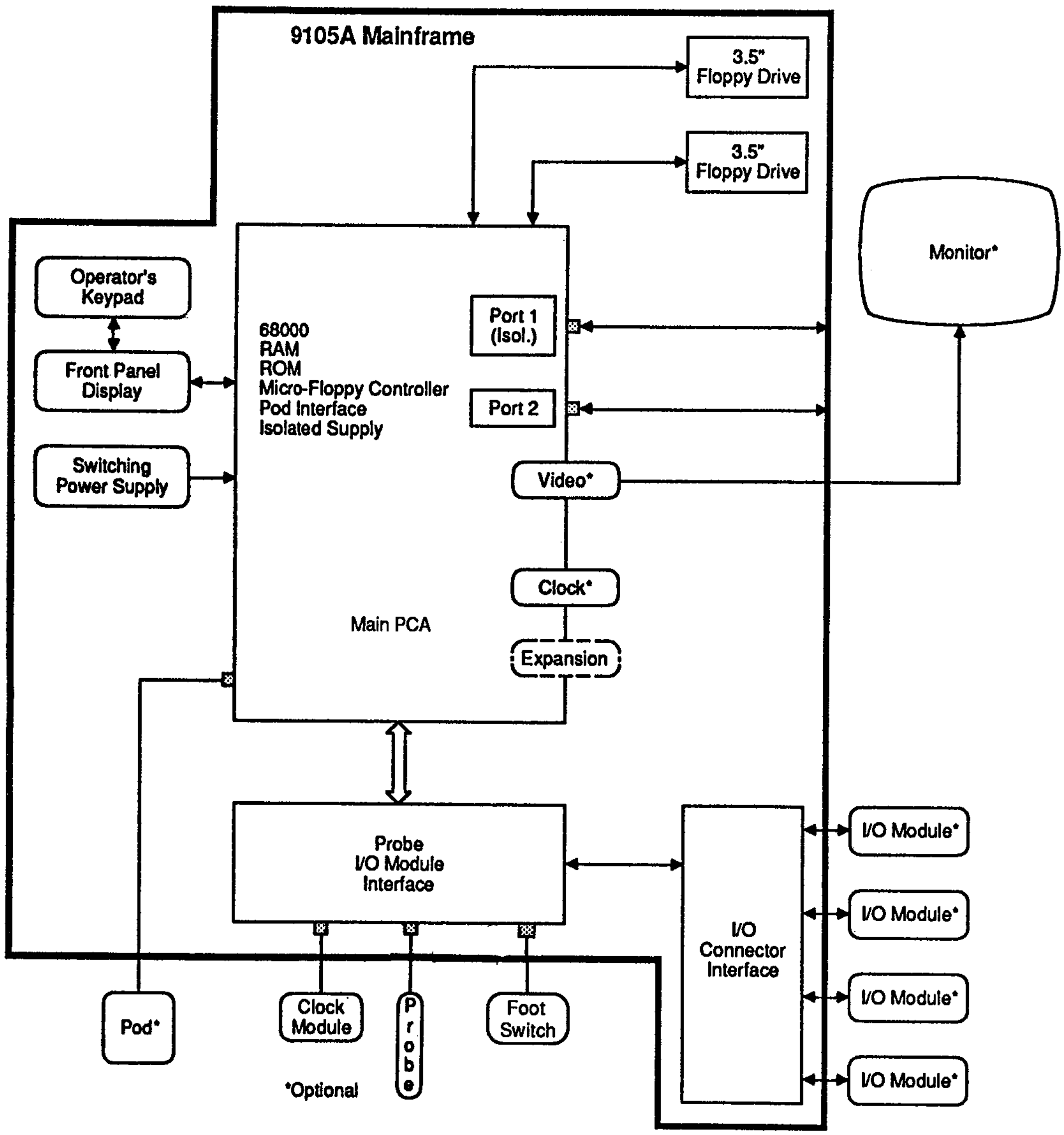


Figure 3-2. 9105A Block Diagram

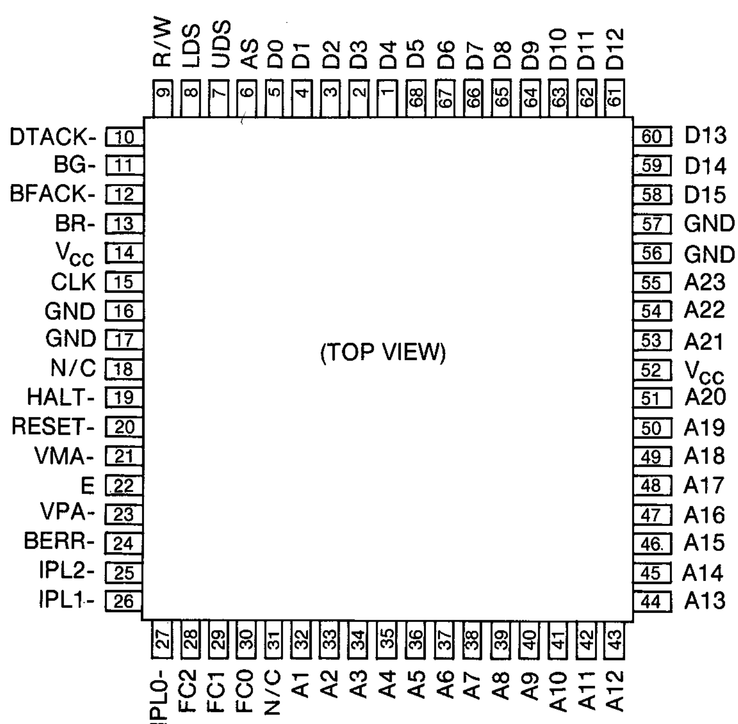


Figure 3-3. 68000 Pin Assignments

Table 3-1. Signal Descriptions

SIGNAL NAME	DESCRIPTION
A1 through A23	Address Bus: 23 tri-state output lines, providing the bus address for all processor operations except interrupt vector fetch cycles. During interrupt acknowledge cycles, address lines A1, A2, and A3 indicate the interrupt level that is being serviced, while address lines A4 through A23 are set high. Address line A0 is used internally by the processor for byte operations.
D0 through D15	Data Bus: 16-bit, bidirectional, tri-state data bus.
FC0 through FC2	Function Code lines: tri-state outputs that indicate the state (user or supervisor) and type (program or data) of the current bus cycle. They are also used to indicate an acknowledge cycle as follows:

FC2	FC1	FC0	CYCLE TYPE
0	0	0	(undefined, reserved)
0	0	1	User data
0	1	0	User program
0	1	1	(undefined, reserved)
1	0	0	(undefined, reserved)
1	0	1	Supervisor data
1	1	0	Supervisor program
1	1	1	Interrupt acknowledge

SIGNAL NAME	DESCRIPTION
AS-	Address Strobe-: a tri-state output that indicates that valid data is present on the address and function code lines and that a bus cycle is in progress.
R/W-	Read/Write-: an output that indicates the direction that data is to be transferred on the data bus.
UDS-, LDS-	Upper Data Strobe- and Lower Data Strobe-: outputs that indicate whether upper, lower, or both bytes are to be used for a data bus transaction. During an interrupt acknowledge cycle, both UDS- and LDS- are asserted, but only the lower byte is read.
DTACK-	Data Transfer Acknowledge-: an input that indicates to the processor that the bus data transfer will be completed at the end of the current processor clock cycle. It is used to terminate the current bus cycle unless superseded by a bus error or a reset.
BR-	Bus Request-: an input that indicates to the processor that some other device is requesting control of the bus.

Table 3-1. Signal Descriptions (cont)

BG-	Bus Grant-: an output that indicates that the processor will relinquish control of the bus at the end of the current bus cycle.
BGACK-	Bus Grant Acknowledge-: an input that indicates that a device other than the processor has assumed bus control.
IPL0-, IPL1- IPL2-	Interrupt Priority Level-: inputs that indicate the encoded priority level of the interrupting device. Level 0 indicates no interrupt is pending, while level 7 is the highest priority interrupt.
BERR-	Bus Error Line: an input that indicates a problem with the current bus cycle. When BERR- is asserted with the HALT- line, the processor reruns the current bus cycle if the HALT- line is released first. If BERR- is asserted during reset vector acquisition, or for two consecutive bus cycles, the processor halts. If BERR- is asserted alone, it causes the processor to execute a non-maskable interrupt to the Bus Error Vector.
RESET-	Reset-: a bidirectional open collector line used to reset the state of the processor. It may also be used by the processor to reset the state of the external environment.
HALT-	Halt-: a bidirectional open collector line that is asserted when the processor stops due to an unrecoverable error sequence. This line can be pulled low during a bus cycle to stop the processor at the end of the cycle, to rerun the last bus cycle (when BERR- is low), or to reset the processor (when RESET- is low).
E	Enable: an output used to simulate a 6800-type processor clock for interface with 6800 family peripherals. This signal runs continuously and is derived by dividing the processor clock by ten. The duty cycle consists of six clock periods low and four clock periods high.
VPA-	Valid Peripheral Address: an input used to request 6800-type bus cycles. During interrupt acknowledge cycles, this line is used to request automatic vectoring.
VMA-	Valid Memory Address: an output used to enable 6800-type peripheral devices. VMA- indicates that the processor is synchronized to the Enable line and has placed a valid address on the address bus.
CLK	Clock: an input used to derive the clocks needed internally by the processor.

SIGNAL ORGANIZATION

The control signals of the 68000 can be grouped for the different functions. The function codes (FC0 through FC2) are the processor status signals that produce code sequences to indicate the mode (user or supervisor) and whether a data cycle or a program cycle is currently being executed. The code output is valid during an active address strobe (AS-). The code output is decoded externally to indicate interrupt acknowledge. The FC2 line is also used for address decode on the Multi-Function Interface PCA, the floppy controller chip, and the first 8K of RAM. This technique prevents user programs from accessing these areas.

The bus request (BR-), bus grant (BG-), and bus grant acknowledge (BGACK-) signals are used for bus arbitration control. These signals determine which component or peripheral controls the bus. The bus request input indicates that another device is requesting to become the bus master. The bus grant output then indicates to all other potential bus masters that the microprocessor will relinquish control at the end of this bus cycle. Once the other device has become the bus master, it returns the Bus Grant Acknowledge input to the microprocessor. These three bus arbitration control signals can be used by the Multi-Function Interface PCA to avoid bus contention.

Asynchronous bus control signals are Address Strobe (AS-), Read/Write (R/W-), Upper and Lower Data Strobes (UDS-, LDS-), and Data Transfer Acknowledge (DTACK-). The R/W- signal indicates the direction of data transfer on the data bus. When R/W- is high, data is being read from another functional block to the microprocessor. In the low state, data is being written to another functional block. The Upper and Lower Data Strobe signals are used in conjunction with the Read/Write signal to identify transfer of valid lower (D0 through D7) and/or upper (D8 through D15) data bytes. This data strobe control is defined in Table 3-2.

Table 3-2. Data Strobe Control

UDS-	LDS-	R/W-	UPPER D8-D15	LOWER D0-D7
High	High	-	none	none
Low	Low	Low	Write 8-15	Write 0-7
High	Low	Low	none	Write 0-7
Low	High	Low	Write 8-15	none
Low	Low	High	Read 8-15	Read 0-7
High	Low	High	none	Read 0-7
Low	High	High	Read 8-15	none

The Address Strobe (AS-) signifies that there is a valid address on the address bus. The Data Transfer Acknowledge (DTACK-) signal is an input signifying that data transfer is complete.

The System Control signals are Bus Error (BERR-), RESET-, and HALT-. The BERR- signal informs the microprocessor that there is a problem on the bus. The RESET- and HALT- signals reset or halt the 9100A/9105A system.

The 68000 uses three signal lines for peripheral control. The Enable (E), Valid Peripheral Address (VPA-), and Valid Memory Address (VMA-) allows for interfacing synchronous peripheral devices with the asynchronous 68000. The VPA- mode is not used in the 9100A/9105A system except for tests using the expansion connector on the Main PCA.

Address/Data Bus Operation

The address bus and the data bus are covered separately in the following discussion. For the address bus, size, contents, address ranges of the entire 9100A/9105A system are included. For the data bus, size and use are discussed.

ADDRESS BUS

The 23-bit address bus (A1 through A23) is used to access other functional blocks throughout the 9100A/9105A. If an interrupt occurs, address lines A1, A2, and A3 provide information about the type of interrupt, and the remaining lines are held high.

Table 3-3 shows ranges of memory available for various functional blocks. Actual addresses used within these ranges are defined under the appropriate functional block descriptions.

DATA BUS

The 16-bit data bus (D0 through D15) provides for bidirectional exchange of data between the microprocessor and an addressed functional block. Data lines D0 through D7 supply the vector number to the processor during an interrupt acknowledge cycle.

Bus Operation During Data Transfer

Three different types of cycles occur during data transfer: read, write, and read-modify-write. The following paragraphs explain the sequence of events during these cycles.

Table 3-3. Address Ranges

HEX ADDRESS	USE
000000 - 07FFFF	ROM
080000 - 08FFFF	Floppy Control *
090000 - 093FFF	DTIO #1: Keypad/Display, RS-232 Port #1 DTIO #2: ASCII Keyboard, RS-232 Port #2
094000 - 097FFF	Interrupt Vector (Read)
098000 - 09BFFF	Parity Error Latch (Read)
09C000 - 09FFFF	Pod Interface
0A0000 - 0AFFFF	Expansion Card Slot
0B0000 - 0BFFFF	Multi-Function Interface Card Slot
0C0000 - 0CFFFF	Logic Probe Circuitry
0D0000 - 0DFFFF	I/O Modules
0E0000 - 0EFFFF	Video RAM
0F0000 - 0FFFFF	Video Controller Chip
100000 - BFFFFF	unassigned
C00000 - FFFFFF	RAM **

* Supervisor Mode only
** C00000 - C01FFF accessible in Supervisor Mode only

THE READ CYCLE

The read cycle involves transmitting bytes of data from a peripheral or from a memory space to the 68000 processor. If a word is read, both the upper data strobe and lower data strobe are active. In the case of a byte operation, an internal A0 bit determines which byte to be read. The 68000 issues the required data strobe for that byte. When the lower data strobe (D00 through D07) is issued, the A0 bit equals 1; when the upper data strobe (D08 through D15) is issued, A0 equals 0.

THE WRITE CYCLE

The write cycle process involves the 68000 sending bytes of data to a peripheral or a memory location. As in the read cycle, the processor uses an internal A0 bit to determine if the high or low byte is written to, and the processor sends the required strobe signal. Both data strobes are active during a word write cycle.

THE READ-MODIFY-WRITE CYCLE

During the read-modify-write cycle, the 68000 performs a read, modifies the data internally, and writes the data to the original address. This cycle is used to let multiple processors communicate, and the address strobe is active throughout the cycle.

Bus Arbitration

The bus arbitration process is required to switch bus control from the 68000 to another device. First, the device sends a Bus Request Signal (BR-) to the microprocessor. The 68000 sends back a Bus Grant (BG-) signal at the end of the current bus cycle. To protect against noise interfering with bus arbitration, the microprocessor continues to process instructions when the BR- signal goes inactive and a BGACK- is not received. After receiving a BR- signal, the 68000 issues a BG- signal and an Address Strobe (AS-). The AS- signal indicates that a bus cycle is in progress. The BG- and AS- signals are not issued at the same moment; the BG- signal is delayed until the AS- signal is issued. When the device requesting the bus receives a BG-, the AS-, DTACK-, and BGACK- must be inactive before it sends a BGACK-. The device remains in control until it inactivates the BGACK- signal, which should be done only at the completion of the bus cycle(s).

A bus request can be initiated from any assembly attached to either the MFI or expansion connector, but not directly from the mainframe. The Main PCA does provide a priority encoding circuit that accepts a bus request (BR) and outputs a bus grant (BG). This circuit, composed of sections of U64 and U65, latches upon receipt of a bus request to ensure that the bus grant is output to the requesting device.

Bus Error and Halt

The 68000 transfers data asynchronously. That is, any device desiring to communicate with the microprocessor does so by handshake. If for some reason a handshake is not completed within seven microseconds, the hardware generates a Bus Error (BERR-) signal at U32-24. With BERR- active, the data and address busses are "off", and the current bus cycle is terminated. When the BERR- goes from active to inactive, several processes occur. The microprocessor stacks the contents of the program counter, the status register, and the error information. Next, a vector table address is read, and a software bus error handler routine from that address is then executed. Refer to Exception Processing later in this description for more information.

The BERR- acts similarly to a non-maskable interrupt, except that the microprocessor stores extra data on the stack. Bus errors can be used to detect the absence of accessories and options during initialization. The BERR- signal is generated by U40 using the enable (E) signal from J4.

The HALT- signal on U32-19 halts the microprocessor (after the current bus cycle) with a continuous active low. A continuous active high on this pin allows the 68000 to run.

If software tries to address a space with no valid memory, U40 asserts a bus error after six E clock periods. At any time, a write command to ROM also generates a bus error.

Privilege Modes

The following paragraphs explain activities of the 68000 that are not related to normal operation. The microprocessor exists in one of three modes: normal, exception, or halted. Exception processing and the 9100A/9105A system interrupts are covered. The normal situation allows for executing instructions, memory read and/or write, and storing results. A stop instruction stops the 68000 and is not related to a halt instruction.

Two types of privilege modes exist within the 68000: the supervisor mode and the user mode. The supervisor mode has higher priority than the user mode. The S-bit of the status register determines the mode in which the microprocessor operates. A 1 in the S-bit designates the supervisor mode, and all exception processing is performed in this state. All operations that require stacking during exception processing use the supervisor stack pointer.

The user mode is the lower of the two privilege modes, with 0 in the S-bit of the status register. Most instructions are executable (as in the supervisor mode) except for the stop and reset instructions. In the user mode the system stack pointer or address register 7 use the user stack pointer. To change from user to supervisor mode during the executing of instructions requires a change from normal to exception processing. To make this change the current status of the S-bit is saved, and the S-bit is forced to a 1. The set S-bit allows the microprocessor to resume the execution of instructions to process the exception in the supervisory mode.

Exception Processing

The 68000 categorizes resets, traps, interrupts, and bus errors as exceptions. Exceptions can be generated by either internal (software) or external (hardware) causes. All exceptions are assigned a number (0 through 255 decimal or 0 through FF hex). All exceptions are handled through a non-relocatable Exception Vector Table located at address 000000 through 0003FF. Each vector consists of four address bytes containing the exception handling routine address.

The externally generated exceptions are Reset, Bus Error, and Interrupt, all discussed in Table 3-1, Signal Descriptions. The internally generated exceptions can occur from program control operations such as trap (TRAP), trap on overflow (TRAPV), check data against upper bounds (CHK), divide (DIV), and trace (TRACE). In addition, software errors such as illegal instructions, word fetches from odd addresses, and privilege violations can cause exceptions. The internally generated exceptions act like non-maskable interrupts.

INTERRUPTS

The 9100A/9105A system uses 15 different interrupts allowing hardware and software to stop the 68000 operation and identify an error or specific condition. The interrupts are prioritized as follows according to their importance:

- The Parity Error Interrupt (I15) is level 7, which is non-maskable (NMI).
- All level 6 and lower levels are software maskable by level.
- Levels 7 through 2 are each used by only one interrupt.
- The level 1 interrupt is shared by several different interrupts. The interrupts within level 1 have priorities to prevent simultaneous requests.
- Level 0 indicates no interrupt is pending.

Pending interrupts are detected between instructions. An interrupt is acknowledged and the service routine started only if the pending interrupt has a higher priority than the current processor priority. When an interrupt is acknowledged, the hardware places a vector value on the data bus. This vector points to a memory location where the address of the interrupt routine is stored. Interrupts can be polled by reading the interrupt vector at byte location 094001. An interrupt request must be reset by the interrupt acknowledging routine. Individual interrupt descriptions in the following paragraphs provide more details.

A list of hardware generated exceptions and their vectors is shown in Table 3-4. These exception vectors are listed by priority with the top priority vector listed first. The maximum amount of vectors is 256. The vectors with priority levels 1 to 7 (refer to Table 3-4) are hardware generated at an interrupt acknowledge. Bus Error and Reset (Level *) behave differently; these exceptions always go to a predetermined address.

The interrupt circuitry located on the Main PCA contains two priority encoders (U49, U75), a D-type latch (U63), and several gates (U54B, U56A-D, U57A). This main interrupt system inputs each 9100A/9105A interrupt. When one interrupt or any number of interrupts go active low, U49 and U75 prioritize the interrupt to honor first. The highest priority interrupt is the Parity Error Interrupt, and the lowest priority is the Self-Vectored Interrupt. The correct priority is assigned to the interrupt control signals (IPL0, IPL1, and IPL2). When an interrupt acknowledge cycle occurs, U63 provides the correct interrupt vector to the data bus, and the reading produces a DTACK-. During a level 1 or self-vectored interrupt, U63 and the READINT- signal are disabled by EXT-INTA. An interrupt acknowledge is sent to the interrupting device through either the Multi-Function Interface PCA (MCINTA-) or the Expansion PCA (ECINTA-). The interrupting device can then supply the DTACK- and the vector.

Table 3-4. Interrupt Vector Table

Level	Number	Name	Hex Vector	Hex Address
*	RESET	Reset	00	00000
*	BERR	Bus Error	02	00008
7	I15	Parity Error Interrupt	8F	0023C
6	I14	Floppy Data Interrupt	9F	0027C
5	I13	DTIO # 1 Interrupt	AF	002BC
4	I12	DTIO # 2 Interrupt	BF	002FC
3	I11	MFI Card Interrupt 2	CF	0033C
2	I10	Expansion Card Interrupt 2	DF	0037C
1	I9	Floppy Control Interrupt	EF	003BC
-	I8	Not Usable	--	-----
1	I7	Probe Interrupt	78	001E0
1	I6	I/O Over Current Interrupt	79	001E4
1	I5	Pod Interrupt (see below)	7A	001E8
1	I4	Pod Power Fail Int (see below)	7B	001EC
1	I3	I/O Module General Interrupt	7C	001F0
1	I2	I/O Module DCE Interrupt	7D	001F4
1	I1	Video Controller Interrupt	7E	001F8
1	I0	Self-Vectored Interrupt	--	-----
-	--	No Interrupt	77	001DC

Interrupts and interrupt acknowledge for the MFI and expansion assemblies are handled in the same manner as bus requests and bus grants. Several sections of U64 and U65 provide a latch upon receipt of an interrupt to ensure that the first interrupting device receives the interrupt acknowledge.

Parity Error Interrupt

The 9100A/9105A checks parity on RAM reads. The 9100A/9105A tests high and low bytes separately. If the RAM read is a byte access, only the byte being read is tested. When a parity error is detected, the non-maskable Parity Error Interrupt (I15) is set, and microprocessor status information is latched. The latch is readable at address 098000 and is described in Table 3-5.

Table 3-5. Microprocessor Status Latches U61 & U62

BIT #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	FC1	PH	PL	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8

- FC1 is Function Control 1 from the microprocessor. It is low if the error occurred during a data access, and it is high if the error occurred during a program access.
- PH and PL are Parity High and Parity Low. One or both of these are set to indicate if the high or low byte of address had the error.
- A20 through A8 are the top bits of the address bus, allowing for error location within 256 bytes.

The latched information allows the processor to determine which 256-byte block of memory failed, whether the error was in the high or low byte, and if the failed location contained data or a program. When the processor reads this latch, the interrupt automatically clears.

Floppy Data Interrupt

The Floppy Data Interrupt is generated by the floppy controller either when it needs the next byte of data while doing a write or when the next byte of data is available in read mode. The interrupt is automatically cleared when the byte is received or read. The interrupt can be enabled or disabled by a bit in the floppy controller latch, and it can be individually polled at DTIO #2 Input Port, bit 4.

DTIO #1 Interrupt

The DTIO #1 Interrupt is generated by the DTIO (Dual UART/Timer/IO) #1 in response to a variety of conditions that may include the following:

- Transmit Buffer Empty
- Receive Buffer Full
- Break Received
- Timer Interrupt
- Pod Change
- 500 millisecond (Frequency Gate)

All possible interrupts can be polled at the ISR (Interrupt Status Register) of the DTIO. A separate register, the IMR (Interrupt Mask Register), is used to program which of the possible interrupts is allowed to generate an interrupt. After an interrupt is generated, the ISR must be read to determine the cause. Different actions are needed to reset the different types of interrupts.

DTIO #2 Interrupt

The DTIO #2 Interrupt is generated by the second DTIO and is similar in function to the DTIO #1 Interrupt. Possible DTIO #2 conditions include:

- Transmit Buffer Empty
- Receive Buffer Full
- Break Received
- Timer Interrupt
- Disk Change

MFI Card Interrupt 2

This interrupt is generated by a peripheral on a card plugged into the Multi-Function Interface (MFI) Card Slot. This interrupt is intended to be used by the SCSI controller chip under program control. This interrupt can be software disabled and polled instead. The MFI Card Interrupt is not used on the 9105A.

Expansion Card Interrupt 2

The Expansion Card Interrupt is reserved for devices connected to the expansion bus.

Floppy Controller Interrupt

The Floppy Controller Interrupt is generated by the floppy controller in response to a variety of conditions. The interrupt status register of the chip must first be read to determine the cause. This interrupt can be individually polled at DTIO #2 Input Port, bit 5.

Probe Interrupt

The Probe Interrupt is generated by the single-point probe for either a blown fuse or a button press. A probe chip status register read is performed to determine the cause.

I/O Overcurrent Interrupt

The I/O Module power supply generates an overcurrent interrupt, (IOOCI), when the current limit is exceeded. The interrupt is generated and latched on the Probe-I/O PCA, located in the mainframe. If this interrupt should occur, a control signal (ODRESET-) is sent to the I/O Module, which instantly turns off the overdrivers. Before clearing the interrupt, the overdrivers must be written to the tristate condition.

Pod Interrupt and Pod Power Fail Interrupt

The pod interrupts (I4, I5) are available and are polled, but they are not used by the 9100A/9105A.

I/O Module General Interrupt

This interrupt can be caused by a button press or a blown fuse on an I/O Module. The interrupt status register(s) on the I/O Module(s) must be read to determine the cause.

I/O Module Data Compare Equal Interrupt

The I/O Module Data Compare Equal Interrupt is generated by one of the I/O Modules when the programmed data compare register matches the input data. This interrupt can also be enabled to toggle MAINSTAT and/or ABORT to the pod. This allows DCE to cause the pod to exit quickly from RUNUUT or abort a test on a predetermined condition.

Video Controller Interrupt

The Video Controller Interrupt is reserved for use by the Video Controller PCA. The present pca does not use this interrupt.

Self-Vectored Interrupt

The Self-Vectored Interrupt (I0), is a special case. It can be generated by more than one device on either the MFI PCA Slot, or the Expansion Bus PCA Slot. A separate Interrupt Acknowledge (INTA) is sent to each pca slot to indicate which interrupt is being acknowledged. The initiating device must supply a vector and DTACK- or a VPA- (for auto-vectoring mode) when it is acknowledged.

No Interrupt

This vector is read if no interrupts are pending or if the interrupting device removed the request before the interrupt acknowledge cycle.

Asynchronous Execution

The 68000 can operate independently of the clock frequency by using only the handshake lines (AS-, UDS-, LDS-, DTACK-, BERR-, HALT-, and VPA-) for data transfer control. The AS- signal is issued by the microprocessor to begin the bus cycle. The data strobe signals verify that the data is valid on a write cycle. The memory space or peripheral places the requested data on the bus for a read cycle or latches the data on a write cycle. The DTACK- signal is issued by the data source to end the bus cycle.

If there is no response from the data source or if a wrong address is accessed, the BERR- or BERR- and HALT- are sent to the 68000 to abort or rerun the bus cycle. On a read cycle, the DTACK- signal can be sent before data is valid. A maximum of 90 nanoseconds is then available for valid data to be latched in the 68000. No maximum length of time is required between AS- and DTACK- signals.

Reset Signal Description and Generation

The following paragraphs describe the RESET- signal types, their use, and how they are produced on the Main PCA. The four types of resets are as follows:

- Power-Up Reset

  This is a "cold" start. It occurs at power up, allowing the processor to initialize the system.

- External Reset

  The hardware has an external switch that allows the user to reset the system. This reset button is debounced and shaped so it will not harm the RAM data. (The user probably was experiencing a situation that was abnormal to be using the reset button).

- Power Glitch Reset

  The mainframe has a special chip (U87) that detects the 5V dc supply falling below 4.5V dc. The length of the reset pulse is equal to the length of the power low time plus the time controlled by C12. If the power goes bad for a long time, the RAM data has probably been lost.

- Software Reset

  A Software Reset does not actually reset the microprocessor. Instead, it is a way for the software to toggle the RESET- line. A Software Reset can be used to reinitialize some peripherals such as the Floppy Disk Controller or the Application Keypad/VF Display Controller.

The reset circuitry located on the Main PCA contains a triggerable multivibrator (U88A), the external reset button (SW1), a power monitor (U87), two Schmidt trigger inverters (U71D, U71E) and a D-type flip-flop (U79A). The reset circuit contains a debounce circuit that cleans up the Ext-Reset signal once the user pushes SW1. U88A produces a long power up reset logic high signal during a cold startup, required by the 68000. The Power-Up Reset and Ext-Reset are gated by U78B to become the RESIN- input of U87. The U87 is used as a reset controller that supervises the supply voltage during power on. U87 keeps its output pin 5 active until the supply voltage reaches 5 volts. If the supply voltage drops below 4.7 volts, the circuit generates reset signals until 5 volts returns, to ensure a proper reset.

Address Decoding and DTACK

Address decoding for all circuits except RAM and ROM is accomplished by U17 and U70. U17 divides the low part of the address base into 64K segments. These segments are used by the floppy controller, the expansion bus connector, the multi-function interface, the probe, and the I/O Module. In addition, two segments are used by the video circuit. A final segment is further divided into 16K segments by U70. These segments are used by the UART (DTIO), interrupt logic, read parity control, and the pod.

Most address decode outputs connect to chip select inputs for the respective circuits. The DTACK- output, which instructs the microprocessor to complete the access cycle, is generated by U55 when the addressed circuit responds with the appropriate signal. For circuits requiring 0 wait states, the appropriate low signals are fed directly to U55. Other circuits require wait states to accommodate a longer access period. Parity reads, UART, and pod circuitry require one wait state. Video, floppy disk, and other pod circuits require three wait states. Signals for either number of wait states are fed through U34 and clocked into U55 by U50. U33 serves as an active pull-up for the DTACK signal out of U76.

Some peripherals require extra setup time during reads and writes. This requirement is satisfied with the new data strobe (NDS) signal from U79. During the write cycle, NDS is active one-half clock cycle after the address strobe. NDS is also withdrawn one-half clock cycle before the end of the write cycle to allow for data hold time.

RAM

RAM CONFIGURATION

Standard configuration includes 2M bytes of RAM for the 9100A and the 9105A. Either instrument can be expanded to 4M bytes of RAM. RAM is housed in single-in-line modules (SIMs), designated as U13, U14, U15, and U16. To achieve 2M bytes, four 512K-byte SIM modules are used. Memory expansion to 4M bytes can be achieved using four 1M-byte SIMs. The SIMs must be exchanged in pairs. The 9105A with serial numbers prior to 4352000 used a standard 1.5M-byte RAM configuration (two 512K and two 256K SIMs), expandable to 4M bytes as stated above.

An 8-segment DIP switch (U83) must be set for each RAM configuration. The settings are shown in Table 3-6. The RAM configuration is also saved as a code in non-volatile memory on the Main PCA (EEPROM U11).

Table 3-6. RAM Configuration (U83)

MODULE TYPE U13/U14	MODULE TYPE U15/U16	TOTAL BYTES	ADDRESS RANGE	SWITCH SEGMENTS 1234 5678
512K	256K	1.5M	C00000-D7FFFF	1001 1011 (9B)
512K	512K	2M	C00000-DFFFFF	1001 1001 (99)
1M		2M	C00000-DFFFFF	0010 0001 (21)
1M	1M	4M	C00000-FFFFFF	0011 0001 (31)

1 = ON (closed)
0 = OFF (open)

For each of these configurations, the first 8K bytes of RAM (C00000 through C01FFF) are accessible only by Supervisor Mode. An access to this area attempted by User Mode produces a Bus Error Exception and does not affect RAM contents.

RAM TIMING

To select a RAM address, U29, U30, and U31 multiplex 20 address lines (A01 through A20) into 10 address signals (RA0 through RA9). This multiplexed address is latched into RAM under control of both a row-address-strobe signal (RAS-) and a column-address-strobe signal (CAS-).

Upper (D15 through D08) and/or lower (D07 through D00) byte(s) can be read from bank 1 or 2. Bank 1 comprises U13 and U14. Bank 2 comprises U15 and U16. Clock signals and microprocessor read asynchronous bus control signals (LDS, UDS) determine read timing.

RAM REFRESH

RAM Refresh utilizes a state machine operating at approximately 33 kHz. RAM Refresh is initiated by a count of E clocks. E clocks are divided by two (U77B) and counted by U81. At every twelve E clocks, U81 generates refresh request (RFRQ). If there is no RAM access occurring at the same time, U85B generates refresh grant (RFGT). If a RAM access is occurring, RFGT is not generated until the end of the RAM access cycle. One-half cycle after RFGT, refresh address enable (RFAE) is generated to turn off the normal multiplexed address lines and enable the refresh address outputs from U26. One-half cycle later, U80A generates refresh RAS (RRAS), which performs the actual refresh. Refresh address is then disabled, and, through U68B, U81 is cleared. RFRQ and RFGT are thereby cleared. On each refresh, U85A changes states, clocking the refresh address output from U26. The Refresh cycle repeats 256 times in approximately 4 ms.

U85, pin 6 changes state for each refresh cycle. This transition is used as the lowest bit of the RAM refresh address through U33. On every change of the low bit, the clock to U26 is enabled to obtain the other eight bits of RAM refresh address (a nine-bit address).

Note that other uses of the U85 33 kHz signal include power supply switching and do not impact the scope of this discussion.

RAM PARITY

On every write cycle, parity is generated for each data byte. The high byte is generated by U24, and the low byte is generated by U23. The ninth bit into the parity comparator is held low during a write. If the parity on the rest of the bits is even, the EV (even) output of the parity comparator goes high. This output serves as a ninth bit of data, resulting in odd parity for the nine bits. If the parity on the rest of the bits is already odd, the ninth bit (EV) remains low to keep the parity odd.

On read cycles, this ninth bit serves as read data. Even parity at this time results in a parity error, which is latched for both high and low bytes by U73. U73 also outputs PLATCH (parity latch) to U61 and U62, latching the address and parity status bits. Parity interrupt is also generated at this time by U78. Refer to the Parity Interrupt description. The latches are cleared by either a reset or a read of the parity latches.

ROM

Sockets for U45/U48 (High Bank) and U46/U47 (Low Bank) accept 256K byte or 512K byte EPROMs, or 1M byte mask ROMs. A PAL (Programmable Array Logic), U28, provides four wire jumpers. Each jumper combination specifies select logic for the desired ROM configuration as shown in Table 3-7.

Table 3-7. ROM Select Logic

JUMPERS				SIZE	ADDRESSES	
W4	W3	W2	W1		Low Bank	High Bank
X	X	0	0	256K	00000 - 0FFFF	na
X	X	0	1	256K	00000 - 0FFFF	na
X	X	1	0	512K	00000 - 1FFFF	na
X	X	1	1	1M	00000 - 3FFFF	na
0	0	X	X	empty	na	none present
0	1	X	X	256K	na	40000 - 4FFFF
1	0	X	X	512K	na	40000 - 5FFFF
1	1	X	X	1M	na	40000 - 7FFFF

(0 = closed, 1 = open)

POD Interface

The Pod Interface accommodates information transfer in two bytes. A low byte is used as an 8-bit, bidirectional data port. U42 handles data (D00 through 07) inputs to the 9100A/9105A. Transparent latch U37 handles data outputs to the pod. An 8-bit, bidirectional high byte (status register) transfers information on data lines D08 through D15, using U58 for inputs and U53 for latched outputs.

Bit assignments for both status and data bytes are shown in Table 3-8. Latched outputs are cleared low by a reset.

Data or response from the Pod is read at handshake completion. Data from the 9100A/9105A to the Pod is latched when written. POD_OE must be active to enable the output buffer.

Refer to Table 3-9 for the pinout and function of each signal line for the Pod Interface.

On the 9100A, presence of a pod is indicated on the PODPRESENT- line when a valid signal is detected on the POWERFAIL line (J9-11).

Table 3-8. Pod Control Port Bit Assignment

STATUS BYTE (ADDRESS 9C000)

BIT	INPUT (U58)	LATCHED OUTPUT (U53)
D15	MAINSTAT	MAINSTAT
D14	POD_OE	POD_OE
D13	PODSTAT-	POD_RESET
D12	ABORT	ABORT
D11	PODPRESENT-	ENDCE-ABORT
D10	DCE	ENDCE-MAINSTAT
D09	PODINT	EN-PODINT
D08	POWERFAIL	EN-PWRINT

NAME	I/O	DESCRIPTION
MAINSTAT	I/O	Handshake line from 9100A/9105A to the Pod.
POD_OE	I/O	Enables the Pod data buffer for write data. A high true signal enables (drives) the latched output data onto the Pod data lines (POD0 through POD7).
POD_RESET	O	Signal from 9100A/9105A to reset the Pod.
ABORT	O	Signal from the 9100A/9105A telling the Pod to abort a long operation.

Table 3-8. Pod Control Port Bit Assignment (cont)

ENDCE-ABORT	O	Enables the I/O Module Data Compare Equal (DCE) Signal to set the ABORT signal to the Pod. This allows the Pod to abort an operation upon a preprogrammed condition.
ENDCE-MAINSTAT	O	Enables the I/O Module Data Compare Equal (DCE) signal to set the MAINSTAT signal to the Pod. This allows the Pod to abort a RUN UUT upon a preprogrammed condition or address.
EN-PODINT	O	Enables the PODINT Signal from the Pod to interrupt the processor.
EN-PWRINT	O	Enables the POWERFAIL Signal from the Pod to interrupt the processor.
PODSTAT-	I	Active low handshake line from Pod.
PODPRESENT-	I	A low true signal that indicates when a Pod is connected to the Pod Interface connector. This signal is derived from the Pod interface POWERFAIL signal. This signal can be enabled to generate an interrupt through the DTIO on change of state, (i.e., connecting or disconnecting the Pod).
DCE	I	Monitors the I/O Module Data Compare Equal (DCE) Signal.
PODINT	I	Buffered active high interrupt line from certain pods. This line will also generate an interrupt if enabled by EN-PODINT.
POWERFAIL	I	Active when Pod detects a bad UUT power supply. Can be enabled to cause an interrupt if EN-PWRINT is set.

DATA BYTE (ADDRESS 9C001)

BIT	INPUT (U42)	LATCHED OUTPUT (U37)
D07-D00	READ DATA	WRITE DATA

Table 3-9. Pod Interface Pinout

NAME	FUNCTION	PIN
POD0	Data bit 0	8
POD1	Data bit 1	20
POD2	Data bit 2	7
POD3	Data bit 3	19
POD4	Data bit 4	6
POD5	Data bit 5	18
POD6	Data bit 6	5
POD7	Data bit 7	17
MAINSTAT-	Handshake	12
PODSTAT-	Handshake	24
PODRESET-	Resets Pod	23
POWERFAIL	Power out of tolerance	11
PODINT-	Pod interrupt	1
ABORT-	abort	9
PODSYNC-	Pod Sync	10
SYNC SH	Pod sync shield	22
+5V	+5 volt power	2,15
+12V	+12 volt power	14
-5V	-5 volt power	21
GND	Ground	4,13,16,25
X SHLD	Pod cable shield	3

DUART-Timer-I/O

The 9100A/9105A uses two 2681 DTIOs (U12 as DTIO1 and U7 as DTIO2). Each performs multiple Dual Asynchronous Receiver/Transmitters (DUART), timers, and input/output functions with two serial ports, one parallel input port, one parallel output port, and a timer.

For DTIO1, register addressing and descriptions are given in Table 3-10. Specific functions are:

- Programmable Timer Interrupt
  - OP3: timer output (50 ms)
  - INT-: Interrupt Request to microprocessor

- EEPROM Control
  - IP4: data output from EEPROM
  - OP4: data input to EEPROM
  - OP5: serial clock to EEPROM
  - OP6: chip enable to EEPROM

- Pod Present Detection
  - IP2: PODPRESENT change-of-state detection (can generate interrupt)

- Frequency Gate Generation/Detection
  - IP3: FGATE frequency gate input
  - OP2: frequency gate load

- DTIO1, Serial Port A: Application Keypad/Display
  - TxDA: Data to Application Keypad/Display
  - RxDA: Data from Application Keypad/Display
  - CTSA- (IP0): Clear to Send from Application Keypad/Display.

  Transmit and receive are at 19.2K baud. This port automatically holds off transmission data when the Keypad/Display is too busy to accept data.

- DTIO1, Serial Port B: Earth Referenced RS-232 Port #2
  - TxDB: Transmit Data
  - RxDB: Receive Data
  - CTSB- (IP1): Clear to Send
  - RTSB- (OP1): Request to Send

  Supports programmable baud rates, data width, stop bits, parity, and interrupts on buffer conditions, with three-deep FIFO on both transmit and receive.

For DTIO2, register addressing and descriptions are provided in Table 3-11. Specific functions are:

- DTIO2, Serial Port A: Programmers Keyboard
  RxDA: Programmers Keyboard Data

  The baud rate is 1200 baud. The keyboard has a separate reset line, which is connected to OP7 of DTIO #2.

- DTIO2, Serial Port B: System Referenced RS-232 Port #1
  TxDB: Transmit Data
  RxDB: Receive Data
  CTSB- (IP1): Clear to Send
  RTSB- (OP1): Request to Send

  Supports programmable baud rates, data width, stop bits, parity, and interrupts on buffer conditions, with three-deep FIFO on both transmit and receive.

- Second Programmable Timer Interrupt
  OP3: Timer output, Divide by 16
  INT-: Interrupt Request to microprocessor

- Floppy Disk Change Detection
  IP2: Drive 1 Disk Change (can generate interrupt)
  IP3: Drive 2 Disk Change (can generate interrupt)

- Floppy Disk Interrupt Monitor
  IP4: Read Floppy Drive Data Interrupt Bit
  IP5: Read Floppy Drive Interrupt Bit

- Programmers Keyboard Reset
  OP7: KBRST- Keyboard Reset

- I/O Module Power Supply Control
  OP5: I/O Module Reset
  OP6: I/O Module Low Current
  IP6: Input from I/O or Probe Board (spare)

- Other
  OP2: RUN UUT LED Drive
  OP4: Disk Access LED Drive

Table 3-10. DTIO #1 (Channels A, B)
Register Addressing and Description

MSA	$90001	* mode register channel A (R/W)
SRA	$90003	* status register channel A (R)
CSRA	$90003	* clock select register A (W)
CRA	$90005	* command register A (W)
ADATA	$90007	* data holding registers A (R/W)
IPCR	$90009	* input port change register (R)
ACR	$90009	* aux control register (W)
ISR	$9000B	* interrupt status register (R)
IMR	$9000B	* interrupt mask register (W)
CTU	$9000D	* counter/timer upper data (R)
CTL	$9000F	* counter/timer lower data (R)
CTUR	$9000D	* counter/timer upper register (W)
CTLR	$9000F	* counter/timer lower register (W)
MRB	$90011	* mode register channel B (R/W)
SRB	$90013	* status register channel B (R)
CSRB	$90013	* clock select register B (W)
CRB	$90015	* command register B (W)
BDATA	$90017	* data holding registers B (R/W)
INP	$9001B	* input port (R)
OPCR	$9001B	* output port configuration register (W)
SCC	$9001D	* start counter command (R)
SOPB	$9001D	* set output port bits command (W)
STC	$9001F	* stop counter command (R)
ROPB	$9001F	* reset output port bits command (W)

Table 3-11. DTIO #2 (Channels C, D)
Register Addressing and Description

MRC	$90000	* mode register channel C (R/W)
SRC	$90002	* status register channel C (R)
CSRC	$90002	* clock select register C (W)
CRC	$90004	* command register C (W)
CDATA	$90006	* data holding registers C (R/W)
IPCR	$90008	* input port change register (R)
ACR	$90008	* aux control register (W)
ISR	$9000A	* interrupt status register (R)
IMR	$9000A	* interrupt mask register (W)
CTU	$9000C	* counter/timer upper data (R)
CTL	$9000E	* counter/timer lower data (R)
CTUR	$9000C	* counter/timer upper register (W)
CTLR	$9000E	* counter/timer lower register (W)
MRD	$90010	* mode register channel D (R/W)
SRD	$90012	* status register channel D (R)
CSRD	$90012	* clock select register D (W)
CRD	$90014	* command register D (W)
DDATA	$90016	* data holding registers D (R/W)
INP	$9001A	* input port (R)
OPCR	$9001A	* output port configuration register (W)
SCC	$9001C	* start counter command (R)
SOPB	$9001C	* set output port bits command (W)
STC	$9001E	* stop counter command (R)
ROPB	$9001E	* reset output port bits command (W)

MICROFLOPPY DISK SYSTEM

Disk Drive

The 9100A uses one OEM 3.5-inch, double-sided, double-density microfloppy disk drive. On the 9105A, two of these drives are used. Each disk uses 80 tracks per side (0 to 4F hex), formatted as 16 sectors of 256 bytes per track, for a formatted capacity of 640K bytes. Each drive is accessed and formatted through the Floppy Controller.

Floppy Drive Controller

An FD1797 floppy controller (U43) and an FDC9229 Floppy Disk Interface Circuit (FDIC) are used for floppy drive control. The floppy controller does not format the floppy disk; this function is performed through software. The controller does perform the following functions:

- It searches for the correct track and sector.
- It calculates CRC values and inserts all required CRC's during a write.
- It serializes data on a write and decodes data on a read.

The FDIC circuit (U44) performs digital data separation and track-selectable write pre-compensation.

Addresses for U43 Floppy Controller registers are shown in Table 3-12.

Table 3-12. Floppy Controller Addressing

NAME	ADDRESS	DESCRIPTION
DCOMND	$80001	* Disk Command Register (write)
DSTAT	$80001	* Disk Status Register (read)
DTRACK	$80003	* Disk Track Register (read/write)
DSECTOR	$80005	* Disk Sector Register (read/write)
DDATA	$80007	* Disk Data Register (read/write)

Output latch U60 (address 80000) controls drive selects and other features. Table 3-13 describes U60 outputs.

Table 3-13. Floppy Drive Control Latch Outputs

NAME	DESCRIPTION
DSO, DS1	Drive Selects (turn on motor and enable communications with floppy controller for one drive at a time.)
SPARE	(not used)
MINI	Controls Floppy Controller clock to select data rate for mini (5 1/4- or 3 1/2-inch, logic low) or standard (8-inch, logic high) drive.
DENS	Selects between single density (logic low) and standard double density (logic high).
PO, P1	Selects the write pre-compensation time, as shown below.

P1	PO	TIME
0	0	0 ns
0	1	125 ns
1	0	250 ns
1	1	375 ns

EN-INT: Enables the floppy data interrupt.

Interrupts

The Floppy Data Interrupt is generated by the floppy controller when it needs the next byte of data while doing a write or when the next byte of data is available in read mode. The Floppy Data Interrupt is automatically cleared when the byte is received or read.

The Floppy Controller Interrupt is generated by the floppy controller in response to a variety of conditions. The chip's interrupt status register must first be read to determine the cause. This interrupt can be polled at DTIO #2 Input Port, bit 5.

HARD DISK SYSTEM

On the 9100A, a standard-feature, O.E.M.-supplied hard disk occupies the space otherwise used in the 9105A for a second floppy disk drive. System software that is resident on this 20M byte, 3.5-inch hard disk is backed up with floppy disks.

The hard disk controller, also an O.E.M. product, attaches to the Internal SCSI Connector (J2) on the Multi-Function Interface (MFI) PCA, which is plugged into J6 on the Main PCA.

POWER SUPPLY

An OEM switching power supply is used to operate from a line voltage of 90 to 132V ac (47-440 Hz) or 180 to 264V ac (47-63 Hz). Single outputs of +5.1V dc and -5V dc and two outputs of +12V dc are provided. The 9100A power supply is rated at 150W (maximum). Pin designations for the power supply are presented in Table 3-14.

Table 3-14. Power Supply Pinout

DC OUT		AC IN	
TB1-1	+12V 4.0 Amps +/- 5%	TB2-1	AC Hot
-2	+12V 2.0 Amps +/- 10%	-2	AC Neutral
-3	-5V 1.0 Amp +/- 5%		
-4,5,6	Power supply common	-3	AC Earth ground
-7,8	+5.1V 15.0 Amps +/- 4%		

OPERATOR'S DISPLAY

Vacuum-Fluorescent Display (VFD)

The vacuum-fluorescent display uses a 254 by 26 pixel layout. Each character comprises a six wide by eight deep group of pixels, allowing for a total width of 42 characters per line (numbered 0 through 41). A pseudo-character at position 42 allows for a backspace to effect character 41. The cursor cannot be positioned prior to character 0 or after character 42. The display contains up to four lines (numbered 0 through 3).

A total depth of 26 pixels allows for display of either three lines separated with a blank row (character mode), or three full lines and a partial fourth line (graphics mode). The character mode is the default at startup.

The vacuum fluorescent display is in essence a tube, with the filaments forming a heated cathode. A switcher circuit supplies 12V to one side of the filament and about 4V to the other side. These voltages are switched at the end of each scan cycle (after all grids have been scanned). The switching is synchronized to the scan rate to prevent flicker.

Each switching cycle is controlled by U14 and its associated output drivers. Two discrete actions occur at the start of each cycle. The filament drive is first switched off briefly. Next, the filament is driven (through Q2/Q6 or Q3/Q5) in the direction opposite to that used in the last cycle. Transistors Q2 and Q6 are used during one cycle direction, and Q3 and Q5 are used during the other cycle direction. U31 supports the filament drive switch off function.

The vacuum fluorescent tube grids are driven in pairs. Grid input (GI) is held high for two clock periods at the beginning of the refresh cycle. The grid drivers are shift registers that are clocked to the next set of grids with each refresh scan. The grids are driven in pairs, G1 and G2, followed by G2 and G3, and so on. This scheme is illustrated in Figure 3-4.

Anodes comprise rows A1 through D24, which are also driven in pairs. Rows A and B (or C and D) are enabled together. If dots associated with only one row are on, both rows in the pair are still enabled.

The Z8 display processor, U1, both receives inputs, data, and commands from the main microprocessor and sends data out through a TTL-level RS-232 interface. Divider U4 uses the Y1 reference clock signal (fed through U1) to derive timing signals for the circuit. U1 uses multiplexed address timing for data output; U2 latches the address for use with RAM and shift registers.

U1 receives the code for the character to be displayed, converts the code to the appropriate pixel pattern, and then writes the converted code to the appropriate row and column of the display RAM. However, U1's main function is to refresh the display tube. U1 uses pointers to the grid counters, reads data from display RAM, and, by holding A11 high, simultaneously writes data to serial shift registers U23 and U24. The state machines U14B and U15B shift the data out of the U23/U24 parallel-serial converters into the correct row drivers. This process is repeated four times for each refresh, at which time the data is latched into the row drivers.

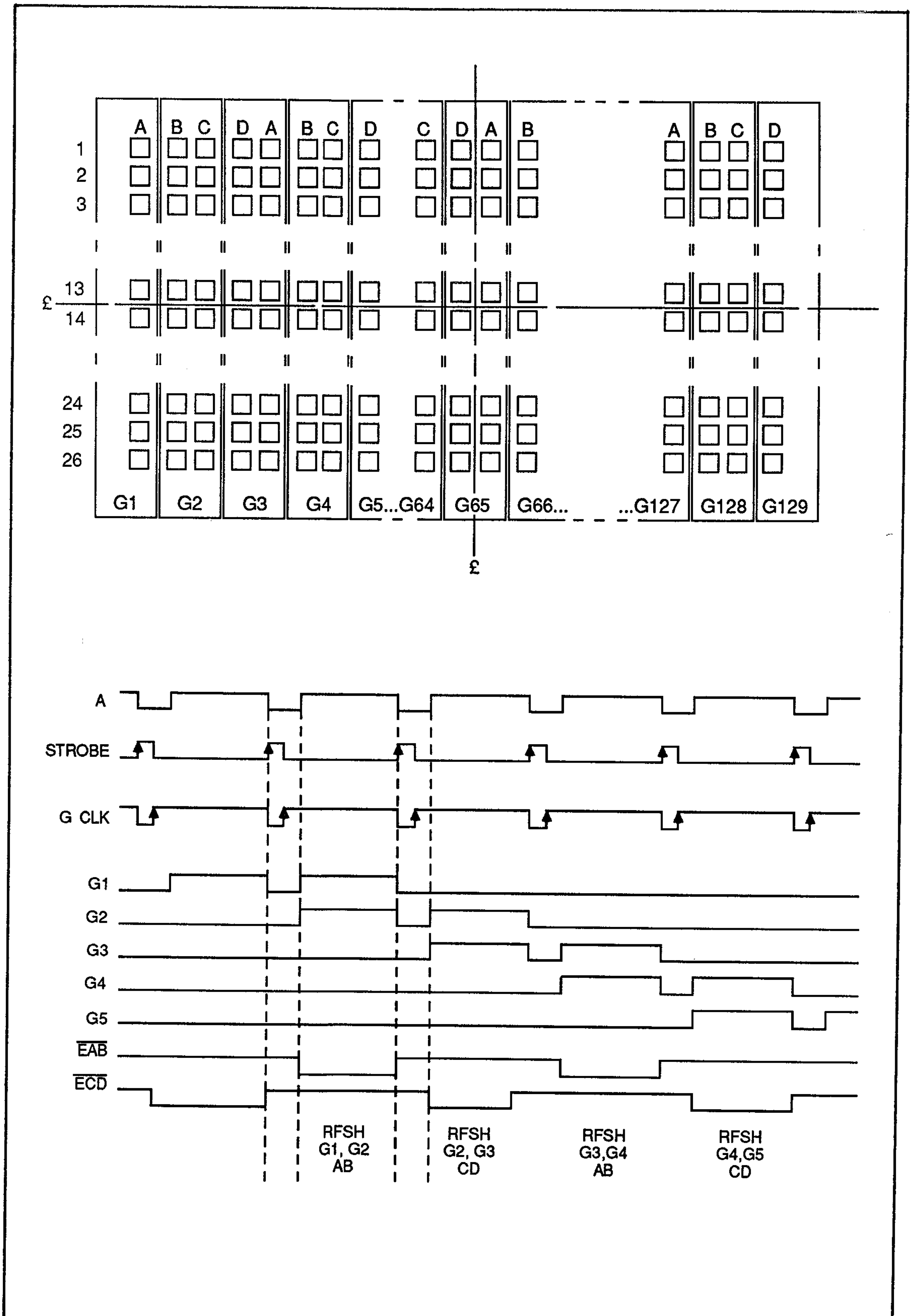


Figure 3-4. Vacuum Fluorescent Display

The SET- pulse from U1 provides the master timing signal for this refresh process. When SET- is true, grid input (GI) is also true. U13 and U14 provide the 1/4-3/4 duty cycle signal A, which is the master timing signal. One A cycle corresponds to one grid pair refresh. STROBE is used to strobe data into the row drivers. GCLK (the inverse of STROBE) is used to clock the grid drivers to the next position (G1/G2 to G2/G3, etc.). Row driver enable is provided by EAB- (for rows A and B) and by EAD- (for rows C and D). Outputs to display grid and row drivers incorporate pull-up resistors to provide valid MOS voltage levels. All grid and row drivers are disabled at reset or power-up by DSPYE (display enable) from U25.

Both grid and row currents flow through the filaments. Therefore, after a reset, the processor, U1, clears all grids and rows before a new enable is output. This action prevents filament destruction due to excess current.

Auxiliary circuitry includes the LED drivers. The RUN UUT and DISK ACCESS LEDs are driven by the Main PCA; all other LEDs are controlled by U1 (with latch U30) on the Display Interface PCA.

At the end of each display refresh, the processor scans the keypad by writing to U26, a 4-to-1 decoder. U26 drives one of the column lines low. The processor then reads the ROWBUSS to determine if any row line has been pulled low, signifying a keypress. Only one key press at a time is recognized by the processor. That key press must be withdrawn before another can be recognized. Multiple key presses are not recognized.

U28 is a shift counter whose output is used for character or graphics mode. In the character mode, nine bits are shifted out (the ninth bit designates a blank between text lines). This cycle is repeated three times, and five bits are shifted out on the fourth cycle to yield the 32 bits. In the graphics mode, an eight-bit load/shift-out cycle is repeated four times to derive 32 bits.

U29 provides a free-running oscillator for the beeper. The processor can enable either or both of two tones.

Resets are handled by U18 and U31, which reset the processor, clear all latched LEDs through U30, and clear all outputs of U25.

A 20-wire ribbon cable connects the Operator Display and Keypad to a Main PCA serial port. Data is exchanged at 19.2K baud. Ribbon cable connections are described in Table 3-15.

Displayable Characters

The characters shown in Table 3-16 (hex values 20 through FF) are displayable. Some of the display characters are not available through TL/1 programs, but can be accessed by the Main PCA processor using the hex values listed. The character codes shown in Table 3-17 are control codes of the display. These codes, which do not represent displayable characters, perform certain control functions.

Table 3-15. Ribbon Cable Connections

LINE	USE	TYPE	DESCRIPTION
10,12,14,20	Ground		
16,18	12 Volts	Power	Power for filament and for bell
6,8	5 Volts	Power	Power for logic
4	70 Volts	Power	Power for vacuum fluorescent display
1,5	Earth		Green Ground
19	Key		Key for alignment
17	RESET	Input	Active high resets the processor
15	TRANSMIT	Output	Transmits data to Main PCA at 19.2K baud
13	RECEIVE	Input	Receives data from Main PCA at 19.2K baud
11	CTS-	Output	Active low holds off Main PCA transmit
9	ROW7	Input	Last row of the keypad scan
7	COLUMN9	Output	Last column of the keypad scan
3	RUN-LED	Input	Controls "RUN UUT" LED
2	DISK-LED	Input	Controls "DISK ACCESS" LED

Table 3-16. Display Characters

20 = ' '	30 = '0'	40 = '@'	50 = 'P'	60 = '`'	70 = 'p'
21 = '!'	31 = '1'	41 = 'A'	51 = 'Q'	61 = 'a'	71 = 'q'
22 = '"'	32 = '2'	42 = 'B'	52 = 'R'	62 = 'b'	72 = 'r'
23 = '#'	33 = '3'	43 = 'C'	53 = 'S'	63 = 'c'	73 = 's'
24 = '$'	34 = '4'	44 = 'D'	54 = 'T'	64 = 'd'	74 = 't'
25 = '%'	35 = '5'	45 = 'E'	55 = 'U'	65 = 'e'	75 = 'u'
26 = '&'	36 = '6'	46 = 'F'	56 = 'V'	66 = 'f'	76 = 'v'
27 = '''	37 = '7'	47 = 'G'	57 = 'W'	67 = 'g'	77 = 'w'
28 = '('	38 = '8'	48 = 'H'	58 = 'X'	68 = 'h'	78 = 'x'
29 = ')'	39 = '9'	49 = 'I'	59 = 'Y'	69 = 'i'	79 = 'y'
2A = '*'	3A = ':'	4A = 'J'	5A = 'Z'	6A = 'j'	7A = 'z'
2B = '+'	3B = ';'	4B = 'K'	5B = '['	6B = 'k'	7B = '{'
2C = ','	3C = '<'	4C = 'L'	5C = '\'	6C = 'l'	7C = '|'
2D = '-'	3D = '='	4D = 'M'	5D = ']'	6D = 'm'	7D = '}'
2E = '.'	3E = '>'	4E = 'N'	5E = '^'	6E = 'n'	7E = '~'
2F = '/'	3F = '?'	4F = 'O'	5F = '_'	6F = 'o'	7F = Full Block
80 = reduced '0' (upper left)	88 = reduced '8' (upper left)				
81 = reduced '1' (upper left)	89 = reduced '9' (upper left)				
82 = reduced '2' (upper left)	8A = bracket (lower right)				
83 = reduced '3' (upper left)	8B = bi-directional pin				
84 = reduced '4' (upper left)	8C = large pin above chip				
85 = reduced '5' (upper left)	8D = I.C. pin above chip				
86 = reduced '6' (upper left)	8E = up arrow				
87 = reduced '7' (upper left)	8F = down arrow				
90 = reduced '0' (lower right)	98 = reduced '8' (lower right)				
91 = reduced '1' (lower right)	99 = reduced '9' (lower right)				
92 = reduced '2' (lower right)	9A = bracket (upper left)				
93 = reduced '3' (lower right)	9B = omega				
94 = reduced '4' (lower right)	9C = large pin below chip				
95 = reduced '5' (lower right)	9D = I.C. pin below chip				
96 = reduced '6' (lower right)	9E = left arrow				
97 = reduced '7' (lower right)	9F = right arrow				

Table 3-16. Display Characters (cont)

A0 = reduced '0' (center)
A1 = reduced '1' (center)
A2 = reduced '2' (center)
A3 = reduced '3' (center)
A4 = reduced '4' (center)
A5 = reduced '5' (center)
A6 = reduced '6' (center)
A7 = reduced '7' (center)
A8 = reduced '8' (center)
A9 = reduced '9' (center)
AA = divide sign
AB = +/-
AC = micro
AD = inverted '-'
AE = pi
AF = pound sign

B0 = reduced inverted '0' (center)
B1 = reduced inverted '1' (center)
B2 = reduced inverted '2' (center)
B3 = reduced inverted '3' (center)
B4 = reduced inverted '4' (center)
B5 = reduced inverted '5' (center)
B6 = reduced inverted '6' (center)
B7 = reduced inverted '7' (center)
B8 = reduced inverted '8' (center)
B9 = reduced inverted '9' (center)
BA = I.C. head
BB = I.C. body segment (full splat)
BC = reduced splat (center)
BD = box
BE = double box
BF = super-reduced splat

C0 = boxed super-reduced splat
C1 = reduced inverted 'A'
C2 = reduced inverted 'B'
C3 = reduced inverted 'C'
C4 = reduced inverted 'D'
C5 = reduced inverted 'E'
C6 = reduced inverted 'F'
C7 = reduced inverted 'G'
C8 = reduced inverted 'H'
C9 = reduced inverted 'I'
CA = reduced inverted 'J'
CB = reduced inverted 'K'
CC = reduced inverted 'L'
CD = reduced inverted 'M'
CE = reduced inverted 'N'
CF = reduced inverted 'O'

D0 = reduced inverted 'P'
D1 = reduced inverted 'Q'
D2 = reduced inverted 'R'
D3 = reduced inverted 'S'
D4 = reduced inverted 'T'
D5 = reduced inverted 'U'
D6 = reduced inverted 'V'
D7 = reduced inverted 'W'
D8 = reduced inverted 'X'
D9 = reduced inverted 'Y'
DA = reduced inverted 'Z'
DB = logic 1 level
DC = logic x level
DD = logic 0 level
DE = 0 -> 1 edge
DF = 0 -> x edge

E0 = x -> 1 edge
E1 = 1 -> 0 edge
E2 = 1 -> x edge
E3 = x -> 0 edge
E4 = left inverse line
E5 = left line
E6 = right inverse line
E7 = right line
E8 = reduced inverted *
E9 = reduced inverted up arrow
EA = reduced inverted down arrow
EB = not yet defined
EC = not yet defined
ED = not yet defined
EE = not yet defined
EF = not yet defined

F0 through FF = not yet defined

Two control modes are available. The first, display mode, specifies display of the two bit maps (page 1 or page 2) as follows:

- Display Mode 0 — Alternately displays Page 1 and Page 2 at a fixed rate of approximately 1 Hz. Display mode 0 is the default at startup.
- Display Mode 1 — Displays Page 1 only
- Display Mode 2 — Displays Page 2 only

The second, write mode, controls placement of the character as follows:

- Write Mode 0 — Places the character in both Page 1 and Page 2. Write mode 0 is the default.
- Write Mode 1 — Places the character in Page 1 only.
- Write Mode 2 — Places the character in Page 2 only.

Table 3-17. Control Characters

HEX	FUNCTION	DESCRIPTION
00	Load bell	Load bell value
01	Time out	Set time out value
02	no op	(not used)
03	Blink	Blank location in page 2, advance cursor, and set write mode 0.
04	Flash	Put the complement of the character at the page 1 cursor into page 2, advance cursor, and set write mode 0.
05	Character mode	Place extra blank dot between lines
06	Graphics mode	No extra blank dot between lines
07	Bell	Ring bell
08	Cursor left	Move cursor one character left
09	Cursor right	Move cursor one character right
0A	Cursor down	Move cursor one line down
0B	Cursor up	Move cursor one line up
0C	Clear	Place in display mode 0, place in write mode 0, clear entire display, and home cursor
0D	<cr>	Carriage return
0E	Test	Perform tests on hardware
0F	Move cursor	Move cursor to a new location
10	<bs>	Backspace and delete
11	Annunciators	Turn annunciators on or off
12	Blink mask	Make annunciators solid or blink
13	XOR next char	XOR with display the next character and advance cursor
14	Clear to eol	Clear to end of line
15	Clear line	Clear entire line and place cursor at zero character
16	Invert next char	Invert the video of the character and advance cursor

Table 3-17. Control Characters (cont.)

17	Underline	Underline character at the cursor and advance cursor
18	Display mode 0	Set display mode 0
19	Display mode 1	Set display mode 1
1A	Display mode 2	Set display mode 2
1B	Graphics	Next 6 bytes define the graphics to be placed in the display
1C	XOR graphics	Next 6 bytes define the graphics to be XORed with the old display value
1D	Write mode 0	Set write mode 0
1E	Write mode 1	Set write mode 1
1F	Write mode 2	Set write mode 2

Annunciators

Seven LED annunciators are used with the display: BUSY, STOPPED, RUN UUT, STORING SEQ, DISK ACCESS, MORE SOFTKEYS, MORE INFORMATION. The RUN UUT and DISK ACCESS LEDs are controlled by the Main PCA; the other LEDs are controlled by the Display PCA.

OPERATOR'S KEYPAD

The 55-key keypad consists of 50 hard-labeled keys and five soft-labeled keys. An LED annunciator, located on the keypad, lights when the alpha mode is activated. Functionally, the keypad is a 9-column by 8-row matrix. Pressing a key completes a connection between a particular column output and row input.

The keypad is scanned by the Display PCA after every display refresh. If a new key closure is detected at this time, the appropriate byte is sent via the serial output to the Main PCA. Values returned for each key are shown in Table 3-18.

A tenth column output (COLUMN9) is not used on the keypad. COLUMN9 is routed (along with the ROW7 input signal) across the Main PCA to the Probe I/O PCA. This arrangement allows for scanning the external footswitch input. A closure of the footswitch connection is detected and the appropriate byte sent to the Main PCA in the same fashion as with a key closure on the keypad.

PROBE I/O MODULE INTERFACE

Overview

The Probe I/O Interface provides the interface from the mainframe to the single-point Probe, Clock Module, and the I/O Connector PCA. The Interface PCA is mounted flush to the Main PCA inside the mainframe. The Probe I/O Interface block diagram, Figure 3-5, contains the following functional block groups:

- o Address Decoding
- o Probe Interface
- o Clock Module Interface
- o Custom Delay Probe Chip
- o Custom Probe Logic Chip
- o Stop Counter
- o I/O Module Interface
- o Miscellaneous Functional Blocks

Table 3-18. Key Values

KEY	VALUE	ASCII	KEY	VALUE	ASCII
SOFTKEYS	58	X	B (1011)	42	B
F1	59	Y	SETUP MENU (P)	24	$
F2	5A	Z	SEQ (Q)	25	%
F3	5B	[	POD (R)	2C	,
F4	5C	\	ROM (S)	2D	-
F5	5D	]	STIM (T)	34	4
RESET	5E	^	4 (0100)	35	5
ALPHA	20	space	5 (0101)	3C	<
EXEC (G)	21	!	6 (0110)	3D	=
PROBE (H)	28	(	7 (0111)	44	D
BUS (I)	29	)	(up arrow)	4C	L
READ (J)	30	0	REPEAT (-)	54	T
C (1100)	31	1	STOP	55	U
D (1101)	38	8	OPTION (U)	26	&
E (1110)	39	9	(V)	27	'
F (1111)	40	@	SYNC (W)	2E	.
ENTER YES	41	A	(X)	2F	/
CLEAR NO	48	H	RUN UUT (Y)	36	6
EDIT (.)	50	P	0 (0000)	37	7
HELP	51	Q	1 (0001)	3E	>
MAIN MENU (K)	22	"	2 (0010)	3F	?
GFI (L)	23	#	3 (0011)	46	F
IO MOD (M)	2A	*	←	47	G
RAM (N)	2B	+	(down arrow)	4E	N
WRITE (O)	32	2	→	4F	O
8 (1000)	33	3	LOOP (Z)	56	V
9 (1001)	3A	:	CONT (SPACE)	57	W
A (1010)	3B	;	footswitch	6F	o

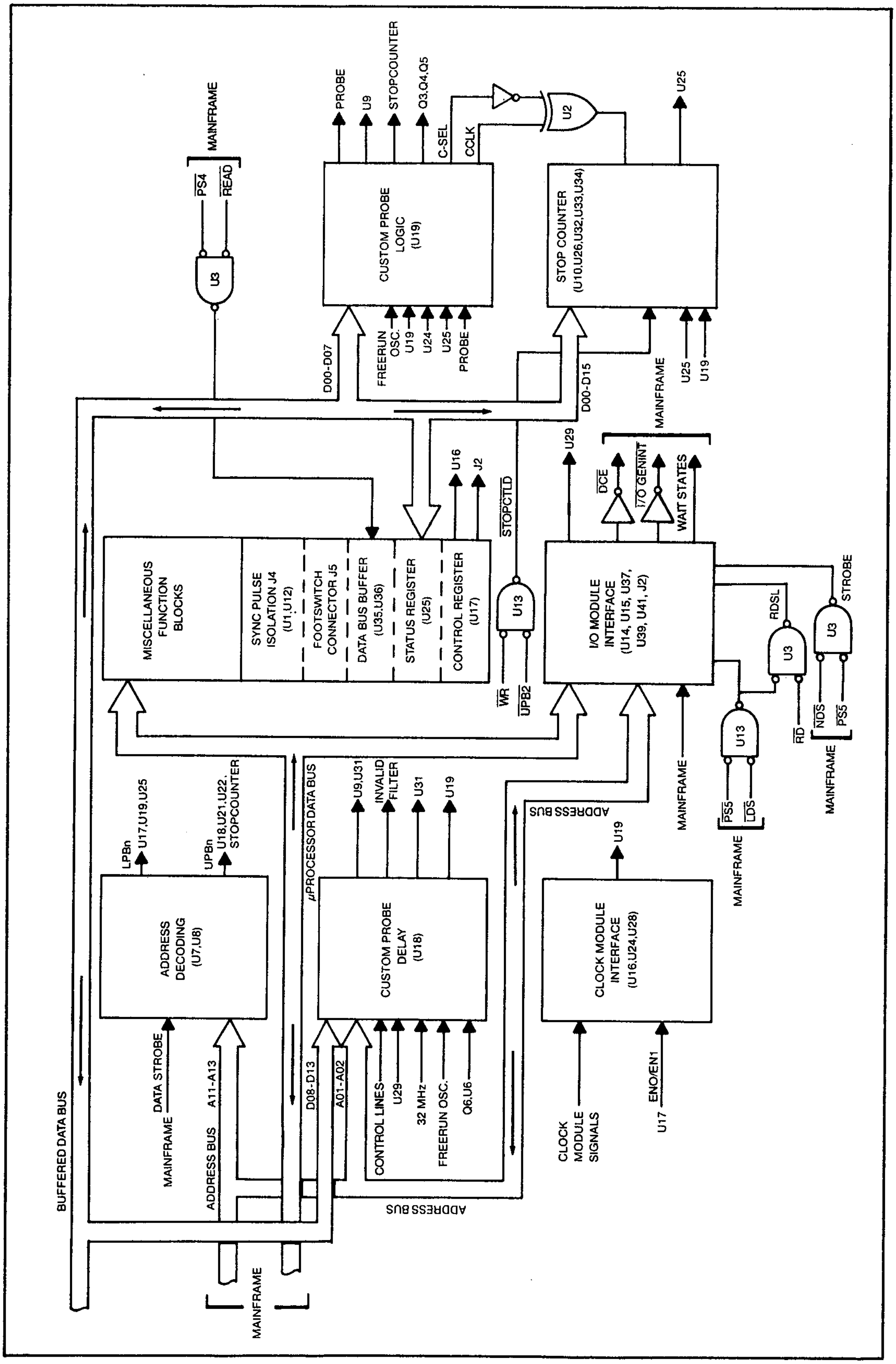


Figure 3-5. Probe I/O Interface Block Diagram

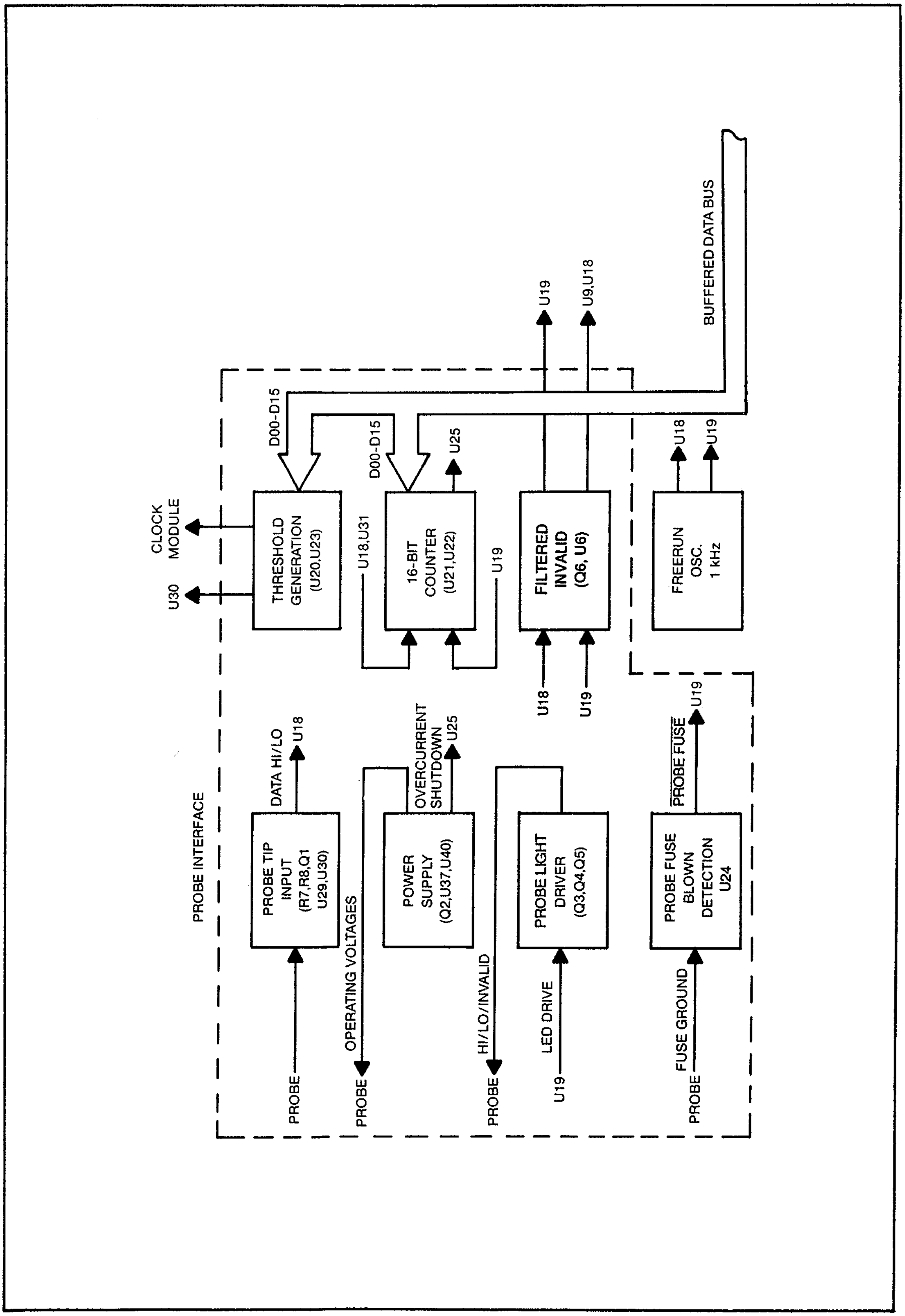


Figure 3-5. Probe I/O Interface Block Diagram (cont)

Probe I/O Module Interface Addressing

The 9100A/9105A allocates two 64K blocks of address space for the Probe and I/O Module system. The address space for the Probe, 0C0000 through 0CFFFF, is selected by PS4- (Peripheral Select 4). The four strobe signals PS4-, UDS- (Upper Data Strobe), LDS- (Lower Data Strobe), and NDS- (New Data Strobe) are gated by NAND gates (U7) to produce an active low enable input for each of the two 1-of-4 Decoder/Demultiplexers (U8). Address bits A11 and A12 are used as the address inputs to U8 to produce Upper and Lower Probe Bank chip select signals. The Upper Probe Bank contains address locations for U18 internal registers, high threshold D/A converter (U23), Stop Counter data and the Pulse Counter (U21, U22). The Lower Probe Bank contains address locations for the Probe Custom Logic chip internal registers, low threshold D/A converter (U20), control register (U17), and the status register (U25). The address map for the Probe I/O Module Interface is located in Table 3-19.

Table 3-19. Probe I/O Module Interface Address Map

ADDRESS	WIDTH	COMPONENT	R/W-
C000x-	(even bytes) (0 through 6)	Probe Delay Chip	(Read/Write)
C000x	(odd bytes) (1 through F)	Probe Logic Chip	(Read/Write)
C0800	(byte)	High Threshold D/A Converter	(Write)
C0801	(byte)	Low Threshold D/A	(Write)
C1000	(word)	External Stop Counter	(Write)
C1001	(byte)	Status Register	(Read)
C1800	(word)	16-bit External Counter	(Read)
C1800	(byte)	Clear External Counter and Delay Chip Latched Registers	(Write)
C1801	(byte)	Control Register	(Write)

Probe Interface

The Probe Interface group block in Figure 3-5 contains smaller specific blocks that contain circuitry for the following:

- o Controlling data input by the Probe.
- o Generating voltages used by the Probe.
- o Controlling and driving the Probe lights.
- o Detecting blown probe fuse.
- o Counting frequency, transitions, or periods with bit counters.

PROBE DATA INPUT

The signal from the Probe tip passes through a resistor divider network on the single-point Probe PCA and the Probe I/O Module PCA. A FET (Q1) buffers the signal before high-speed dual comparator U30 samples the signal. The comparator thresholds are set by programmable digital-to-analog converters (DACs) U20 and U23. The low DAC (U20) generates the low threshold by receiving input data on D00 through D07 from the buffered data bus; the high DAC (U23) generates the high threshold from D08 through D15 of the same bus. The probe data input threshold voltages can be set in 10 millivolt increments by the DACs. The outputs of U30 are converted from ECL (Emitter-Couple Logic) levels to TTL levels before entering the Custom Gate Array Delay Chip (U18).

If the Probe I/O PCA is repaired or replaced, a probe offset calibration is required. This calibration value is stored in an EEPROM on the Main PCA. Any offsets in the FET (Q1) are corrected by adding the calibration value to the U20 and U23 voltage.

THRESHOLD VOLTAGE CALCULATION

The following paragraphs describe how voltages on the Probe I/O PCA and Probe PCA determine the input voltages to U30 and output voltages of U20 and U23. The calculated results aid the technician in determining if the pca components are operating properly. The example below determines U30 output and U20 and U23 input voltages.

STEP 1: Calculation of U20 and U23 multiplier.

A. Attenuation from probe input to U30.
a = R8/(R8 + RSERIES) = 15K/(15K + 100370) = .130
RSERIES = probe series resistance

B. Attenuation from U20 and U23 to U30
b = R51/(R51 + R50) = 511/(511 + 1150) = .307

C. a/b = .130/.307 = .42

STEP 2: Calculation of U20 and U23 output voltage. (TTL level)

LOGIC LEVEL	REAL THRESHOLD VOLTAGE		U20 AND U23 OUTPUT VOLTAGE
Hi	2.4V	* .42 =	1.00V
Lo	2.8V	* .42 =	0.33V

STEP 3: Calculation of U30 input voltage.

LOGIC LEVEL	U20 AND U23 OUTPUT VOLTAGE		U30 INPUT VOLTAGE
Hi	1.00V	* .307 =	.307V
Lo	.33V	* .307 =	.101V

Three choices of probe input threshold are available to the user: TTL, CMOS, and RS-232. To generate a negative threshold from U20 in RS-232 applications, the software sets a bit in the probe custom logic chip (U19) to set the RS-232- signal active. This signal is used to force a negative 3.2 volt threshold on U20. Various voltage threshold levels are presented in Table 3-20.

Table 3-20. Voltage Threshold Levels

TARGET VOLTAGES		REAL THRESHOLD VOLTAGE	DAC OUTPUT VOLTAGE	U30 INPUT VOLTAGE
	TTL			
5.0V	------------------			
	Guaranteed HIGH			
2.6V	-----			
	high or invalid	2.4 volts	1.0 volt	.31 volt
2.2V	-----			
	Guaranteed INVALID			
1.0V	-----			
	low or invalid	0.8 volt	0.33 volt	.10 volt
0.6V	-----			
	Guaranteed LOW			
0.0V	------------------			
	CMOS			
5.0V	------------------			
	Guaranteed HIGH			
3.7V	-----			
	high or invalid	3.5 volts	1.47 volts	.45 volt
3.3V	-----			
	Guaranteed INVALID			
1.2V	-----			
	low or invalid	1.0 volt	0.42 volt	.13 volt
0.8V	-----			
	Guaranteed LOW			
0.0V	------------------			
	RS-232			
30V	------------------			
	Guaranteed HIGH			
3.2V	-----			
	high or invalid	3.0 volts	1.26 volts	0.39 volt
2.8V	-----			
	Guaranteed INVALID			
-2.8V	-----			
	low or invalid	-3.0 volts	0	-0.39 volt*
-3.2V	-----			
	Guaranteed LOW			
-30V	------------------			

* Pulled negative by Q8 and R60.

PROBE OPERATION VOLTAGES

Two voltage levels (regulated +5 volts and -1.2 volts) are produced on the Probe I/O Interface PCA. The +5 volts is used for the Pulse High probe signal and as power for U1. The +12VN (nonregulated) voltage is converted to +5 volts by a +5 volt regulator (U40). Voltage comparator U37 acts as an overcurrent shutdown sensor for the +5 volt supply. A -1.2 volt power supply (Q2) converts -5 volts to -1.2 volts used to produce Pulse Low for the Probe.

FUSE BLOWN DETECTION

Fuse blown detection circuitry for the Probe is located between the probe connector and the Probe Custom Chip. The probe ground fuse (F1), located on the Probe I/O Interface, protects circuitry in case the user incorrectly connects the ground clip to a power supply. Detection for blown fuses is generated by two LM339 voltage comparators (U24) that generate the output Fuse-P.

PROBE LIGHT DRIVE AND CONTROL

The Probe Light Control block contains a 2:1 Line Multiplexer (U9), and a 4-bit Data Latch (U31). The 2:1 Line Multiplexer selects latched/unlatched data. Invalid asynchronous data is filtered by the Filtered Invalid block, which requires that the invalid signal persist for 100 ns before being detected. Synchronous data invalid levels are taken as is on the clock edge. The output of the Filter block is multiplexed with the invalid signal from U31 to become INVALID IN at U19-58 along with the High and Low outputs of U9. The HI IN, INV IN, and LO IN pulses are stretched 50 ms internally within U19 to to become the light drive inputs to Q3, Q4, and Q5.

The three transistors Q3, Q4, and Q5 drive the three logic level indicator lights on the Probe. Each transistor drives one light:

- Q3 for the (green) low logic level light.
- Q4 for the (yellow) invalid logic level light.
- Q5 for the (red) high logic level light.

The input signals to the transistors originate from U19-28, U19-29, and U19-30.

EXTERNAL 16-BIT COUNTER

Two 8-bit binary counters (U21, U22) are cascaded together to form a 16-bit external counter. The 16-bit counter together with a 8-bit internal counter of U19 combine into a 24-bit counter. The 24-bit counter counts transition changes, clock frequency counts, and period counts from data collected by the probe tip.

Clock Module Interface

The Clock Module Interface on the Probe I/O Module Interface PCA contains a Quad ECL-TTL Translator (U28), a Dual 4:1 Line Multiplexer (U16), and a fuse blown detection circuit. The START/START-, STOP/STOP-, ENABLE/ENABLE-, and EXT CLK/EXT CLK- signal lines are ECL (Emitter-Coupled Logic) level outputs of the Clock Module. These outputs are converted to TTL level signals before being introduced to U19. Before entering U19, the ENABLE/ENABLE-, SYNC, EN1, and EN0 signals are combined to form a multiplexed input line to U19-24 via U16 for the purpose of selecting an External Enable. A blown Clock Module fuse detection circuit signals to the mainframe that a Clock Module fuse is blown. Two voltage comparators (U24) detect the blown fuse and generate the blown fuse signal (FUSE-C) to U19.

Custom Delay Chip

The Custom Delay Chip (U18) is one of two Probe Control chips on the Probe I/O Module Interface PCA. The functional block located on Figure 3-5 contains internal components dealing with Probe Input Signal Delay. The function of U18 is to produce high, low, and invalid data signals including CRC data and CRC clock generation. These signals are sent to support chips and to the Custom Probe Logic Chip (U19).

The Delay Chip contains a data multiplexer that can select either the Probe threshold or a presently unused current input U18-5. A FREERUN signal (a 1-kHz continuous square wave) and a input clock is used for internal calibration. The CURRENT input is for future expansion purposes. Once data is past the multiplexer, two separate data paths form the DATA HIGH, the DATA LOW, and INVALID OUT outputs. The Enable Clock U18-19 has a 60 ns delay switchable in or out (0 delay or 60 ns delay). A history and CRC data latch contained in U18 provides valid data (high or low) or the last valid data input for the CRC register in U19.

Functions of U18 include:

- Delaying data high and low from the probe tip input for U31 and U9 to interpret.
- Latching synchronous/asynchronous Hi, Lo, and Invalid Probe Data.
- Generating CRC clock and CRC data signals used by U19 from Enable Clock input.
- Generating INVOUT signal output at U18-34.
- Qualifying CRC Clock Data, either present data or last valid data.

An Invalid signal, which amounts to a lack of valid high or valid low, is generated by the custom delay chip as the INVOUT signal. This is routed through a filter (U6 and associated resistor/diode arrays); the resulting output is termed Filtered Invalid. In asynchronous mode, the invalid pulse must exceed 100 ns in width. This is accomplished by using an RC network to delay the trip point of U6, pin 1 by 100 ns. An invalid input exceeding 100 ns trips this circuit, producing the filtered invalid output. In asynchronous mode, this output is used by both the internal latches and the probe light circuitry. For the RS-232 threshold, Q6 is used to switch in C34, increasing the RC timing and producing a longer filter time of about 2000 ns for the invalid signal. The RS-232- signal from U19 is also used to pull the U20 logic level negative through level shifters Q7 and Q8.

Synchronous invalid constitutes an absence of a valid low or valid high at the clock time.

For accurate probe operation, the delays in the probe system must be calibrated. Before delay calibration can be performed, the software must determine the amount of delay per tap on the delay line internal to the custom delay chip (U18). At power-up or reset, an external 32 MHz clock signal is routed through both the high and low data paths. By choosing differing amounts of delay and counting clock edges, the software is able to compute the amount of delay per internal delay line tap. This data is saved for use in delay calibration.

The clock delay (60 ns) is switched in for negative delays, and the data delay is switched in for positive delays. Calibration is accomplished by adding delays and reading the pca's history latches. Note that any change in the external lights during this process results from pulses being fed through related circuits and has no other significance.

The delay calibration value is computed by the probe calibration procedure. Both the Clock Module and the Probe are used during the procedure, with the Probe tip being pulsed to generate the calibrating clock signal. Delays are adjusted until both the clock (probe tip pulse) and the data arrive at the history latch at the same time. The delay value derived is saved in memory and can then be stored on disk for subsequent use.

Custom Logic Chip

The second of two custom chips on the Probe I/O Module, the Probe Custom Chip, is located on the functional block diagram Figure 3-5. Internal structure and the functions of U19 deal with Probe Data signals, Probe Light drive, counting events, and clock selection. The Custom Logic chip contains the following internal structures:

- Digital Pulse stretcher circuitry for Probe Lights.
- A counter configurable for frequency, period, or transition.
- Pulser control logic.
- A CRC register circuit.
- Start_stop_enable logic for the clock.
- A multiplexer to select the clock.

The Custom Logic Chip supports functions from both the Probe and the Clock Module with different clock-type selection (Pod SYNC, FREERUN, and EXT CLK) determined within U19. CRC data is also calculated by U19.

Predetermined synchronous or asynchronous data selected by the 2:1 Line Multiplexer (U9) on the Hi in, Invalid in, and Lo in signal lines are stretched by U19 to at least 50 ms. The stretched signals become the three light drives for Q3, Q4, Q5.

An 8-bit internal counter (U19) and a 16-bit external counter (U21, U22) perform three counting modes: transition, frequency, and period. These functions count either data high transitions or 8 MHz clock transitions and are controlled as described below:

- Transition Mode: The counter counts data transitions with a software controlled start/stop.

- Frequency Mode: The counter counts the data transitions for a 50-ms period. The software converts this count to frequency by multiplying the count by 20.

- Period Mode: The counter counts the 8-MHz clock from one data high transition to another. The software uses this mode to measure low frequencies, converting the count from period to frequency for display.

CRC data is gathered at the internal CRC register (part of U19). The CRC uses the delayed data and clock signals from U18.

PULSE HI and LO signals for the Probe are generated by U19 to stimulate signal lines in the UUT. To produce pulser signals, a logic low from an internal clock logic register plus a Hi, Lo, or software- generated clock enter a pulse logic register. The two outputs of the pulse logic register are the PHI and PLO signals on U19, pins 10 and 26, respectively.

The Probe Logic Chip contains an internal selection system to provide the enabled clock for U18 and the 16-bit Stop Counter, and to provide a SYNC Pulse to an externally-connected oscilloscope via a BNC connector located on the mainframe back panel. EXT START and EXT STOP from the Clock Module, and STOPCNT- are combined to enable the internal clock signal input to the internal Clock Logic Register of U19. The selected enable, SYNC-, FREERUN, and EXT CLOCK from the Clock Module combine to enable the internal Clock Logic Register, which generates the enabled clock outputs CCLK and CCLK-.

When the probe/pulser is active, the internal clock logic requires the opposite edge of the pulse to start the clock; in a non-pulsing condition, the clock starts on the first selected edge to provide an edge (before the clock edge) to start the probe output pulse. The clock is inverted internally in U19 when the pulser is active. The CSEL output is high when the clock has been inverted internally, forcing pins 3 and 6 of U2 to invert the clock outputs again to provide the correct signals to U18 and the sync output.

Stop Counter

The Stop Counter is a series of four presettable 4-bit binary up/down counters (U26, U32, U33, U34). Each counter has four parallel data inputs to count the total 16 data bus lines. STOPCTCK (Stop Count Clock) from U2-6 is the clock pulse for the counter chips. The STOPCTLD- (Stop Count Load) input to U26 (U32-, U33-, and U34-generated from U13-11) overrides counting and loads the data present on the parallel data lines into the counter. Each counter chip has a maximum count output that is gated by U38. When all of the counters reach maximum count, the output from U38 puts an active low on the data input of a dual D-type flip-flop (U10). U10 then provides the STOPCNT- input for U19-20 on the next clock pulse. RDMISC- (Read Miscellaneous) from U11-8 enables the U25-10 output, which is bit 1 of the Status Register, to read the status of the Stop Counter. The Stop Counter is programmable for 1 to 64K counts and is used to control SYNC history latches and CRC registers.

I/O Module Interface Connector

The I/O Module Interface Block located on the Probe I/O Module Interface PCA, shown in Figure 3-5 of the functional block diagram, contains three parts.

- o The connector and related components for the I/O Connector PCA connector.
- o The -VDRV Regulator for the I/O Module Pattern Drive.
- o The Overcurrent Detection Circuitry for the I/O Module Pattern Drive.

The I/O Connector PCA Connector interfaces data lines D00 through D15, address lines A01 through A12, and control lines between the I/O Module and the mainframe.

The 16 data lines from the I/O Connector PCA to the Probe I/O Module Interface PCA connect to the uP Data Bus with the low eight data bits direction controlled by an Octal Bus Transceiver (U39). The transceiver's data flow direction is controlled by an RDSL (Read Select) signal generated from PS5-, LDS-, and READ-. The upper eight data bits are unused. The address lines and four control lines (R/W- (Read/Write), FGATE (Frequency Gate), ODRESET (Over Drive Reset), and SEL- (Select)) are buffered by line drivers to maintain signal levels for communication with the I/O Modules and the I/O Connector PCA. The STROBE signal is generated for the I/O Modules by gating NDS- (New Data Strobe) with PS5- (Peripheral Select 5). The STROBE signal is sent to the I/O Connector PCA for further processing before reaching the I/O Module. Outputs from the I/O Module include the two interrupts DCE and IOGEN. The sense + and sense - signals are sourced from the +VDRV voltage regulator on the I/O Connector PCA.

I/O MODULE -VDRV VOLTAGE REGULATOR

This regulator provides a -0.85V output with a high short term current sinking ability (greater than 2A) and a long term current sinking capability of 250 mA. Overload detection is also provided. Figure 3-6 presents a simplified schematic of the -VDRV Voltage Regulator.

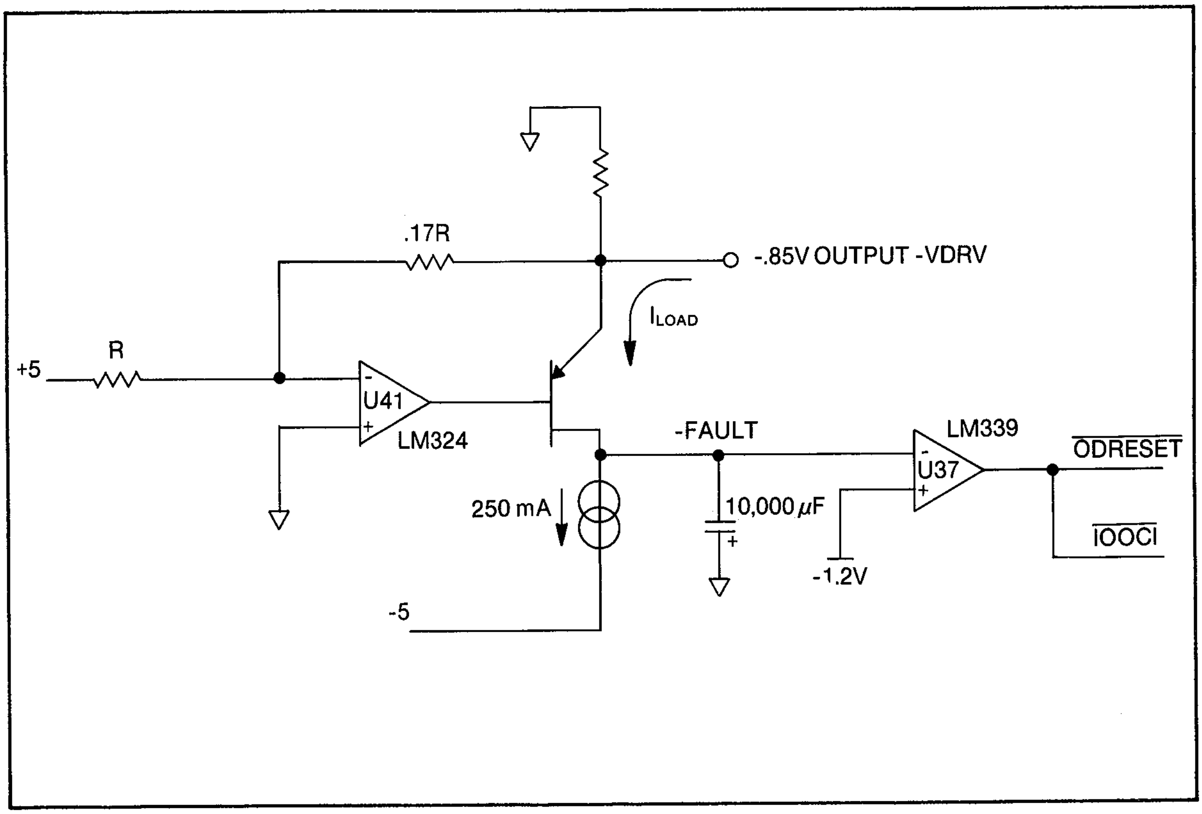


Figure 3-6. -VDRV Voltage Regulator Simplified Schematic

The regulator uses an inverting op amp circuit. With a gain of -0.17, the op amp provides -0.85V output from the 5V input. The PNP power transistor (implemented as PNP/NPN compound Q9/Q10) is configured as an emitter follower and is used to provide increased current sinking capability. The collector supply is a 250 mA constant current sink. Dual Diode CR10 is used to return feedback to U41 and to clamp U41's output during low current situations.

When the current demand is low (less than 250 mA), the current sink saturates, and the -FAULT signal is at about -4.5V. If a high current transient appears, the current sink (Q11 and part of op amp U41) turns on, and 250 mA flows into the -5V supply. The rest of the current flows into the 10,000 uF capacitor, slowly charging it up. Because this capacitor is in the collector circuit of the power transistor, the regulator's output remains unaffected while this voltage is rising. If the current demand is high enough or long enough, the capacitor charges to above -1.2V. At this level, the LM339 comparator trips, generating an

IOOCI- interrupt and forcing the control line ODRESET- low. This in turn shuts off the I/O module overdrivers, limiting the current. The time constants of the circuit are set so that 2A can be sunk for 10 ms without affecting the regulated -VDRV output or generating an overcurrent fault.

I/O MODULE OVERCURRENT DETECTION

I/O Module overcurrent conditions are detected from either of two sources: the +VDRV supply or the -VDRV supply. The +VDRV regulator is situated on the I/O Connector PCB. Current sense from that supply is provided via the sense+ and sense- signals, which are differentially amplified by a section of U41 and compared by a section of comparator U37 to a reference. This reference is switchable, via the LO-CURRENT- line, to one of two settings. The low setting, commanded when LO-CURRENT- is low, sets a reference of about .4V, which in turn sets an effective current limit of about 200mA. The high setting sets the reference to about 4V, which sets the current limit to about 2A. This high current setting is guaranteed by software to never be active for more than 10 ms, (with a max duty cycle of 1%). R73, C18, and CR12 slow down the output of the differential amplifier so that it does not trip on transients.

A -VDRV overcurrent condition is detected by another section of the U37 comparator. These two comparators are "wire ORed" together. If either one detects a fault, both of their outputs goes low. This fault causes the ODRESET- line to go low, which turns off the I/O Module overdrivers, thus removing the overcurrent fault. At the same time, flip-flop U27 is clocked, making IOOCI- go active and generating an interrupt. This interrupt can be cleared by writing line IOCLRINT- low; (WRITE @ C1801: bit 1 = 1 says clear interrupt; bit 1 = 0 says release interrupt).

Miscellaneous Functional Blocks

The Probe I/O Module Interface PCA has two functional blocks for the specific purpose of interfacing with external equipment: the SYNC Pulse Isolation block and the Footswitch Connector (J4). Two other functional blocks (Data Bus Buffers, Status Register, and Control Register) support operations for probe control.

SYNC PULSE ISOLATION

SYNC Pulse Isolation uses an optoisolator and an earth-referenced divider to provide an earth-referenced TTL level SYNC Pulse (isolated from the 9100A/9105A) to an oscilloscope. Inputs to this block include an earth referenced +5 volts and a clock pulse from U2-6. The resulting external trigger output is available at a BNC connector on the rear panel.

FOOTSWITCH CONNECTOR

The Footswitch Connector (J5) is a standard telephone jack that connects to a normally open switch. The switch is used as an external event recognizer. A test program can use such a switch to make a program depend on an external event, a manually generated signal, or a limit. Access to J5 is on the right side of the mainframe labeled (EXT SW). A switch closure is detected by the COLUMN9 and ROW7 signals; these signals are sourced from the keypad scanning circuitry on the Display PCA.

DATA BUS BUFFERS

Data Bus Buffers (U35, U36) permit data transfer from the microprocessor data bus to a buffered data bus. Instructions from the microprocessor to the ICs on the Probe I/O Module Interface PCA move along the microprocessor data bus through J6 to U35 and U36. The data moves through the Data Buffers onto the buffered data bus to the required ICs.

STATUS REGISTER

The Status Register (U25) monitors single data bits on the Buffered Data Bus to detect I/O Overcurrent Interrupts, Probe Power, Stop Counter Status, and Pulse-Transition Counter Carry-Bit Status. The Status Register is a quad 3-state buffer (U25) connected to the output of the circuit and the data bus. U25 is read only, and Figure 3-7 summarizes the status bits. The Status Register output to the data bus is enabled by the RDMISC- (Read Miscellaneous) signal from U11, pin 8.

```
ADDRESS R/W-   READ BOARD STATUS BITS   7 6 5 4 3 2 1 0
C1001
               Not Used                 (bits 7-4)
               I/O Overcurrent Interrupt          (bit 3)
                 1 = no interrupt active
                 0 = active overcurrent interrupt
               Probe +5 Power                     (bit 2)
                 1 = 5V power present
                 0 = Power shutdown
               Stop Counter Status                (bit 1)
                 1 = Stop counter not at max count
                 0 = Stop counter at max count
               Transition Counter Carry Bit       (bit 0)
                 1 = Carry bit set
                 0 = Carry bit not set
```

Figure 3-7. Status Register Bit Breakdown

CONTROL REGISTER

A 4-bit Write-Only Control Register (U17) generates the STOPCTENA- (Stop Counter Enable), IOCLRINT- (IO Clear Interrupt), EN0 (Enable 0), and EN1 (Enable 1). The Control Register decodes data bits 00 through 03 of the Buffered Data Bus to generate the output signals. Data bits 02 through 03 determine different ENABLE combinations. Data bit 01 either clears or allows an I/O Overcurrent Interrupt, and data bit 00 enables or disables the Stop Counter. Figure 3-8 represents the data bit breakdown for the Control Register.

```
ADDRESS R/W-   WRITE CONTROL DATA BITS     7 6 5 4 3 2 1 0

C1801    0     Not Used
               External Enable Mux
                       Bits  3  2
                             0  0 = Pod SYNC
                             0  1 = Pod SYNC Qualified
                                    by Enable
                             1  0 = Enable
                             1  1 = Pod SYNC Qualified
                                    by Enable-
               Clear I/O Overcurrent Interrupt
                       1 = Force clear
                       0 = Allow interrupt
               Stop Counter Enable
                       1 = Enable stop counter operation
                       0 = Disable stop counter operation
```

Figure 3-8. Control Register Bit Breakdown

I/O CONNECTOR INTERFACE

Overview

The I/O Module Connector PCA provides the interface for the I/O Module to the 9100A/9105A. The I/O Connector Interface shown in Figures 3-1 and 3-2 is a vertically-mounted PCA that plugs into the Probe I/O Module Interface PCA, which connects to the Main PCA. Up to four I/O Modules can be connected to the 9100A/9105A. The I/O Connector and the Probe I/O Interface PCAs buffer the 68000 microprocessor address and data bus to send data out to the modules. The PCAs also contain the I/O Module overdriver power supplies and circuitry to gather and distribute control, data, and address signals, event detection, and operational power for each I/O Module.

Power Supplies

There are two power supplies for the I/O Module, one at 5V, (called +VDRV), and one at -0.85V (called -VDRV.) The +VDRV power supply is a linear supply derived from the +12V supply. Current is sensed by measuring the voltage across the .47 ohm resistor. This voltage is measured on the Probe I/O PCA from the SENSE +/- lines.

Gross overcurrent protection is provided by an LM338 voltage regulator (U4). Normal overcurrent protection is provided via an overdriver shutdown line, (ODRESET-). This line instantly turns off the overdrivers, removing the overcurrent fault. An overcurrent fault is triggered if current exceeds two programmable levels: 200 mA, and 2A. The 200 mA level is the power-up default, and is only changed to the higher level during pattern drive. The 2A level is a short term (10 ms 1% duty cycle) maximum amount of current for all four I/O Modules. The overcurrent level is controlled by the (LO_CURRENT) control line produced by DTIO #2 (U7) on the Main PCA. If the 200 mA and 2A thresholds are violated, an I/O Overcurrent Interrupt (IOOCI) is generated. Simultaneously, all of the overdrivers on all of the I/O Modules are shut off.

The 10,000 uF capacitor is part of the -VDRV regulator, which is covered in the Probe I/O Module Interface discussion.

I/O Module Connector PCA Contents

The I/O Connector PCA contains four DB-37 vertically-mounted connectors that are accessible on the rear panel of the mainframe. On the other side of the PCA is a voltage regulator (U4) with supporting capacitors (.01 uF, 1000 uF), and the 10,000 uF capacitor used in the -VDRV regulator. The connector to the Probe I/O PCA (J1) supplies all I/O Module power, event detection, address, data, and control signals to the I/O Module.

The address bus containing A01 through A11 and the data bus containing D00 through D07 distribute address and data lines to each connector with A08 through A11 used to determine the +/- STROBE for the selected I/O Module. When the STROBE signal is divided between each module connector, the signal has PS5 and "hot bits" decoded in the signal. The Pod +/- SYNC signal used for timing with the Probe and I/O Module is also distributed to the four I/O connectors by a quad ECL-TTL translator (U2).

The DCE- and IOGEN- interrupts from each module are input to a dual 4-input NAND gate (U3). The outputs of U3 are connected to J1 and sent to the mainframe for further processing. The MODSEL- line is connected through jumper J8 to IWAIT3-. This forces I/O Module bus communications to occur with three wait states, allowing for reliable bus operation over long cable lengths.

PROBE/PULSER

Overview

The Single-Point Probe/Pulser is a 9100A/9105A interface device used to measure portions of the UUT PCA not accessible to the I/O Module. The Probe/Pulser measures inputs up to 40 MHz and generates stimulus pulses at up to a 50 kHz rate. A 1-bit-wide data channel provides input measurement and output stimulus capabilities. Features available through use of the Probe/Pulser include: 16-bit cyclic redundancy checks (CRC), clocked and asynchronous level history, and frequency measurements. The Probe/Pulser instrument is divided into four functional blocks:

- o Sensing Block (Probe)
- o Pulsing Block (Pulser)
- o Level Indicator Block (Lights)
- o Switch Block (Switch)

Refer to Figure 3-9 for the functional block diagram of the Probe/Pulser.

Probe

The Probe measures signals from the UUT, with the Probe tip making a single-point connection on the UUT board. The UUT signal is routed through Probe circuitry and the Probe cable to the 15-pin Probe connector on the right side of the mainframe. The Probe functional block contains both the common ground and the one-bit data channel for the UUT.

PROBE TIP INPUT

Signals enter the Probe Tip, passing through R1 and R2. These two resistors in conjunction with R8 on the Probe I/O PCA form a resistor-divider compensation network to match the impedance of the Probe cable. R9 is a pull-up resistor to pull the Probe to a tri-state condition when no other inputs are connected. The input signals exit the Probe via J1-14 and enter the Probe I/O Module Interface PCA. The speed of the input signals must meet the criteria listed in Figure 3-10 to be captured by the Probe Data Channel.

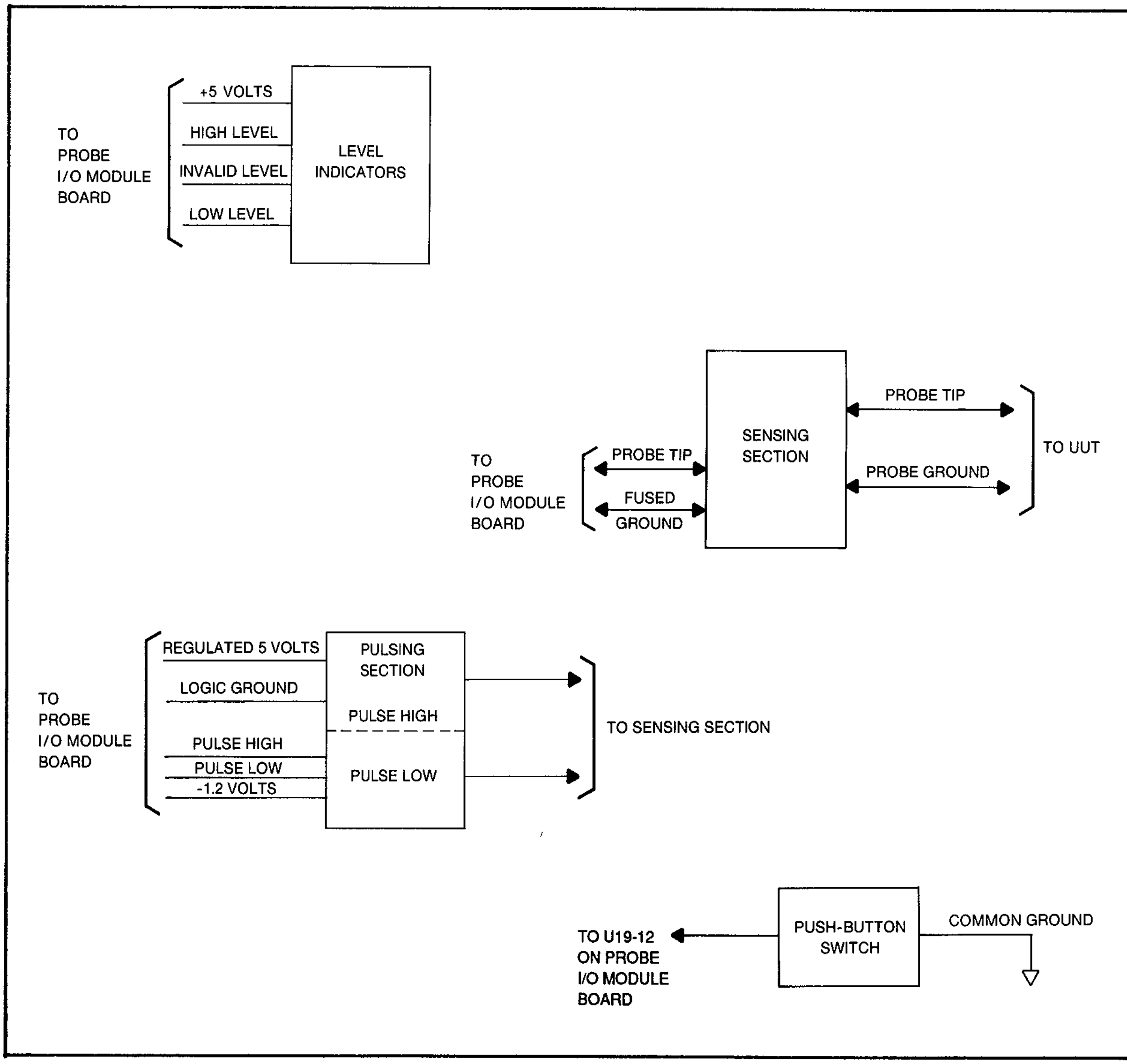


Figure 3-9. Probe/Pulser Functional Block Diagram

Square Wave Pulse

Asynchronous Mode → High > 12.5 ns
Tri-State > 100 ns +/- 20 ns (TTL or CMOS)
> 2000 ns +/- 400 ns (RS-232)
Low > 12.5 ns

Synchronous Mode → Tri > 20.0 ns

Figure 3-10. Probe Speed Specifications

COMMON GROUND CLIP

The Common Ground Clip connected to the Probe/Pulser clips to the UUT common ground. At the point where the ground connects to the Probe/Pulser, the common lead screws in to make connection. The ground line passes directly through the instrument to J1-9. If the user misconnects the Common Clip, a Probe Fuse located next to the Probe Connector on the mainframe provides protection from power supply shorts or other overcurrent conditions. The Ground Clip must be connected to the UUT to ensure a short return path for pulsing current.

Pulser

The Pulser stimulates input signals for checking output data on the UUT. The Pulser drives a short duration high current level either high or low at a node being tested. The output pulse can be toggled between High and Low or turned off completely (Tristate). During the low pulse, current is supplied by Q4. A high logic level on the PULSE LO signal line turns on Q4, driving the Probe tip low through CR4. C4 supplies instantaneous current for the low pulse. When the Pulse low signal line is off (logic low), Q3 conducts to turn off Q4 quickly. CR4 prevents the Probe tip from being pulled high at this time. The -1.2 input voltage from the Probe I/O Module (J1-13) is used to generate the low pulse.

On the PULSE HI signal line, the logic high into U1-5 inverts to a logic low to turn Q1 on, driving the probe tip high through CR1. C2 is a speed-up capacitor that drives Q1 into saturation, and C3 supplies instantaneous current for the high pulse. A logic low on the PULSE HI line turns Q1 off; Q2 is turned on, and CR1 prevents the Probe tip from being pulled low. The regulated +5-volt supply is used to generate the Pulse High signal and supplies power to U1. Both pulse levels drive the voltage at a specified current for the time shown in Table 3-21.

The Probe pulser exhibits a certain delay in reacting to the synchronous inputs. The maximum propagation timing from synchronous input to pulser action is listed in Figure 3-11.

Pod Sync Falling Edge to →	→ Pulse High Rising Edge (23 ns max)
	→ Pulse Low Falling Edge (22 ns max)

Figure. 3-11. Probe Response Timing Specifications

Table 3-21. Typical Probe Pulser Amplitude

LEVEL	VOLTAGE	CURRENT
High	> 3.5V	200 mA for less than 10 us (1% duty cycle)
	> 4.0V	5 mA continuously
Low	< .8V	200 mA for less than 10 us (1% duty cycle)
	< .4V	5 mA continuously

The minimum pulse widths of the Pulser are shown in Table 3-22.

Table 3-22. Pulser Pulse Width

MODE	WIDTH
Pod Sync	> 50 ns
Free Run	2 us @ 1 kHz pulse rate
External	> 50 ns

Level Indicators

There are three level indicators on the Probe. The level indicators are used to indicate what logic levels have been encountered. The indicators have the following meaning:

- Red: A valid high signal was encountered.
- Yellow: An invalid signal was encountered.
- Green: A valid low signal was encountered.

The logic indicators are driven by a circuit on the Probe I/O PCA that stretches the pulses to a minimum length of 50 milliseconds.

LOGIC LEVEL MODES

The lamp logic can display either in a synchronous or asynchronous logic mode. A writable register in the Probe Custom Logic Chip on the Probe I/O PCA chooses either synchronous or asynchronous mode. The choice is hardware independent of the SYNC Mode of the CRC and other clocked latches. Asynchronous information is displayed when SYNC is set to FREERUN, and all other SYNC modes display the last synchronous data.

LEVEL INDICATOR OPERATION

The three level indicators are driven by three open-collector transistors (Q3, Q4, Q5) on the Probe I/O Module PCA. Three resistors (R11, R12, R13) are connected to the lights to maintain keep alive current flow in the off condition to increase bulb life.

Push Button Switch

A push button located on the Probe allows the user to indicate when the Probe is in place and ready to perform a "read probe". When the user presses the push button, an interrupt is generated by the Probe I/O PCA. The interrupt is shared by the fuse-monitoring circuits and thus requires that a status register in the Probe Custom Logic chip be polled to determine the origin of the interrupt.

CLOCK MODULE

Overview

The Clock Module is an external unit that is plugged into the right side of the mainframe. When used in conjunction with the Probe, the Clock Module samples external events (start, stop, clock, and enable) that are necessary in gathering signatures from the UUT to synchronize data input and output through the Probe.

Clock Module Operation

Four comparators (U1A, U1B, U2A, U2B) are used, with respective start, stop, clock, and enable input thresholds provided by the Probe I/O Module PCA. The inputs go through a divide-by-2 resistor-divider network to the comparators. The other input (0.8V) to the comparator is provided by the Probe I/O Module PCA, giving a threshold of 1.6 volts for external signals. The resulting balanced ECL signals are routed through J6 to the Probe I/O Module Interface. An external ground connection is also provided, with a user-accessible fuse (F1) protecting the circuit in case of inadvertent contact of the ground lead to the power source.

The balanced ECL signals from the Clock Module are converted to TTL level signals on the Probe I/O PCA before being introduced to the Custom Probe Logic chip (U19). A detection circuit is used to sense a blown fuse in the Clock Module. The outputs from the Clock Module are Start, Stop, Clock, and Enable. The Enable signal is multiplexed by the selection multiplexer (U16) signal lines; Pod SYNC, Enable ANDed with Pod SYNC, or inverted Enable ANDed with Pod SYNC produces the EXT ENABLE signal to U19-24.

Clock Module Speed

The clock module timing specifications listed below are valid for all signal lines into the pod.

- Maximum Repetition Rate: 40 MHz square wave
- Minimum Pulse Width: 12.5 ns

MULTI-FUNCTION INTERFACE

Overview

The Multi-Function Interface (MFI) PCA supports peripheral systems for use with the 9100A. A Small Computer System Interface (SCSI) and a Real Time Clock are supported as standard features for the 9100A. A version of this pca (Real Time Clock only) is optional in the 9105A.

Addresses

The MFI Card plugs into J6 (the MFI Card Connector) on the Main PCA. The card is allocated the address space 0B0000 through 0BFFFF. A PAL (U3) on the MFI Card divides the applicable address space among the installed peripheral systems. Line FC2 qualifies these addresses, allowing access only from System Mode.

Clock

The Real Time Clock consists of clock chip U9, 32.768 kHz crystal Y1, and a lithium-battery backup backup circuit centered on B1. A DTACK generator (U10) provides the extended read and write cycles required by the clock. Test point TP3 facilitates monitoring of crystal oscillator Y1. Clock U9 contains internal battery-sustained RAM. The clock is addressed through even bytes at addresses B1000 - B1020.

SCSI

The SCSI (Small Computer System Interface) is structured around a 5380 controller chip (U2 on the MFI PCA). Generally, U2 handles hardware and software interfacing between the 9100A and the SCSI bus. On the 9100A, the bus accommodates a hard disk and hard disk controller accessed through the internal SCSI connector (J2); the hard disk and SCSI circuits are not available with the 9105A. The external SCSI connector (J3) provides SCSI bus connection for additional devices. Controller chip U2 is mapped to the 16 odd addresses B1001 through B101F.

VIDEO

The separate Video Controller PCA supports the Monochrome Monitor or a color monitor. It is supplied with the 9100A Programmer's Station. The Video Controller PCA is available with the 9105A as an option. Note that the video system is character-mapped; in other words, a specific video RAM address maps into a physical location on the monitor screen.

Video Controller

The 9100A Video Controller PCA uses the 2674 Advanced Video Display Controller (AVDC), U1, along with the 2675 Color/Monochrome Attributes Controller (CMAC), U2. The 2674 (AVDC) generates the vertical and horizontal timing signals necessary for the display of data on a CRT monitor. The 2674 is programmed with terminal setup information, providing cursor, blanking, and clock signals to the CMAC. The AVDC is assigned address space 0F0000 through 0FFFFF. In time with horizontal (HSYNC) and vertical (VSYNC) signals, the AVDC addresses Video RAM (U3 and U4) and the Character PROM (U5) on lines DADD00 through DADD11. By using the ASCII codes supplied by the microprocessor (and stored in Video RAM) and the correct display character data stored in the Character PROM, this sequencing yields display characters.

Video RAM

U3 and U4 provide two kilobytes of static video RAM. When addressed over the main address bus (AA01 through AA10), Video RAM is used to store ASCII character codes supplied by the microprocessor over the main data bus (DB00 through DB15). Video RAM uses address space 0E0000 through 0EFFFF.

Video Control sequentially samples these addresses using lines DADD00 through DADD11 and generates display characters using the ASCII codes found at these addresses and the corresponding display character information found in the Character PROM (U5).

Video RAM is shared by both the mainframe processor and the video-generating circuitry. The ASCII codes for display characters are stored in memory at the same addresses used by the Monitor. This memory mapping allows for efficient updating of data on the CRT. Figure 3-12 demonstrates display address mapping.

```
0E0002, 0E0004, ......................0E00A0
  .
  .
  .
  .
  .
  .
  .
0E0E62, 0E06B4, ......................0E0F00
```

Figure 3-12. Video Display Address Mapping

The video RAM, which resides in a 4K-byte memory space, supplies 2K words for storing characters (1920 words are needed by the 24 lines by 80 characters per line). Both the microprocessor on the Main PCA and the AVDC on the Video Controller have access to video memory; the Main PCA is allowed only to write to video memory. Video control circuitry synchronizes Video and Main PCA requests for memory.

Each displayed character resides in one word of memory, divided into two bytes. Use of the high (or attribute) byte differs between color operation and monochrome operation. The low (or character) byte does not differ between operating modes. Figure 3-13 illustrates the overall data format.

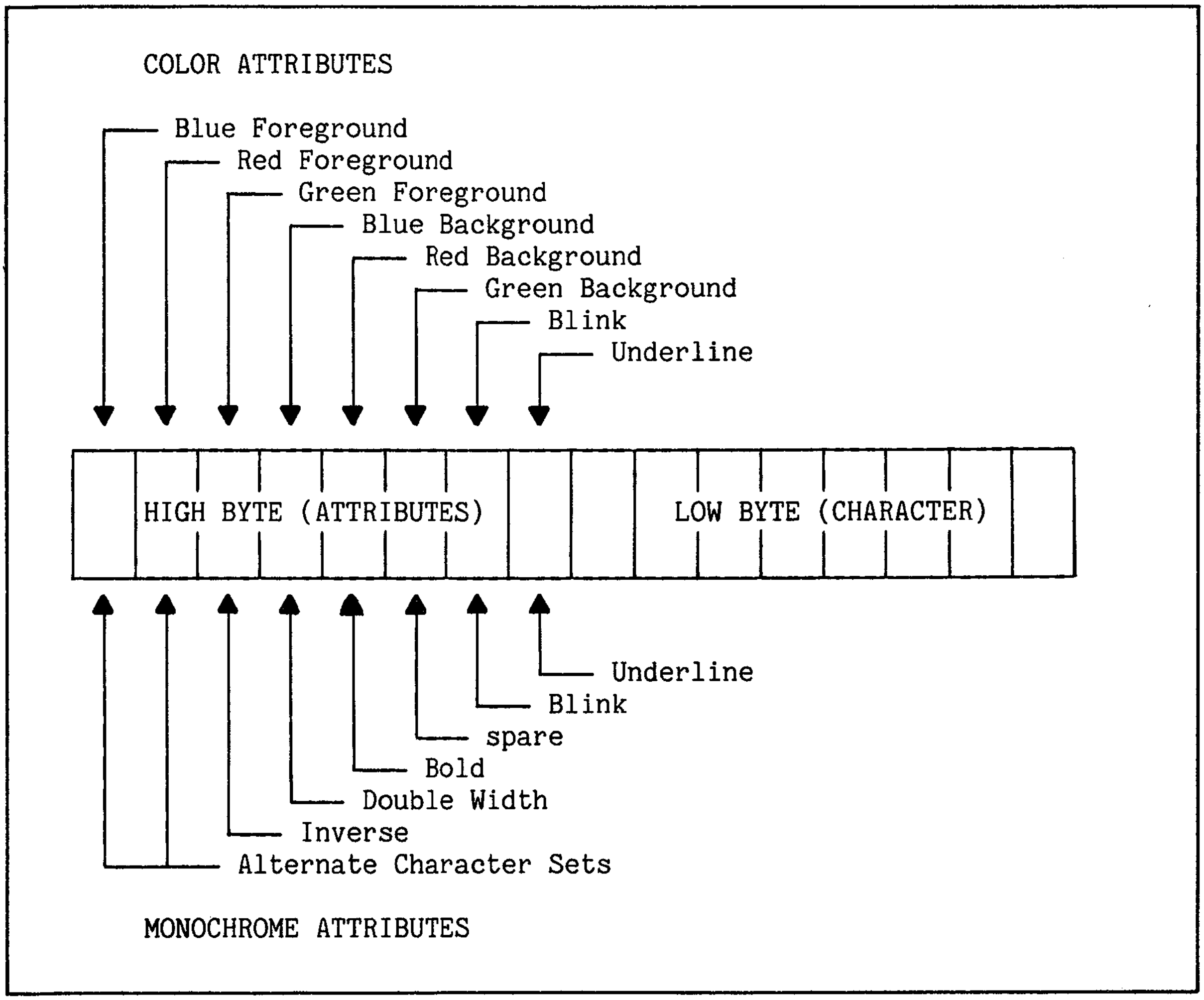


Figure 3-13. Video Character Data Format

The eight registers controlling the video display are selected by the processor using address lines A1, A2, and A3. In addition, line A4 can be high or low for register selection in color mode, but must be high for register selection in monochrome mode.

Outputs to the Monitor include horizontal and vertical sync signals (positive polarity, TTL levels) for both monochrome and color operation. Video data is output as positive white analog levels in monochrome operation or as RGB TTL levels in color operation.

The isolated output allows the mainframe to remain isolated from the earth-grounded monitor. All color and synchronization signals pass through high-speed opto-isolators (U28 - U31). For monochrome output, red and blue output channels are combined to provide high and low intensity signals. Buffer U27 sets the output voltage level, as determined by the red/blue signal intensity encoding. With a color monitor, +5V dc is provided by an earth-grounded power supply on the Main PCA. Otherwise, power from the monochrome monitor is used for enhanced noise immunity.

MONITOR

A separate Monitor can be used with the 9100A Video Controller. A 12-inch monochrome version is available from Fluke. This unit includes a power supply, a CRT, and CRT drive circuitry. Video timing functions are performed by the Video Controller and are not part of the Monitor.

The monitor power supply, which is not manufactured by Fluke, is a switch mode supply that operates from an unregulated 90 to 132V or 180 to 264V ac line voltage and generates the following regulated voltages:

- +12V dc +/- 5%
- -12V dc +/- 10%
- +5.0V dc to +5.1V dc

A color monitor can also be used. See "Color Monitor Specifications" in Section 2 for either the Fluke monochrome monitor or color monitor specifications.

PROGRAMMER'S KEYBOARD

The Programmer's Keyboard is a full ASCII keyboard with additional cursor control and special function keys. Key press codes are sent at 1200 baud in a standard asynchronous format of one start bit, eight data bits (LSB to MSB), and two stop bits. The keyboard buffers up to 31 key codes, at which time the buffer will be filled and subsequent key presses are lost.

The Programmer's Keyboard attaches to the ASCII Keyboard Connector (J10) on the Main PCA. A DUART-Timer-I/O (DTIO#2), U7, provides the Main PCA interface for keyboard signals. The ASCII characters are received as the RxDA input at U7-35.

I/O MODULE

I/O Module Overview

The I/O Module is a device that adds multiple lines of input/output capability to the 9100A/9105A mainframe. The I/O Module has the capability to take CRCs, measure frequency or take event counts, and record logic levels. These measurements can be done simultaneously on up to 40 lines per I/O Module. It is also possible to synchronize the data gathering to the 9100A/9105A uP Pod or to external events using the I/O Module external clock, enable, start, and stop lines. In addition, the I/O Module has the ability to "overdrive" dynamic patterns or static levels onto any of its lines for use in testing devices that cannot be stimulated by the uP Pod. The I/O Module is capable of reading or writing a 40-bit word, and it provides breakpoint capability by generating an interrupt when the data on the inputs equals a programmed value. Input thresholds for each module are selectable between "TTL" and "CMOS" levels. Up to four I/O Modules may be connected to the 9100A/9105A mainframe. The I/O Module consists of seven functional blocks. See Figure 3-14 for a functional block diagram of the I/O Module.

Each of these blocks is described in more detail in the paragraphs that follow:

- Bus Interface Functional Block
- Custom Chip Functional Block
- Clock and Enable Mux Functional Block
- General Control Latch Functional Block
- Connector Code Functional Block
- Input Protection/FET Output Block
- I/O Module Top PCA Functional Block

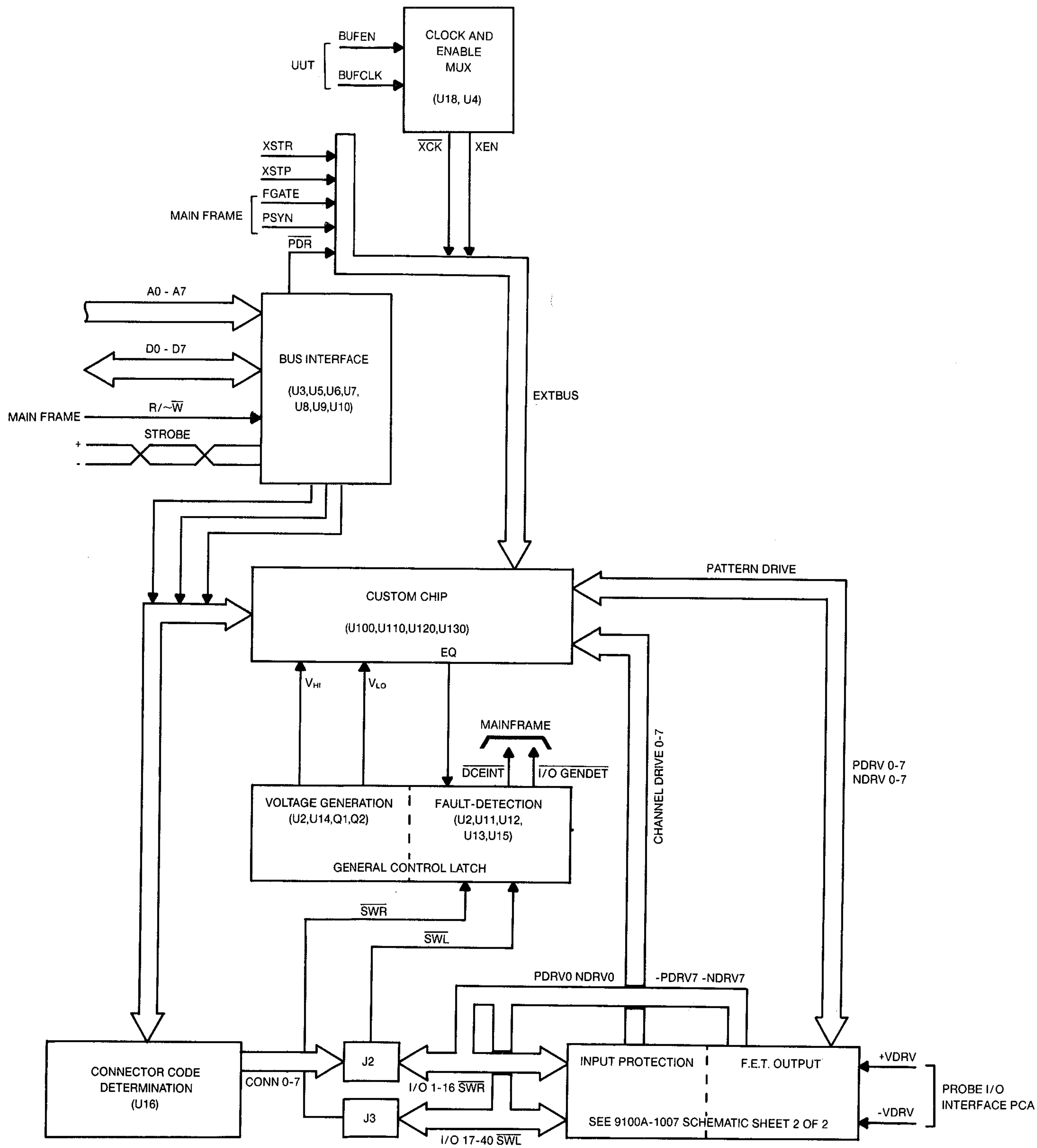


Figure 3-14. I/O Module Functional Block Diagram

Bus Interface Functional Block

OVERVIEW

The bus interface block connects the 9100A/9105A microprocessor bus to the I/O Module. The I/O Module is a memory-mapped device, with all control performed by writes to the I/O Module memory space. A control bus enters the I/O Module on connector J1 and consists of the following lines:

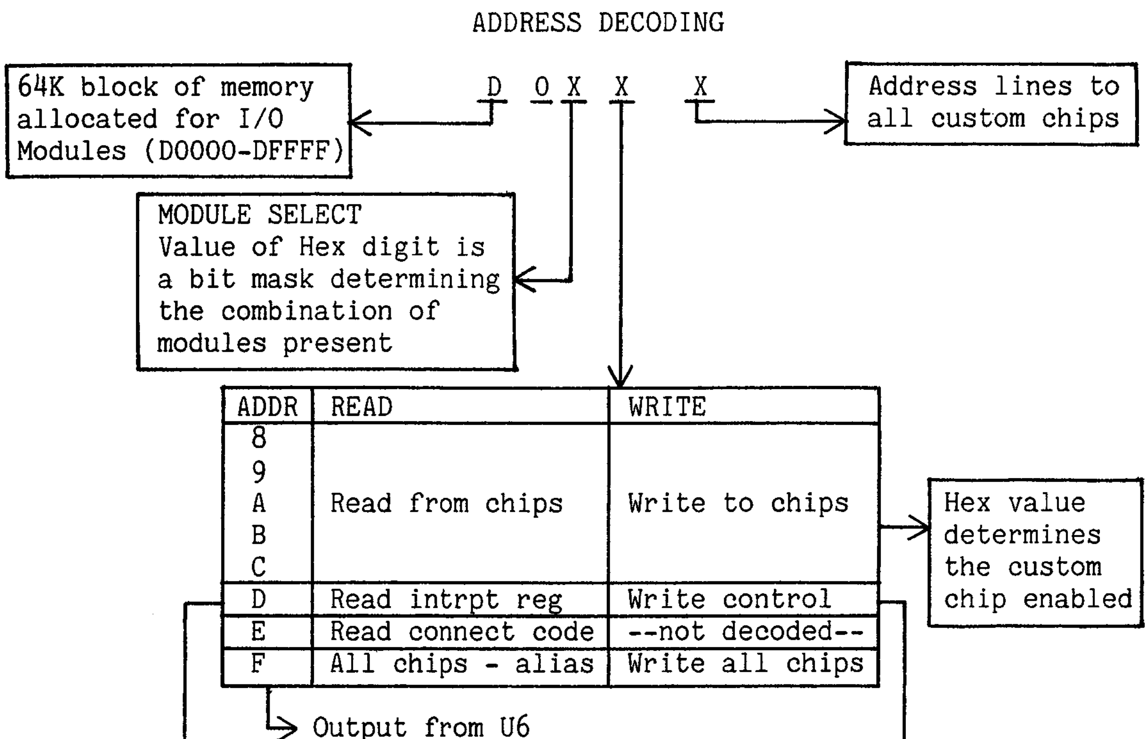
- Seven address lines: A01 through A07
- Eight data lines: D00 through D07
- Two differential strobe lines: STROBE+, STROBE-
- One control line: R/W-

The two strobe signals, which are sent up the cable on a twisted-pair as differential ECL signals, are the key to the clean bus interface. They are translated by U9 into the STROBE- signal. As sent by the mainframe, the STROBE- signal already has some amount of address decoding done in it; STROBE- for any particular module will only be active on accesses to addresses DXXXX, with A0 = 1, and with the proper "hot bit" identifying the module. (See the paragraphs on addresses for more information on hot-bit decoding). STROBE- is the key signal used to qualify all of the bus activities and is used by U7 to latch the addresses and R/W- and to enable the data bus buffer. The STROBE- signal, in conjunction with the latched version of R/W- generates the read strobe (RD-) and the write strobe (WR-). The STROBE- signal and the decoder U6 generate the chip select signals: CS0 through CS4, ADD-, and ADE-.

The following paragraphs explain how the I/O Module address is broken down and what the hex digits signify. I/O Module selection is described with a figure showing which I/O Module(s) are selected. A timing diagram shows typical waveforms during a read and write cycle. The process of enabling the I/O Module custom chip(s) is also described.

ADDRESSING

Memory reserved for I/O Module control occupies addresses D0000 through DFFFF. Out of this 64K-byte block, four I/O Modules can be addressed. Lower Data Strobe, (LDS-), is used to qualify all I/O Module addresses; thus A00 is effectively a 1. Addresses within this space using Upper Data Strobe (UDS-) are unused. Figure 3-15 shows a summary of I/O Module address decoding. Figure 3-16 provides an addressing example.



The bits of the interrupt register are read to monitor interrupt and general I/O Module status. The bits are:

BIT	DESCRIPTION
7	Threshold status
6	Clk mux status
5	Enable mux status
4	Ground (0)
3	Fuse blown
2	Push button (right)
1	Push button (left)
0	DCE (Data Compare Equal)

The bits of the control register are written to reset interrupts or to perform general control functions. The bits are:

BIT	DESCRIPTION
7	Threshold (1=TTL)
6	Clk mux (0=XCLK)
5	Enable mux (0=EXTENA)
4	--not used--
3	Clr fuse blown (0=clr)
2	--not used--
1	Clr gen intrpt (0=clr)
0	Clr DCE intrpt (0=clr)

Bits 5 and 6 in the control register select the signal that appears on the XEN and XCLK lines, as follows:

CLKMUX	ENAMUX	XEN	XCLK
0	0	BUFENA	BUFCLK
0	1	PSYN	BUFCLK
1	0	BUFENA	CALCLK1
1	1	PSYN	CALCLK2

Figure 3-15. I/O Module Address Decoding Summary

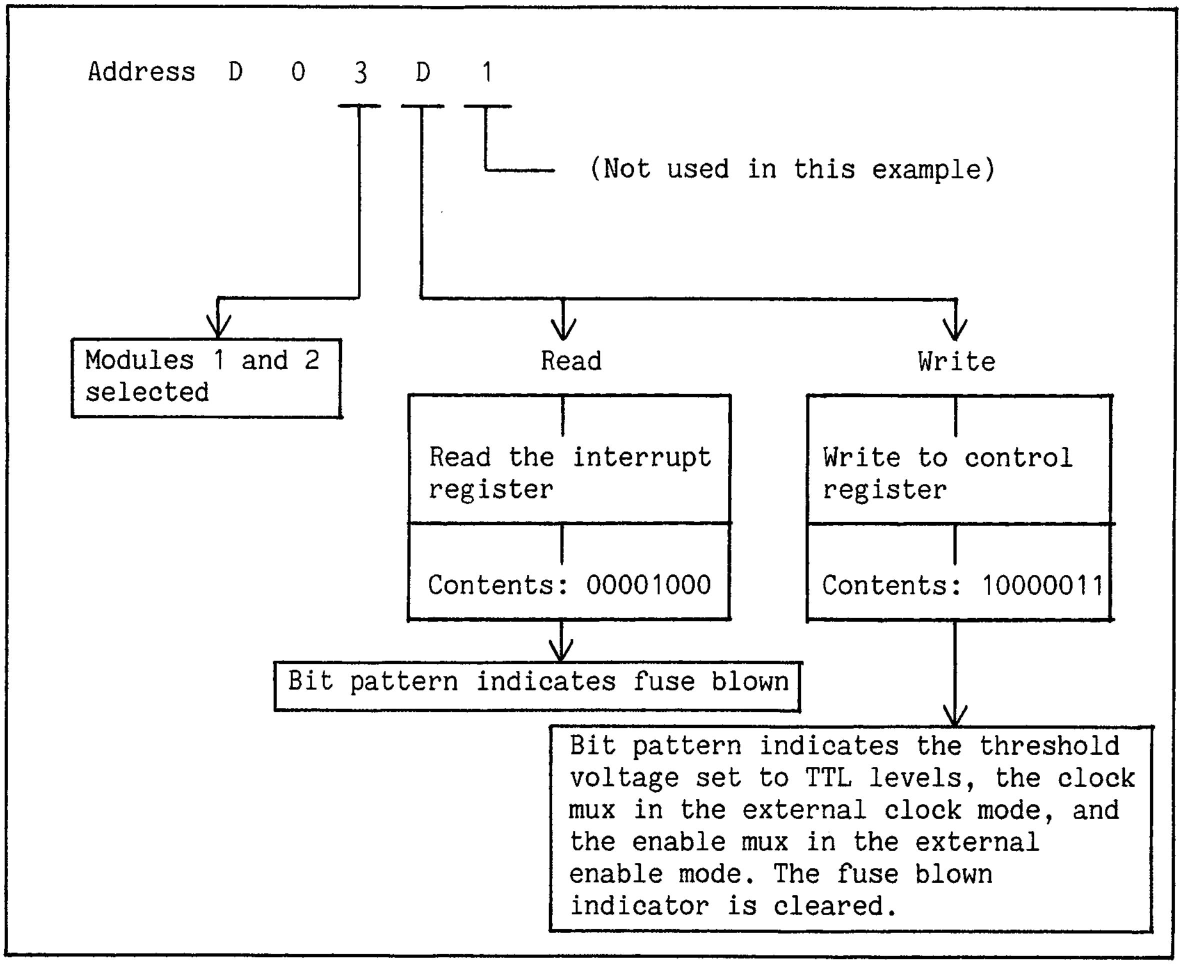


Figure 3-16. Address Decoding Example

Each of the four I/O Modules is controlled via "hot-bit decoding" of address lines A8 through A11. This method of decoding allows any combination of modules to be addressed simultaneously. A brief explanation of "hot-bit decoding" requires examination of the 5-digit hex I/O Module address. The third LSD of the address is broken down into binary form. The position of the set bit(s) determines the module(s) to be addressed. See Figure 3-17 for examples.

The timing diagram, Figure 3-18, shows the signals contained in the bus interface block during a read and write cycle. Each transition point is further explained.

- A: Address appears on bus, and R/W- goes high signifying a read cycle.
- B: RD- and CS- go active. Data bus transceiver U8 turns on, pointing toward the mainframe. Addresses and R/W- are latched by U7 and are guaranteed valid.
- C: Valid read data appears on data bus.

Address	D 0 1 X X	I/O Module 1
	D 0 2 X X	I/O Module 2
	D 0 4 X X	I/O Module 3
	D 0 8 X X	I/O Module 4
	D 0 9 X X	I/O Modules 1, 4
	D 0 F X X	I/O Modules 1, 2, 3, 4
Binary Breakdown	0 0 0 1	I/O Module 1
	0 0 1 0	I/O Module 2
	0 1 0 0	I/O Module 3
	1 0 0 0	I/O Module 4
	1 0 0 1	I/O Modules 1, 4
	1 1 1 1	I/O Modules 1, 2, 3, 4

Figure 3-17. Hot-Bit Decoding Examples

- D: STROBE-, RD-, and CS- return high. Read data guaranteed valid here.
- E: End of read cycle.
- F: Address appears on bus and R/W- goes low signifying a write cycle.
- G: WR- and CS- go active. Data bus transceiver U8 turns on, pointing toward the I/O Module. Addresses and R/W- are guaranteed valid.
- H: STROBE-, WR-, and CS- return high. Write data latched into I/O Module registers.
- I: End of write cycle.

CUSTOM CHIP SELECTION

One use of the Bus Interface is to decode address lines A01 through A07 from the mainframe to determine which custom chips are enabled. As the address signals enter the Main I/O Module PCA through J1, the address lines are latched by U7 (the latch signal is STROBE-). Address lines A07 through A04 are used as address inputs for the decoder (U6). The outputs of U6 are gated to determine which custom chip is enabled. Any one of the five custom chips, or all five may be addressed simultaneously. Particular combinations of the custom chips are not addressed within a module.

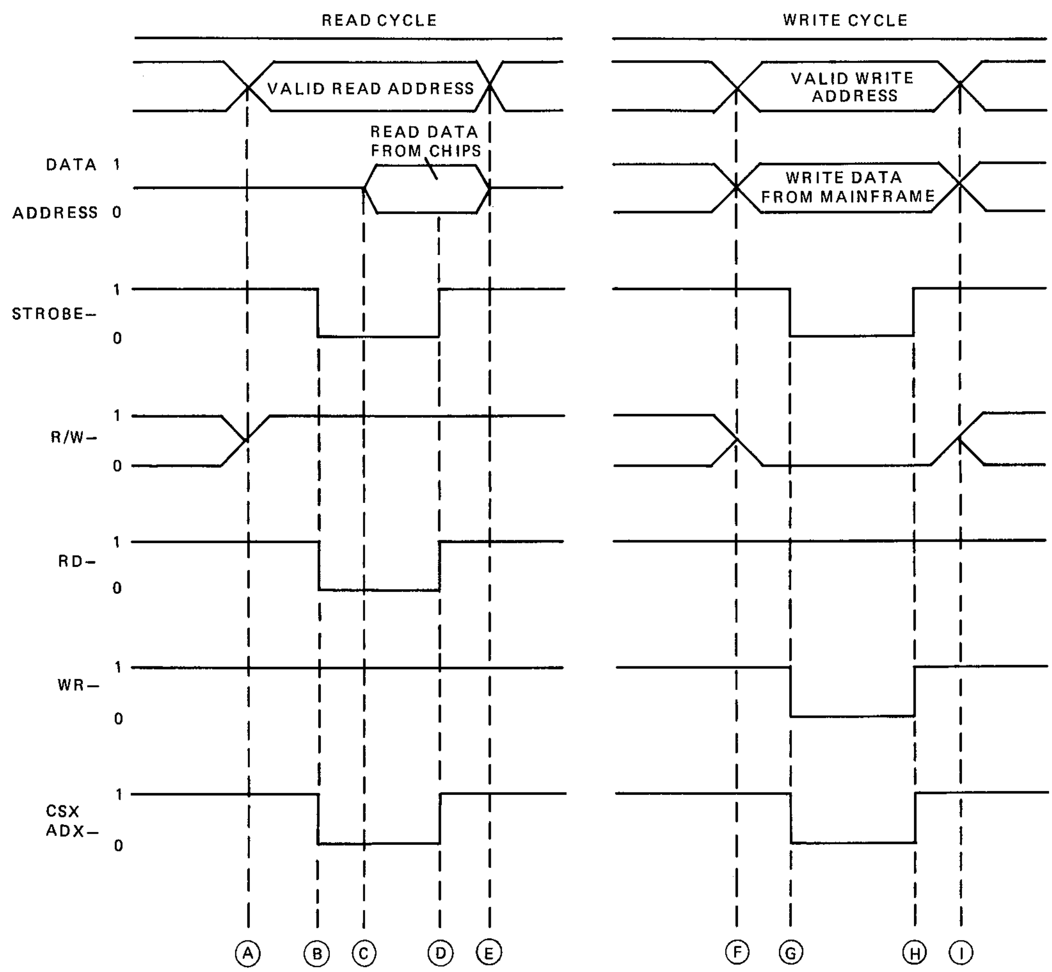


Figure 3-18. Bus Interface Timing Diagram

For example, to select "custom chip U100", the input at U7-13 (A07) from the address bus of the mainframe is at logic low, and U7-18 (A04), U7-17 (A05), and U7-14 (A06) are at logic high. At the occurrence of a strobe signal, U7 latches the logic levels on these pins. At the output signals of U7, LAT-A7 is logic high, and LAT-A4, LAT-A5, and LAT-A6 are logic low. U6 decodes the latched address lines and sets output line AD8- low. The logic low on AD8- is gated and sets up a logic low on CS0-, thereby enabling "custom chip U100". If this were to occur on I/O Module 3, address D0481 would be written.

A custom chip may be addressed individually, or all custom chips may be addressed simultaneously. Address bits A04 through A07 are used to determine custom chip selection. To address all chips, an address in the form DXXFX must be used. This address causes the ALLCHIP signal (U6-7) to go active, making all five chip selects active.

Custom Chip Functional Block

The custom chips each contain eight channels of data acquisition. Each channel performs 16-bit Cyclic Redundancy Checking (CRC), 23-bit (with overflow) transition counting, 3 bits of asynchronous level history recording, 3 bits of synchronous level history recording, and 1 bit of data comparison. The custom chips are used for I/O Module control, and they connect to the data bus via U8. Eleven internal registers control the custom chip. These registers are controlled by Address lines A01 through A03, and the R/W- line.

The pin-out of the custom chip is shown in Table 3-23.

Clock and Enable Mux Functional Block

The Clock and Enable Mux block is located on the I/O Module Main PCA and is shown in the I/O Module Functional Block Diagram, Figure 3-14. Two ICs make up this block: the 74HCT153 (U18) Dual 4:1 Select Multiplexer and the 74HCT04 (U4) Hex Inverter. This block selects one of three sources for the XCK- signal, and one of two sources for the XEN signal.

CLOCK AND ENABLE MUX OPERATION

Inputs

The Clock and Enable block receives inputs from the BUFENA (Buffer Enable) and the BUFCLK (Buffer Clock) signal lines. These signal lines originate from the XCLK (External Clock) and XENA (External Enable) lines. The PSYN (Pod Sync) signal obtained from the EXT-BUS (External Bus) is an alternative clock signal to the external clock and is used for data gathering by the custom chip(s). U18 inputs: POD SYNC, CALCLK1 (Calibration Clock 1), and CALCLK2 (Calibration Clock2) are all clock signals used by the Clock and Enable Mux Block. The POD SYNC signal, which enters the I/O Module as differential ECL, is converted by U9 into TTL levels. This signal enters the EXT-BUS to be used in conjunction with CALCLK1, CALCLK2, ENMUX, and CLKMUX.

Table 3-23. Custom Chip Pin Description

PIN	TYPE	FUNCTION
A0-A2	Input	Address lines
POR-	Input	Power-on reset
SRCK	Input	1 MHz Serial-to-Parallel conversion clock
PDRV0-PDRV7	Output	Pattern Drive PMOS gate drive
NDRV0-NDRV7	Output	Pattern Drive NMOS gate drive
VDD1	Input	Positive voltage supply
VDD2	Input	Positive voltage supply
GND1	Input	Logic common
GND2	Input	Logic common
XD0-XD7	Input/Output	Microprocessor data bus
EQ	Output	Equal (data comparison match) output
TC	Output	Test clock output
WR-	Input	Write enable
RD-	Input	Read enable
CS-	Input	Chip select
VPAT	Input	Negative supply for DRV outputs
TEN	Input	Test mode enable
XSTP	Input	External stop
GATE	Input	Frequency gate input
XSTR	Input	External start
XEN	Input	External enable
XCK	Input	External clock
PSYN	Input	Pod sync clock
VLO	Input	Low voltage threshold select for CD0-CD7
VHI	Input	Hi voltage threshold select for CD0-CD7
CD0-CD7	Input *	Channel inputs
TLI	Input	Test channel comparator input
TLO	Output	Test channel comparator output

* CDn inputs have an internal resistor network to control the voltage at which they will float (the "invalid" voltage). This voltage is approximately 1.6V, through an effective resistance of >50 kilohms.

The CALCLK2 signal enters the Main I/O PCA through the Connector Code Determination Block. CALCLK 1 is not used. Channels 1 through 39 are tied together and to CALCLK 2 when the Calibration Module is plugged in. CALCLK2 is an input to U18-13. The ENMUX and CLKMUX signals are generated by the Control Register (U14-15 and U14-16, respectively) and are control inputs to U18. U18 generates outputs XEN and XCK. Table 3-24 shows which signals appear on the outputs of the multiplexer for all four states of the control inputs.

Table 3-24. U18 Truth Table

Control In		Outputs	
CLKMUX	ENAMUX	XEN	XCK
0	0	BUFENA	BUFCLK
0	1	PSYN	BUFCLK
1	0	BUFENA	CALCLK 1
1	1	PSYN	CALCLK 2

Outputs

The Clock and Enable MUX block outputs XEN and XCK- signals to the EXT-BUS. These two control signals are sent to each custom chip. Three parallel inverters invert the XCK signal from U18-9, and are necessary to ensure a fast rise time into the relatively high capacitance XCK- line.

General Control Latch Functional Block

OVERVIEW

The General Control Latch block, located on the I/O Module Main PCA, is used to vary input thresholds, clear fault conditions, and control the Clock and Enable Multiplexer. Refer to Figure 3-14 for the block's functional relationship on the block diagram. The ICs in this block include: a 74LS273 (U14) 8-bit latch, an LM324 (U2) quad op-amp, two 2N3906 (Q1, Q2) PNP transistors, a 74LS08 (U3) quad 2-input AND gate, a 74LS30 (U15) 8-input NAND gate, and two 74LS112 (U11, U12) dual JK negative-edge-triggered flip-flops.

CONTROL REGISTER

Data lines from the A-D-BUS to U14 produce DCECLR- (Data Compare Equal Clear), GENCLR- (General Clear), FUSCLR- (Fuse Clear), ENMUX (Enable Multiplex), CLKMUX (Clock Multiplex), and THRSH (Threshold) signals. U14 is accessed by a write to DXXDX, where the ADD- and WR- latch data into U14. The Control Register (U14) is cleared by a PWRUP (Power Up) signal held low by C44 to ensure a proper reset.

The J2 and J3 connectors provide the input to the General Control Latch block for detection of Clip and Calibration Modules. J2-25 and J3-6 are the input pins to a detection circuit that provides the SWRDET (the right-hand or B Switch Detect) and SWLDET (the left-hand or A Switch Detect) signals to generate an interrupt. The mainframe reads the interrupt register to determine the reason for an interrupt.

DATA COMPARISON INPUTS

All 40 lines of the I/O Module are compared to a programmable 40-bit data register and qualified by a programmable 40-bit "don't care" register. This comparison is done inside the custom chip(s), eight lines per chip. The EQ outputs (pin 55 of the custom chip), are gated together, and, when they are all high (i.e., a comparison has been detected), an interrupt is generated.

FUSE DETECTION

The FUSEDET (Fuse Detect) is a part of the Multi-Detection area, General Control Latch Block. A 1A slow-blow ground fuse located on the I/O Module Main PCA is used to protect the ground line. The FUSEDET signal becomes an input to the interrupt register (U13-8), along with the other detection signals.

DATA COMPARISON and GENERAL INTERRUPTS

The General Control Latch block outputs detection and interrupt signals for any problems or special operations of the I/O Module. Also, an external DCE pin allows the user to examine the state of the I/O Module hardware.

The following two interrupts are produced by the General Control Latch block:

- DCEINT- (Data Compare Equal Interrupt)
- IOGENINT- (I/O General Interrupt)

The Data Compare Equal Interrupt

The DCEINT- is generated by the I/O Module when the programmed data compare register matches the input data. The DCEINT- signal originates from the EQ pin of each custom chip. The EQ signals are gated to form a DCE- signal. The DCE- signal triggers a J-K flip-flop to produce the DCEDET and DCEINT- signals.

The I/O General Interrupt

The IOGENINT- is an interrupt generated by the I/O Module when either pushbutton on a clip module is pressed. The interrupt status register on the I/O Module must be read to determine the cause. In the case of a button push, two J-K flip-flops output the SWLDET (A side) and SWRDET (B side) signals. These signals are gated to produce the IOGENINT- signal.

Data Compare Equal Output Pin

DCE output pin P1-6 can be used to trigger a logic analyzer or oscilloscope. Buffers and protection circuitry safeguard the DCE signal output.

OPERATION OF GENERAL CONTROL LATCH BLOCK

The General Control Latch Block is divided into three areas. These areas produce voltages for I/O Module operation and contain circuitry that generates detection for a blown fuse. The functional block contains the following areas:

- Threshold Voltage Generation
- Multi-Detection and Interrupt
- Fuse Blown Detection

Threshold Voltage Generation

Threshold Voltage Generation produces the threshold voltages necessary for control of data input to the custom chips. Data Bit 7 of the command register (U14) determines the level of threshold, with a 1 selecting TTL, and a 0 for CMOS. See Figure 3-19 for the command register bit positions.

```
                                      DATA BITS
                                  7 6 5 4  3 2 1 0    Write @ DXXDX
I/O COMMAND REGISTER              X X X X  X X X X

Threshold (1 = TTL)               bit 7
Enable Mux (0 = Ext)              bit 6
Clk Mux (0 = Xclk)                bit 5
Not Used                          bit 4

Clr Fuse Blown (0 = Clr)          bit 3
Not Used                          bit 2
Clr Gen Int (0 = Clr)             bit 1
Clr Dce Int (0 = Clr)             bit 0
```

Figure 3-19. I/O Module Command Register

The threshold (THRSH) signal output of U14-19 passes through circuitry that produces a low voltage level (VLO), and a high voltage level (VHI). These voltage levels are used by the custom chips pins 39 and 45 to define the logic low, invalid, and logic high voltage ranges. A logic high out U14-19 designates a TTL logic level and a logic low for CMOS. The THRSH signal controls resistor dividers that are used to create the VHI and VHO signals. Two parts of op amp U2 and transistors Q1 and Q2 are used together to provide a regulated output with high current sinking capability. Typical current seen by these regulators can vary from 10 to 40 mA. Approximate VHI and VLO levels generated are listed in Table 3-25.

Table 3-25. VHI and VLO for TTL and CMOS Logic Levels

DESC	THRSH	VHI	VLO
TTL	1	-1.0V	-2.4V
CMOS	0	-0.25V	-2.2V

Within the custom chip, a voltage level-detection system uses data inputs, VHI, and VLO voltage levels to detect a high voltage input, a low voltage input, or a tristate situation. See Figure 3-20 for an illustration of detection circuitry within the custom chip.

NOTE

The actual input thresholds for the high and low comparators are computed from the formulas shown in Figure 3-20.

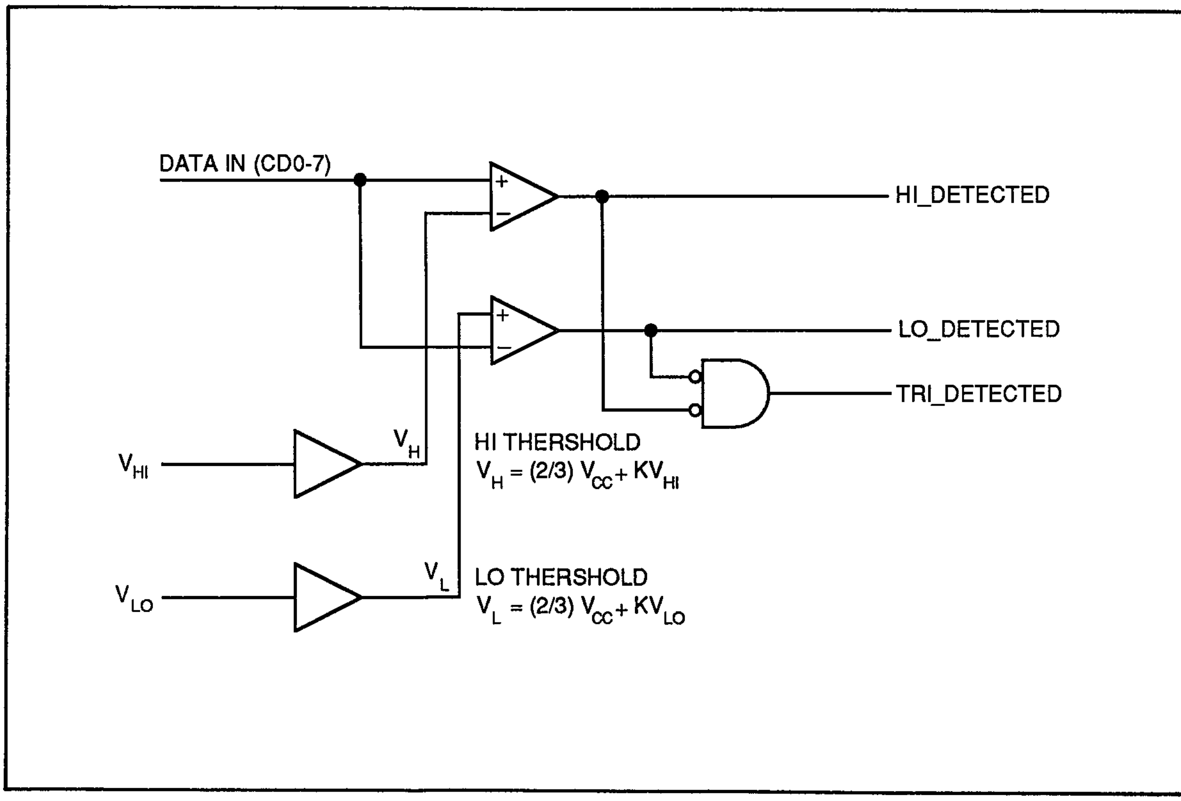


Figure 3-20. Custom Chip Voltage Level Detection

Multi-Detection and Interrupt

The I/O Module accepts different sizes of clip modules. A detection system within the I/O Module is necessary for the mainframe to know the size of the clip that has been installed on the I/O Module. Clip Modules are available in a half-size module and a full-size module. The half-size module plugs into one connector (either J2 or J3), and the full-size module plugs into both connectors (both J2 and J3). Together, clips plugged into both J2 and J3 generate an 8-bit code that can be decoded by the mainframe identify the plugged-in clips.

Fuse Blown Detection

Detection of blown fuses is performed by two LM324 (U2) op-amps and one part of U3 configured as a window detector. If the XGND signal exceeds a +/- 100 millivolt window, U3-6 will go low, forcing the FUSEDET line to go high. This means that when the Interrupt Register is read (READ @ DXXDX), a 1 in bit 3 indicates the fuse is blown. This blown fuse indication is cleared by writing to the I/O Command Register (WRITE @ DXXDX) with a data value having bit 3 = 0.

Connector Code Functional Block

The components associated with the Connector Code block are the 74HCT244 (U16) Octal buffer/line driver and part of J2 and J3 connectors. This block is located on the I/O Module Main PCA as indicated on function block diagram Figure 3-14.

The mainframe determines which Clip Module the user has installed by reading and decoding connector codes embedded in each Clip Module. To read the code, the mainframe performs a read @ DXXE1. This operation generates the ADE- signal, which in turn enables U16, placing the code on the data bus. Of the eight bits read, the lower four bits refer to the "A side", and the upper four bits refer to the "B side". Thus, differentiation is possible for 16 different conditions on each side of the module. Clips that use up an entire module use an 8-bit code. The most significant nibble of these codes is 1110. For a list of the codes, see Table 3-26.

Table 3-26. Dip-Clip and Calibration Module Configuration Codes

4 BIT CODE	MEANING
0000	14-Pin Clip
0001	16-Pin Clip
0010	18-Pin Clip
0011	20-Pin Clip
0100	24-Pin Clip
0101	(reserved)
0110	Used as most significant byte of calibration header
0111	(reserved)
1000	(reserved)
1001	(reserved)
1010	(reserved)
1100	(reserved)
1101	20-Pin Flying Lead Set
1110	Full width connector, use other 4 bits for ID
1111	No Clip Installed

8 BIT CODE 7654 3210	MEANING
1110 0000	28-Pin Clip
1110 0001	40-Pin Clip
1110 0010	Calibration Header
0110 0010	Calibration Header
1110 0011	(reserved)
1110 0100	(reserved)
1110 0101	(reserved)
1110 0110	(reserved)
1110 0111	(reserved)
1110 1000	(reserved)
1110 1001	(reserved)
1110 1010	(reserved)
1110 1011	(reserved)
1110 1100	(reserved)
1110 1101	(reserved)
1110 1111	(reserved)
1111 1111	No Clips Installed

CONNECTOR CODE EXAMPLES

If the connector codes are to be determined on I/O Module 3, a Read @ D04E1 would be performed. Table 3-27 presents some examples of codes and their interpretation.

Table 3-27. Connector Codes

DATA READ	MEANING
F3	No clip on B side, 20 pin clip on A side
4F	24 pin clip on B side, no clip on A side
E1	40 pin clip installed
14	16 pin clip on B side, 24 pin clip on A side
FF	no clips installed

Input Protection/FET Output Block

OVERVIEW

The Input Protection/FET Output Block combines the functions of input channel protection for each custom chip and output for the I/O Module. Input protection clamps overvoltage, undervoltage, and static conditions before they reach the custom chip.

The output circuitry uses complementary N and P channel DMOS FETs. These FETs can be commanded to drive the I/O line high or low or leave it undriven (off). The custom chip drives these FETs through a 74HC244 buffer. Figure 3-21 shows a simplified circuit of a single channel. All 40 channels are functionally identical to each other.

This output circuit uses power supplies +VDRV and -VDRV. These voltages are generated, regulated, and current limited on the Probe I/O and I/O Connector PCAs. The nominal voltages for these supplies are 5 volts and -0.85 volt, respectively.

INPUT PROTECTION SECTION OPERATION

Data from the I/O lines travels through its respective connector into the protection circuit. Diodes connected to +5 volts and ground protect the custom chip from undervoltage and overvoltage.

FET OUTPUT SECTION OPERATION

The output block can assume three states: high, low, and off. The output block, in conjunction with the input block, allows for measurement of signals at the inputs. The truth table shown in Table 3-28 lists the logic levels of NDRV and PDRV.

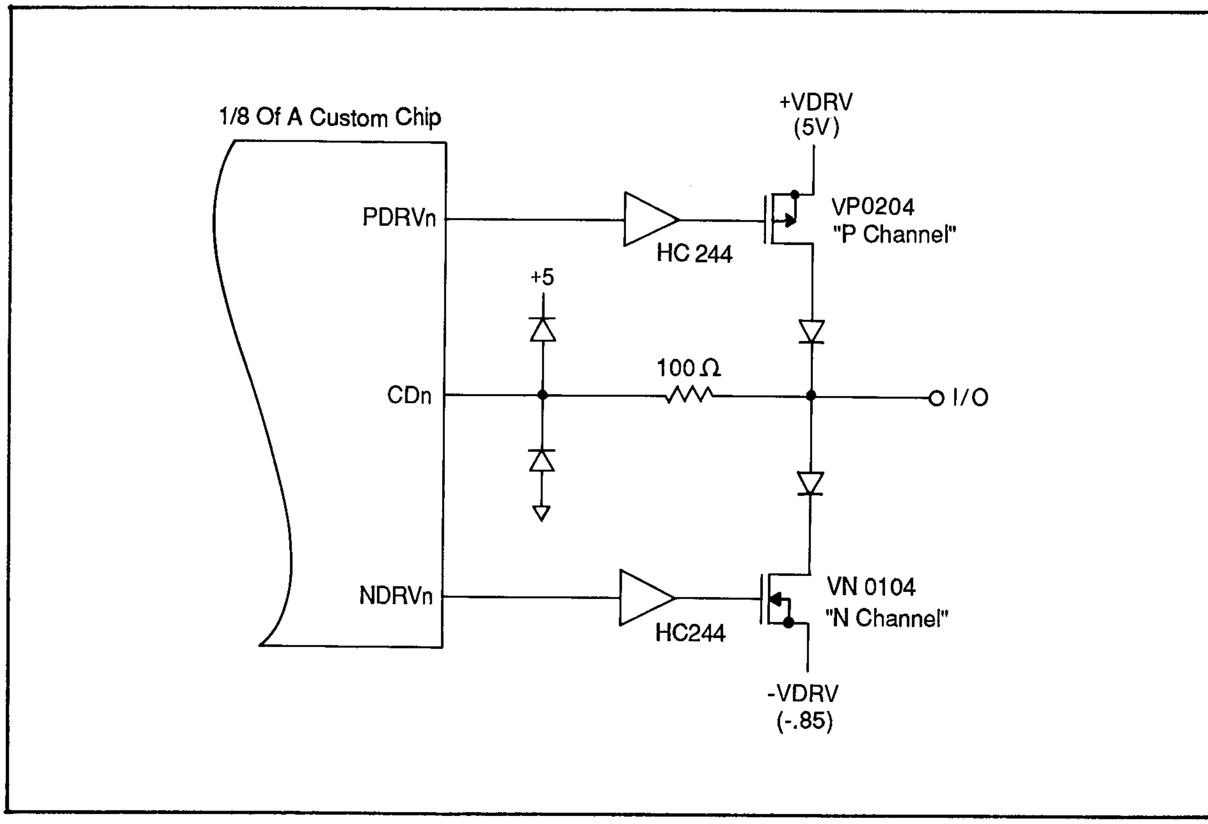


Figure 3-21. Chip Channel Input/Pattern Drive Output Simplified Schematic

Table 3-28. Logic Levels of NDRV and PDRV

OUTPUT	NDRV	PDRV
HI	0	0
LO	1	1
OFF	0	1
(illegal)	1	0

I/O Module Top PCA Functional Block

The top PCA of the I/O Module is a four-layer board consisting of connectors J2 and J3, banana plugs P1-P4, headers J1 and J4, and four 4700 uF capacitors. The top board connectors (J2, J3) provide the input for the 40 I/O lines from the Clip or Calibration Module. The four capacitors together form an effective 4700-uF bipolar capacitor. This is placed across the ground fuse to lower the fuse impedance. P1-P4 represent reference plug-in points between the plug-in module and the I/O Module for external ground and signal ground. The top I/O Module PCA allows for plug-in of a half or full Clip Module or a Calibration Module. These modules plug into J2 and/or J3 of the top PCA and transfer I/O lines to J2 and J3 of the I/O Module Main PCA. P1 and P3 are the signal ground connection points between the I/O Module and the Clip Module. P2 and P4 are the external ground connection points. These connection points improve grounding by providing multiple paths between the clip modules and the I/O Module.

DIP CLIP AND CALIBRATION MODULE FUNCTIONAL BLOCK

The Clip Module is a 9100A/9105A system accessory that offers the user a selection of configurations to test UUT I/O lines. There are two different sizes, a half width and a full width. The number of pins each size can handle is explained in the following paragraphs. The Calibration Module is another unit that the user installs onto the top of the I/O Module for calibration of clock signals.

Overview of the Clip and Calibration Modules

The Half-Width Clip Module is used for connecting the I/O Module to an IC. Five modules are available, in 14-, 16-, 18-, 20-, and 24-pin configurations. If one of these IC clip modules cannot be used, a 20-pin flying lead set is available.

The Full-Width Clip Module connects the I/O Module to 28- and 40-pin IC configurations. The Full Width Module contains two connectors to provide access for up to 40 I/O lines and a ribbon cable attached to either a 28- or a 40-pin IC clip.

The Calibration Module helps perform I/O Module calibration by assuring that simultaneous level transitions occur at both the clock and data inputs of the I/O Module. The clock and data inputs are recorded simultaneously by the latches in the I/O Module. The Calibration Module attaches to the two I/O Module connectors (J2, J3).

Clip and Calibration Module Operation

HALF WIDTH CLIP MODULE

The user plugs the Clip Module into the top of the I/O Module, then attaches the clip connected to a ribbon cable to the UUT. The Half Width Module can be connected to J2 (A side) or J3 (B side) of the I/O Module.

NOTE

Check the schematic for the I/O signals lines used in each case.

An SPST four-position dip switch contained in the Half-Width Module determines the code for the module. This code tells the mainframe the type of pin configuration used during the current I/O test. The connector code is factory set, and should not be changed. For a list of connector codes, see Table 3-27. A black ID button located on the front of the module housing can be used to signal the mainframe.

FULL-WIDTH CLIP MODULE

The Full-Width Module connects to IC chips under test (28- and 40-pin configurations). The Full-Width Module uses the same procedures and tests as the Half-Width Module. The Full-Width Module uses both I/O Module connectors for the additional I/O signal lines.

To identify the connection code of the Full-Width Module, the Module contains an SPST eight-position DIP switch. The Full-Width Module requires an 8-bit connection code so that the mainframe can determine the size of the clip the user has plugged into the I/O Module. A black ID button located on the front of the Full-Width Module is used to signal the mainframe.

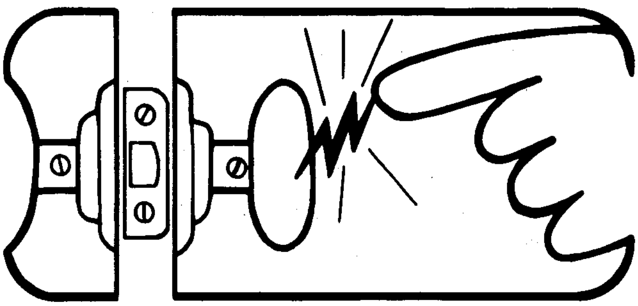
CALIBRATION MODULE

The Calibration Module is used in calibrating both the delay between the data input and the external clock output and the delay between the data input and the pod synchronous clock. The Calibration Module ties channels 1 through 39 and CALCLK2 together. Channel 40 is connected to a "Flying Lead" and is used for calibration to the pod. With the Clock Multiplexer (U18) signal properly programmed, CALCLK2 appears on the XCK lines and clocks all of the custom chips. The Calibration Module connection code is hard-wired as Hex E2. The Calibration Module has an ID button located externally for detection by the mainframe.

static awareness

A Message From

John Fluke Mfg. Co., Inc.



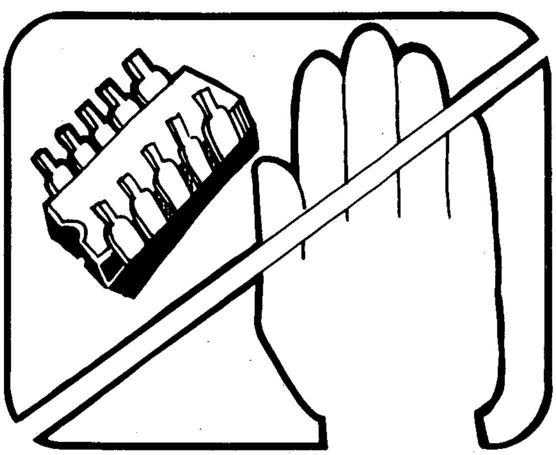
Some semiconductors and custom IC's can be damaged by electrostatic discharge during handling. This notice explains how you can minimize the chances of destroying such devices by:

1. Knowing that there is a problem.
2. Learning the guidelines for handling them.
3. Using the procedures, and packaging and bench techniques that are recommended.

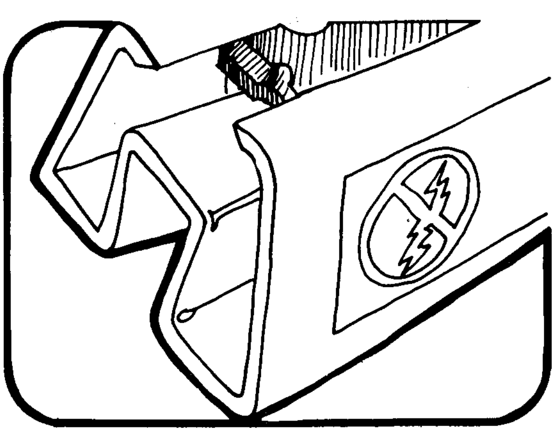
The Static Sensitive (S.S.) devices are identified in the Fluke technical manual parts list with the symbol

" "

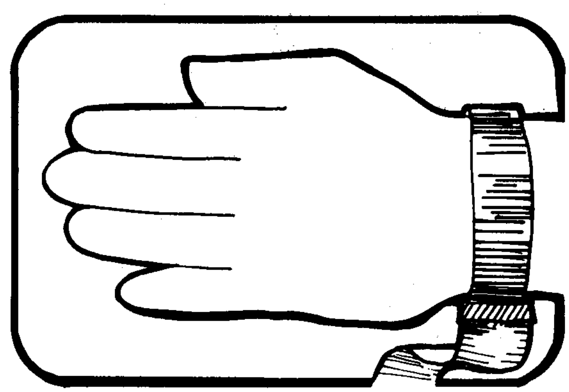
The following practices should be followed to minimize damage to S.S. devices.



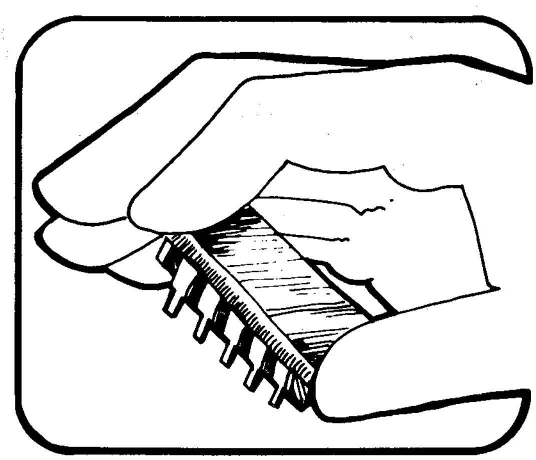
1. MINIMIZE HANDLING



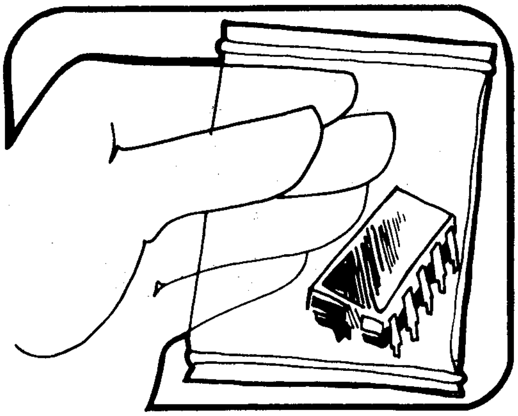
2. KEEP PARTS IN ORIGINAL CONTAINERS UNTIL READY FOR USE.



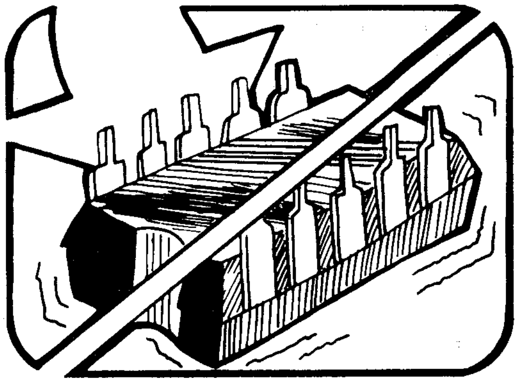
3. DISCHARGE PERSONAL STATIC BEFORE HANDLING DEVICES. USE A HIGH RESISTANCE GROUNDING WRIST STRAP.



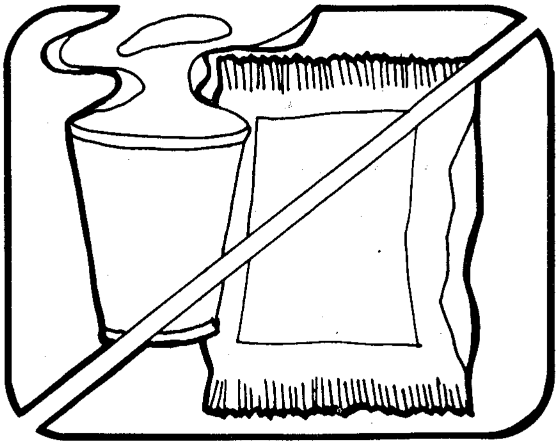
4. HANDLE S.S. DEVICES BY THE BODY



5. USE STATIC SHIELDING CONTAINERS FOR HANDLING AND TRANSPORT



6. DO NOT SLIDE S.S. DEVICES OVER ANY SURFACE



7. AVOID PLASTIC, VINYL AND STYROFOAM® IN WORK AREA

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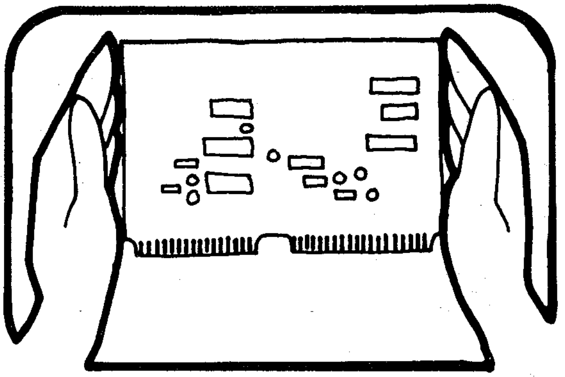
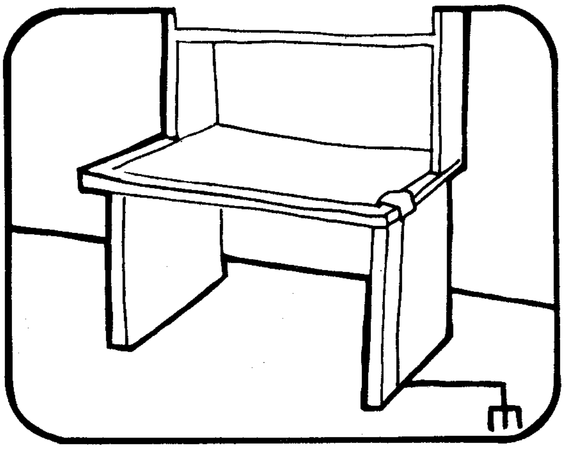


8. WHEN REMOVING PLUG-IN ASSEMBLIES, HANDLE ONLY BY NON-CONDUCTIVE EDGES AND NEVER TOUCH OPEN EDGE CONNECTOR EXCEPT AT STATIC-FREE WORK STATION. PLACING SHORTING STRIPS ON EDGE CONNECTOR HELPS TO PROTECT INSTALLED SS DEVICES.



9. HANDLE S.S. DEVICES ONLY AT A STATIC-FREE WORK STATION
10. ONLY ANTI-STATIC TYPE SOLDER-SUCKERS SHOULD BE USED.
11. ONLY GROUNDED TIP SOLDERING IRONS SHOULD BE USED.

A complete line of static shielding bags and accessories is available from Fluke Parts Department, Telephone 800-526-4731 or write to:

JOHN FLUKE MFG. CO., INC.
PARTS DEPT. M/S 86
9028 EVERGREEN WAY
EVERETT, WA 98204

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J0089D-07U8604/SE EN Litho in U.S.A.
Rev. 1 MAR 86

CONTENTS

WARNING

SERVICING DESCRIBED IN THIS SECTION IS TO BE PERFORMED BY QUALIFIED SERVICE PERSONNEL ONLY. TO AVOID ELECTRICAL SHOCK, DO NOT PERFORM ANY SERVICING UNLESS YOU ARE QUALIFIED TO DO SO.

INTRODUCTION

This section describes maintenance procedures for the 9100A/9105A. Some of these procedures do not require access to the instrument and can be performed by the operator. Troubleshooting procedures, which are covered in detail in the 9100A/9105A Service Kit, may require reference to the disassembly and reassembly instructions found in this section.

Refer to Table 4-1 for a list of tools and test equipment required during 9100A/9105A maintenance.

SELECTING LINE VOLTAGE

Selecting Mainframe Line Voltage

The mainframe line voltage selection switch is located on the 9100A/9105A rear panel. The switch setting (110V or 220V) must correspond to the local line voltage as follows:

Setting	Voltage/Frequency Range	Required Fuse (F1)
110V	90 to 132V ac, 47 to 440 Hz	2A SLOW BLOW
220V	180 to 264V ac, 47 to 63 Hz	1A SLOW BLOW

A correct setting can be verified visually at any time. Otherwise, to change the setting, use the following procedure:

1. Ensure that the 9100A/9105A is turned off and its line power cord is disconnected.

2. Rotate the rear panel switch to the desired setting (110V or 220V).

3. If necessary, replace the power fuse as described later in this section. See Table 4-2 for the fuse part number.

4. Connect the power cord to the correct line voltage, and turn the 9100A/9105A on.

Table 4-1. Required Tools and Test Equipment

EQUIPMENT REQUIRED FOR GENERAL SERVICING

EQUIPMENT	RECOMMENDED MODEL	FUNCTION/COMMENTS
Digital Multimeter	Fluke Model 77	
Oscilloscope	Philips Model PM3065 (or equivalent)	
Adjustment Tool	P/N 800540	
Flat Blade Screwdriver		1/8-inch (3 mm) blade
Flat Blade Screwdriver		1/4-inch (6 mm) blade
Phillips Screwdriver		#2, blade 4 inches (10 cm) or longer
Hex Driver		3/16-inch (5 mm)
Hex Driver		5/16-inch (8 mm)
Wrench		3/16-inch (5 mm) or adjustable

REQUIRED EQUIPMENT FOR COMPONENT LEVEL REPAIR

EQUIPMENT	RECOMMENDED MODEL	FUNCTION/COMMENTS
9100A Service Kit	P/N 818948	
Digital Test Station, with I/O Module	Fluke Model 9105A (or 9100A) with 9100A-003 option	Runs programs supplied with Service Kit
68000 Interface Pod	Fluke Model 9000A-68000	Used with Service Kit
Surface Mount Repair tools		See Table 4-6

Table 4-1. Required Tools and Test Equipment (cont.)

REQUIRED EQUIPMENT FOR MONOCHROME MONITOR MAINTENANCE		
EQUIPMENT	RECOMMENDED MODEL	FUNCTION/COMMENTS
Hex Adjustment Tool	P/N 572321	Horizontal Size/Linearity
Alignment Template	P/N 777144	Use with Monitor Pattern Program
Long-Nose Pliers		
Flat-Blade Screwdriver		1/4-inch (6 mm) blade, plastic handle with blade at least 5 inches (12.5 cm) long.
Phillips Screwdriver		#2, plastic handle with blade at least 3 inches (7.5 cm) long.
Phillips Screwdriver		#2, non-magnetic tip blade, plastic handle, with blade at least 12 inches (30 cm) long, for crt replacement.
Torque Hex Driver		3/16-inch (5 mm).
Soft Pad (foam or quilted)		Approximately 8 x 10 inches (20 x 25 cm).
1 megohm, 1W Resistor	P/N 109793	To discharge crt anode.
Clip Leads (2)		For connecting resistor to chassis and screwdriver shaft.
Safety Gloves		Mid-forearm length, soft leather.
Full Face Shield (preferred) or Safety Goggles		
Lab Smock with Zipper		Plastic zipper. Metal parts should not come in contact with crt.

Selecting Monitor Line Voltage

The line voltage selection switch for the Fluke Monochrome Monitor is located on the monitor rear panel. The mainframe voltage setting (110V or 220V) must be repeated with the Monitor. No fuse changes are required with monitor line voltage changes.

Setting	Voltage/Frequency Range
110V	90 to 132V ac, 47 to 440 Hz
220V	180 to 264V ac, 47 to 440 Hz

To change the setting, use the following procedure:

1. Set the rear panel power switch to off ("0").

2. Rotate the rear panel switch to the desired setting (110V or 220V).

3. Connect the power cord to the correct line voltage, and set the power switch to on ("1").

CHANGING FUSES

Changing the Mainframe Fuse

The mainframe fuse (labeled F1) is accessible from the rear panel. Prior to changing the fuse, set power to off and remove the line power cord. Then, press in and turn the fuse holder cap counterclockwise. Fuse sizes are:

110V	2A SLOW BLOW
220V	1A SLOW BLOW

See Table 4-2 for fuse part numbers.

Changing the Probe Fuse

An operator display message ("probe fuse blown") indicates that the probe fuse has opened. This problem can occur when the probe common lead is incorrectly connected to the UUT.

Prior to replacing the fuse, determine the incorrect common lead connection. Then disconnect probe leads and replace the fuse as follows:

1. Locate the fuse holder, labeled PROBE FUSE, on the mainframe right side.

2. Press the fuse holder cap in, then rotate it counterclockwise.

3. Pull the cap and fuse straight out. Separate the fuse cap and fuse.

4. Use a 0.25A, 250V fast-blow fuse. See Table 4-2 for the fuse part number.

Changing the Clock Module Fuse

An operator display message ("clock module fuse blown") indicates that the Clock Module fuse has opened. This problem can occur when the Clock Module COMMON lead is incorrectly connected to the UUT.

Prior to replacing the fuse, determine the incorrect COMMON lead connection. Then disconnect all Clock Module leads and replace the fuse as follows:

1. Locate the fuse holder on the Clock Module.

2. Press the fuse holder cap in, then rotate it counterclockwise.

3. Pull the cap and fuse straight out. Separate the cap and fuse.

4. Use a 0.25A, 250V fast-blow fuse. See Table 4-2 for the fuse part number.

Changing the I/O Module Fuse

An operator display message ("I/O module fuse blown") indicates that the I/O Module fuse has opened. This problem can occur when the I/O Module COMMON lead is incorrectly connected to the UUT.

Prior to replacing the fuse, determine the incorrect COMMON lead connection. Then disconnect all I/O Module leads and replace the fuse as follows:

1. Locate the fuse holder on the back of the I/O Module, near the cable.

2. Press the fuse holder cap in, then rotate it counterclockwise.

3. Pull the cap and fuse straight out. Separate the cap and fuse.

4. Use a 1A, 250V slow blow fuse. See Table 4-2 for the fuse part number.

Each 9100A or 9105A uses one of two different types of fuses. Instruments configured at the factory for 110V line voltage use 1/4 x 1-1/4 inch fuses with grey fuse holder caps. Instruments configured at the factory for 220V use 5 mm x 20 mm fuses with black fuse holder caps. First, check the color of the fuse cap (grey caps hold U.S. fuses; black caps hold metric fuses). Then select the fuse part number as shown in Table 4-2.

Table 4-2. Fuse Part Numbers

FUSE	US P/N	METRIC P/N
2A SLOW BLOW:	109181	na
1A SLOW BLOW:	109272	808055
0.25A FAST BLOW:	109314	543504

The fuse holder cap is part number 460238 for U.S (grey) usage and 461020 for metric (black) usage.

CLEANING

General

CAUTION

Do not use aromatic hydrocarbons (such as gasoline or other fuels) or chlorinated solvents for cleaning. They may damage plastic materials used in the instrument.

Avoid using excessive amounts of liquid, particularly around the keypad, keyboard, or disk drives.

Both the operator's display and the monitor screen should be cleaned with a soft cloth that has been lightly dampened with a cleaner. Commercially-available lens or crt cleaners or nonabrasive household cleaners are appropriate for this purpose.

Clean the instrument exterior and accessory cables with either a mild solution of detergent and water or a nonabrasive household cleaner.

The operator's keypad and keyboard should be cleaned gently with a cloth or towel that has been lightly dampened with either a nonabrasive household cleaner or a mild solution of detergent and water.

Fan Filter

The fan filter should be cleaned at least once every 90 days, or more often if necessary, to ensure the free flow of cooling air. The filter is positioned behind the louvered filter cover found on the mainframe right side.

To remove the filter, first pull on the cover at both sides of the upper disk drive. Once the latching pins have snapped out of the chassis, lift up on the cover until its bottom is free. Remove and clean the foam filter. Use warm water and detergent.

Floppy Disk Drive

Each floppy disk drive should be cleaned at least once a year. Cleaning involves running a commercially-available cleaning disk in the drive for five seconds.

MAINFRAME ACCESS, REMOVAL, AND INSTALLATION TECHNIQUES

System Connections

System connections are fully explained in the Getting Started guide. Here, in the Service Manual, Figures 4-1 and 4-2 also illustrate system component interconnections. If additional information about reconnecting the system is needed, refer to the Getting Started Guide.

Mainframe Access

WARNING

TO REDUCE THE RISK OF ELECTRIC SHOCK ALWAYS TURN OFF THE 9100A/9105A AND DISCONNECT THE POWER CORD FROM THE PANEL ON THE REAR OF THE CHASSIS BEFORE ACCESSING THE MAINFRAME.

1. With the instrument positioned bottom side up, remove the five screws securing the top. There are two screws on each of the side lips and one screw located at the bottom front.

2. Holding case top and bottom together, rotate the entire instrument to the top up position.

3. Working from the front of the instrument, remove the top cover by gently lifting at midpoint on both sides.

NOTE

Once the cover is free of the mainframe, notice the various cables attached between it and the mainframe. Protect these cables by proceeding cautiously with the following steps.

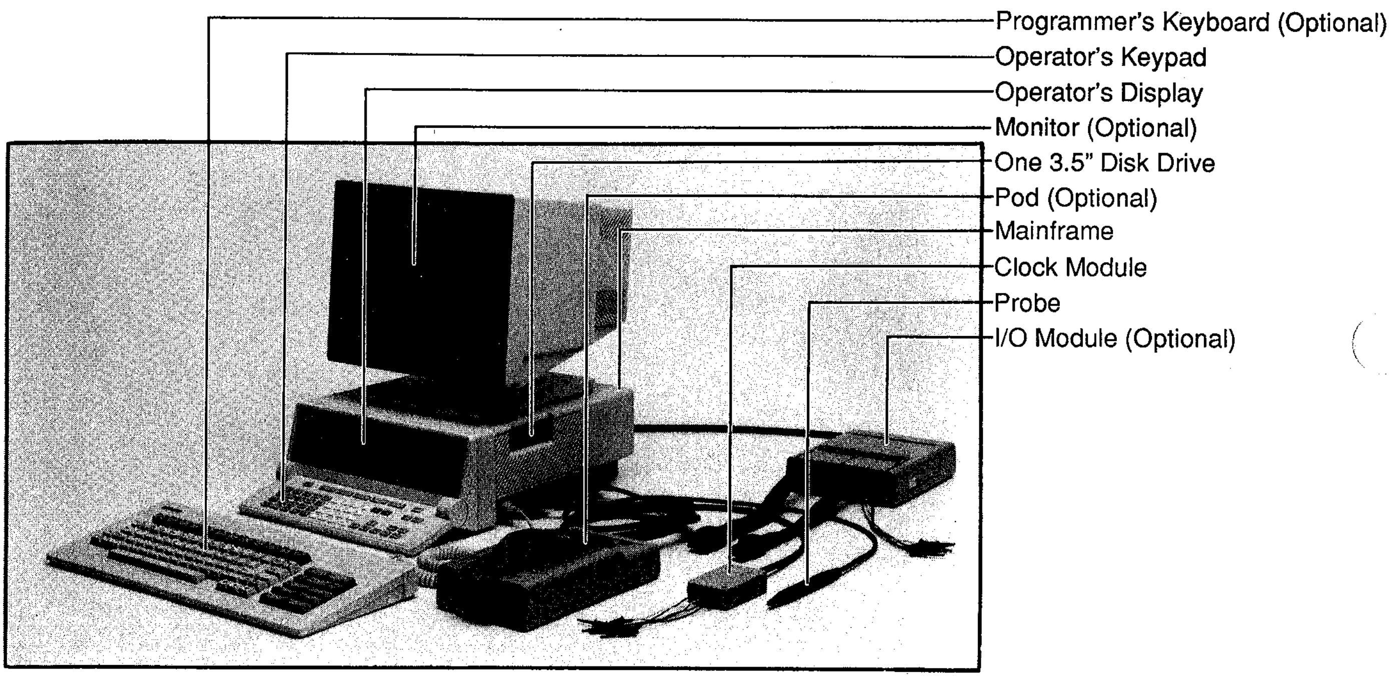


Figure 4-1. 9100A System

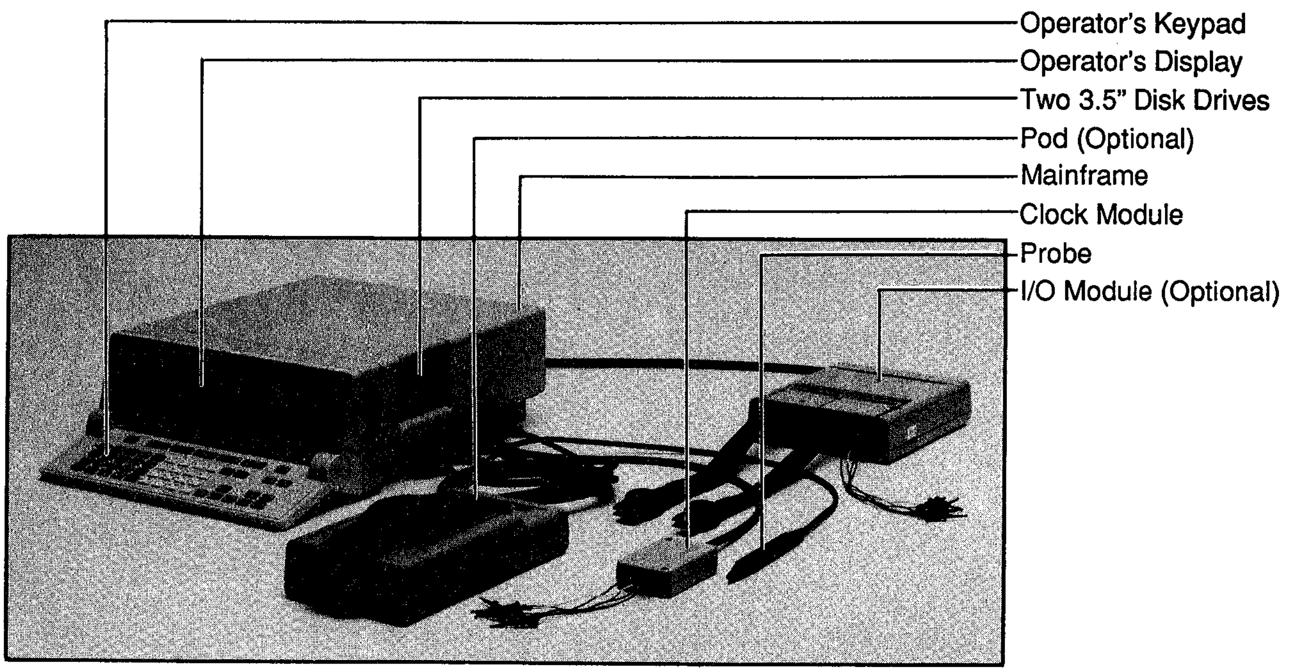


Figure 4-2. 9105A System

4. Rotate the cover 90 degrees clockwise.

5. Tilt the top cover 90 degrees to the left, placing it on a flat surface next to the mainframe. In this position, the floppy disk drive is on edge, facing forward.

CAUTION

The floppy disk drive must be positioned properly to function reliably. Do not position the removed cover so that the floppy disk drive is on top, facing up. Also, the hard disk drive (9100A only) may fail if operated in an incorrect position.

Any instrument assembly or subassembly can now be removed. Note that removal of some assemblies requires prior removal of other assemblies.

Operator Keypad/Display

REMOVING THE ASSEMBLY

The Keypad/Display is attached to the mainframe electrically with one ribbon cable and is physically attached with two screws. First, disconnect the cable at either end (J11 on the Main PCA, or J1 on the Display Interface PCA) by grasping the connector and pulling with a gentle end-to-end rocking action. Then remove the two screws (one at each pivot point), and pull the Keypad/Display free of the mainframe.

SEPARATING THE SUBASSEMBLY

The Keypad and Display can be separated by first disconnecting the ribbon cable connector at J2 (Display Interface PCA). Grasp the connector at both ends and pull with a gentle end-to-end rocking action. Then remove the two securing screws, one at each corner of the pca case. Finally, while guiding the ribbon cable and connector through the respective pca opening, pull the Keypad and Display subassemblies apart.

NOTE

On the Keypad, the two round rotator caps are no longer secured in place when the subassemblies are detached. These caps should be retained separately to avoid inadvertent loss.

When reconnecting the Keypad and Display subassemblies, route the ribbon cable/connector back through the pca opening, but avoid actual connection to the pca until the two securing screws are tightened. This sequence avoids undue stress on the cable and connector.

DISASSEMBLING THE KEYPAD

Although Keypad disassembly is seldom necessary, it can be accomplished quite easily. Before beginning disassembly, awareness of the two precautions is important.

- Once the keypad halves are separated, the keys are no longer secured in place. Avoid key loss by separating the keypad and case only when the keypad is upside down (keys facing down).

- Each rotator cap conceals a spring and plastic securing flange. Particularly note the flange orientation; a small "R" faces right, and a small "L" faces left. Each flange must be reinstalled in the same manner. Also, the springs are not secured in place once the keypad halves are separated and must be separately retained. When separating the keypad halves, note the location of the alignment holes used by the springs.

Use the following steps to separate the two keypad case halves:

1. Remove the screw found along the rear of the keypad.

2. Turn the keypad so that the keys face down, then pull off the securing flange revealed under each rotator cap. Note the orientation of the torsion springs (one at each end).

3. Now pry the two case halves apart, and remove the torsion springs. Leave the key half facing down until otherwise called for during reassembly.

Use the following procedure to reconnect the keypad case halves.

1. With the key half still facing down, install the torsion springs in their respective alignment holes.

2. Now, while holding each spring in place, lower the bottom half onto the key half.

3. Once the springs are properly aligned, install the two securing flanges in the same orientation as noted earlier.

4. Carefully rotate the two halves so that the keys face up. Then press and secure each of the three securing tabs along the front.

5. Install the securing screw.

Disassembling the Disk System

REMOVING THE HARD DISK CONTROLLER

On the front of the Hard Disk Controller card, apply pressure to the card edge, then carefully rock the 50-pin ribbon cable connector loose from J1.

On the rear of the card, remove the 20-pin ribbon cable connector from J2. Then disconnect P1 and J4, both found at the rear card edge.

Now physically disconnect the PCA by removing the screws and gently disengaging its standoff/retainers.

REMOVING THE DISK DRIVE ASSEMBLY

Refer to Figure 4-3. In sequence, remove the two card-edge connectors on the hard disk (9100A only), the 34-pin ribbon cable connector at J14 (Main PCA), and the seven screws securing the disk drive assembly. Grasp the assembly securely before removing the final screw.

The disk drives can now be removed from the disk drive assembly as described below.

- o Floppy Disk Drive: Remove the two screws from each side. Lift or slide the drive out. Then remove the power connector.
- o Hard Disk Drive: Remove the two screws from each side. Gently slide the drive out. Then disconnect the power connector.

CAUTION

The Hard Disk Drive is extremely fragile. Do not jar this assembly at any time during installation or removal.

INSTALLING THE DISK DRIVE ASSEMBLY

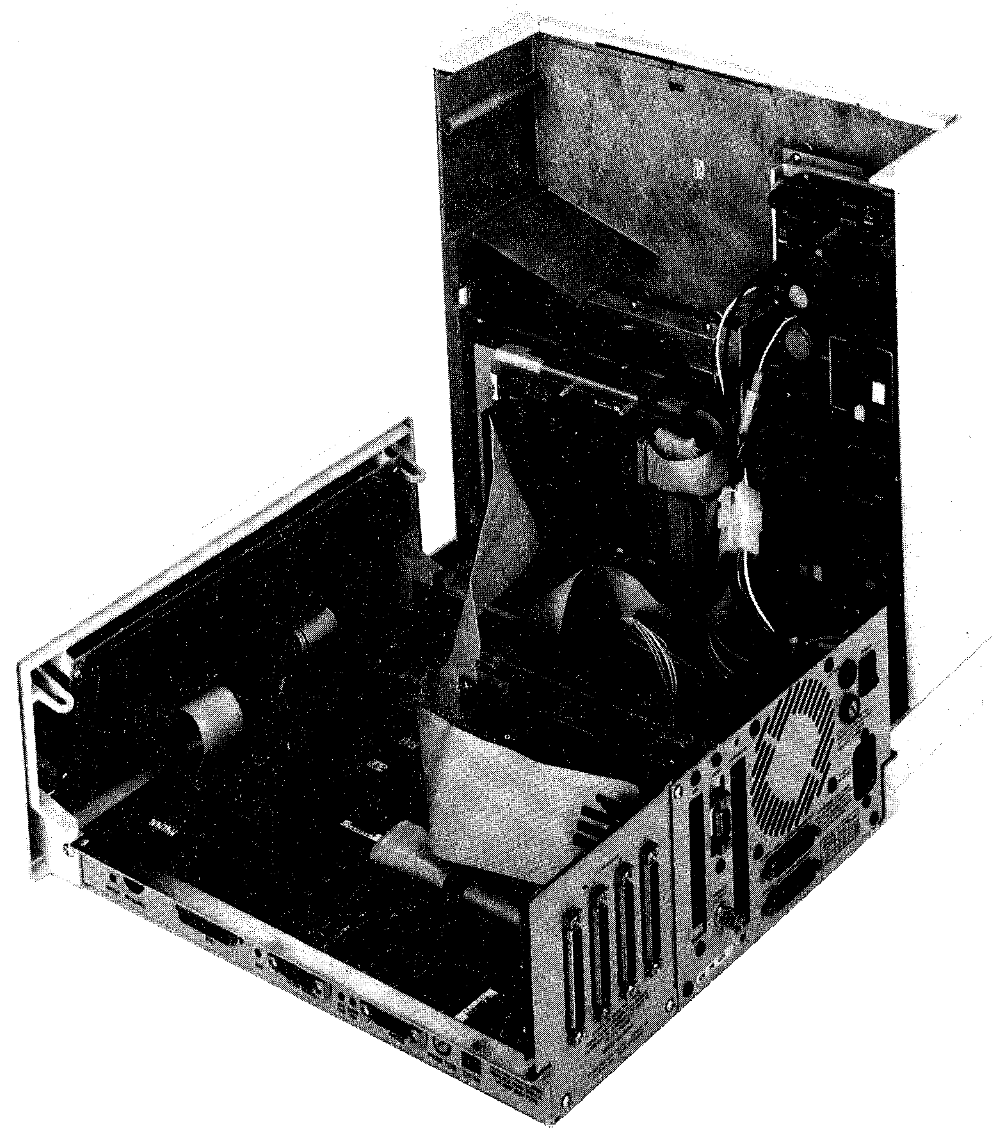
Generally, reassembling and installing the Disk Drive Assembly involves reversing the steps used above during removal. Make sure the 34-conductor ribbon cable and the 4-conductor discrete cable are not pinched between the disk drive assembly and the top cover.

Removing the Power Supply

The Power Supply Assembly uses electrical connections to the Main PCA, the rear panel fuse and power switch, and the disk drive assemblies (as applicable). Disconnect the related cables at the Main PCA and at the in-line connector leading to the rear panel fuse/power switch.

To remove the connections to the disk drives, remove the Disk Drive Assembly, and unplug the power connectors to the floppy disk drive(s), hard disk (9100A only), and hard disk controller (9100A). Disk drive disconnection can also be accomplished by removing the power supply wiring harness from the terminal blocks on the Power Supply Assembly.

Remove the five securing screws, and lift the Power Supply PCA free. Note that four shoulder screws (with nylon washers) are used in the corners. Make sure these items are used during reassembly.



Note: Refer to system interconnect diagrams in Section 7 for electrical connection details.

Figure 4-3. Disassembly Details

If this Power Supply will not be reused in the same instrument, remove the back mounting plate. This plate adapts the Power Supply mounting requirements to those of the 9100A/9105A top cover.

Removing the MFI and Video Controller PCA

Remove the Multi-Function Interface (MFI) PCA, Video Controller PCA, or the Expansion PCA using the following procedure:

1. From the rear panel, remove the screws securing the pca.

2. To dislodge the pca from its connector, alternately lift first at the top-rear, then at the top-front.

Removing the I/O Connector Interface PCA

Remove the three screws securing the I/O Connector Interface mounting plate to the rear panel. Then pull the mounting plate and pca straight up. The pca can be detached from its mounting plate by removing the two screws securing each of the four I/O Module connectors.

Removing the Probe I/O Module Interface PCA

1. Remove the I/O Connector Interface PCA (see above).

2. Detach the ribbon cable connectors at J6 and J7. Grasp each connector at both ends and pull with a gentle end-to-end rocking action.

3. Detach the pca connector for the rear panel TRIGGER OUTPUT.

4. On the right side of the mainframe, remove two screws each for the CLOCK MODULE connector and the PROBE connector.

5. Now remove the four screws securing the pca in place.

6. Gently lift on the inside edge until the pca is detached from the remaining clip connection to the mainframe.

Removing the Main PCA

Use the following procedure for removing the Main PCA:

1. As appropriate, remove the MFI and Video Controller PCAs first.

2. Detach all connectors (8 to 10 places).

3. Remove the two connector locking posts from the pod connector on the right side of the mainframe.

4. Remove the five corner-retaining screws.

5. Gently work the Main PCA free of its mainframe retaining clips.

PROGRAMMER KEYBOARD ACCESS PROCEDURE

1. Place the keyboard on a soft pad to avoid scratching the keycaps.

2. Remove the six screws in the keyboard base plate using a Phillips screwdriver. Lift off the base plate.

3. Pull the keyboard cable connector (J3) off of the Encoder Printed Circuit Assembly (PCA).

4. Remove the ground connection, using a flat-blade screwdriver.

5. Gently pull out the three ribbon connectors from J1 and J2.

6. Remove the Encoder PCA attachment (four screws) from the keyswitch assembly using a flat-blade screwdriver.

7. Remove the keyswitch assembly from the keyboard case (four screws) using a flat-blade screwdriver.

8. To replace the keyboard components, reverse the above procedure. When replacing the three ribbon connectors, do not insert the clear acetate into the connectors.

Replace the keycaps by using the following procedure:

1. Use a flat-blade screwdriver to lift up the corner of the keycap, and lift the keycap off with your fingers.

   Removing the keycap exposes a spring, a plunger, and a keyswitch base.

2. Keycaps slide on more easily if they are not pressed straight down.

   To replace a keycap, position it over the plunger and press the bottom edge of the keycap down first, then press down the top edge.

   NOTE

   Some of the keycaps come completely off, leaving the plunger and spring on the keyswitch membrane. Other keycaps come off with the plunger still attached and the spring loose. To replace these keycaps, the plunger, spring and keycap must be properly aligned before they can be pressed down.

3. Replace the space bar using the following procedure:

   a. Using a flat-blade screwdriver, lift off the space bar. This exposes a wire, plunger, spring, center post, and two corner posts.

   b. If necessary, remove the wire, plunger and spring.

c. Place the spring on the center post.

d. Place the plunger on the spring. Press on the front edge and then the back edge of the plunger to work it into place on the center post.

e. Slide the metal wire into the corner posts so that the wire rests over the center plunger and will depress the plunger when pressed.

f. Turning the keyboard up to view it from an angle, snap the wire in place in the two depressions beneath the hooks on the underside of the bar. Use a screwdriver to assist you in snapping the wire into place.

g. Press down on the space bar to lock it into place.

SCREEN OVERLAY

Recommended Use

The Contrast Enhancement Overlay enhances contrast and reduces reflection from external sources.

Removing the Overlay

To remove the overlay, spread the fingers of one hand and place your hand on the screen. Close your hand slightly, allowing the friction of your fingers to pull the overlay away from the screen.

Installing the Overlay

Use the following procedure to remove the Contrast Enhancement Overlay:

1. The overlay has adhesive on both tabs on the side opposite the matte surface. Remove the backing from the adhesive.

2. With the matte surface facing out, insert one overlay tab under the center of the lip at the top of the screen.

3. Insert the other overlay tab under the center of the lip at the bottom of the screen. Hold the overlay in place with your hand.

4. Slip the side of the overlay under the lip at the left side of the screen by simultaneously running your finger along the left edge of the overlay, and sliding the overlay under the screen lip.

5. Spread the fingers of your left hand to hold the left side, top, and bottom of the overlay in place. Use your right hand to insert the overlay right edge under the right edge of the screen lip.

6. Center the overlay. Press firmly directly over the tabs of the overlay to activate the adhesive.

MONITOR ACCESS, REMOVAL, INSTALLATION TECHNIQUES

The following instructions pertain to the Monochrome Monitor used with the 9100A Programmer's Station and Monochrome Video option.

Removing the Monitor Cover

1. Disconnect the line cord from the Monitor.

2. Use a Phillips screwdriver to remove the two screws along the bottom front and the single screw at the top rear.

3. Place the Monitor face down on a flat surface. To protect the screen from scratches, the surface must be covered with a soft cloth or pad.

4. Remove the four Phillips screws securing the tilt-base assembly to the Monitor. Rotate the assembly so that the hole found in the plastic foot successively allows access to each screw.

5. Pull the plastic Monitor case up and off.

6. Replace the Monitor case by reversing these steps.

Accessing the Monitor Chassis

1. Remove the five Phillips rear panel securing screws. Do not remove the power panel.

2. Place the Monitor screen face down on a flat surface that is protected by a soft cloth or pad.

3. Swing the bottom chassis cover open. The hinge will allow the chassis cover to open to 90 degrees.

4. To close the Monitor chassis, reverse the above procedure.

Removing the Front Bezel

1. Remove the monitor cover as described above.

2. Place the monitor chassis on a flat surface, with the front bezel extended over the edge of the work surface.

3. Locate the six front bezel connector holes. The connector holes are located on each side of the metal chassis, where the plastic snaps from the bezel are inserted in the chassis.

4. Insert a flat screwdriver into each of the connector holes, and push in to disengage the front bezel snaps. Maintain an outward force on the bezel to keep the snaps disengaged.

5. Lift the front bezel away from the chassis.

6. To reinstall the front bezel, position the bezel with the bezel snap fingers in line with the connector holes. Press in evenly on the bezel until all of the front bezel fingers snap into place.

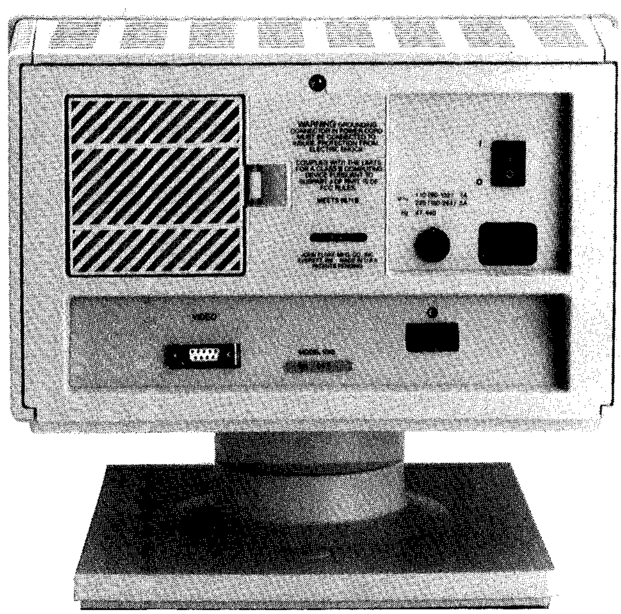


Figure 4-4. Monitor Rear Panel

Monitor Power Supply

REMOVING THE MONITOR POWER SUPPLY

WARNING

USE EXTREME CAUTION WHEN REMOVING THIS UNIT. THERE IS A DANGER OF ELECTRICAL SHOCK FROM HIGH VOLTAGE STORED IN CAPACITORS.

1. Lethal voltages may be present. Disconnect the power and wait 30 seconds before working with the power supply.

2. Open the chassis as described under the heading, "Accessing the Monitor Chassis".

3. Place the Monitor face down on a soft, level surface.

4. Disconnect the six wires that connect the power panel to the power supply. Refer to Figure 4-5 for wire locations.

5. Remove the power panel (two Phillips screws).

6. Remove the Phillips screw found in the rear corner of the Power Supply PCA.

7. Now work the Power Supply PCA loose from the three securing standoffs found in the remaining three corners.

8. Holding the Power Supply PCA in one hand, use the other hand to disconnect the power/video cable connector from the power supply. Be careful not to brush against the crt or yoke.

9. Remove the Power Supply PCA from the chassis.

NOTE

Do not discard the piece of foam that rests between the power supply and the chassis.

INSTALLING THE MONITOR POWER SUPPLY

The following installation procedure assumes that the existing Power Supply has already been removed:

1. Place the Monitor face down on a soft, level surface.

2. Install three new plastic standoffs into the square holes in the chassis top.

NOTE

> Do not reuse plastic standoffs. Damage to standoffs may occur during removal without being clearly apparent. Fluke recommends that PCAs ALWAYS be equipped with new standoffs. All replacement modules are provided with new standoffs.

3. With the power/video cable connector directed toward the rear of the Monitor, connect the power/video cable to the power supply. The power/video cable connector may be fit over any two of the three sets of pins.

4. Reinsert the foam piece between the power supply and the chassis.

5. Place the power supply over the standoffs and press on the PCA to lock it in place. Install the Phillips screw in the rear corner of the pca.

6. Connect the power leads and ground. Refer to Figure 4-5 for wire connections.

NOTE

> The mains wiring must not touch the secondary wiring (power/video cable). If wires touch, the unit will probably exceed conducted emissions limits. The power/video cable should be taut against the side of the chassis.

7. Replace the power panel.

8. Close the chassis cover.

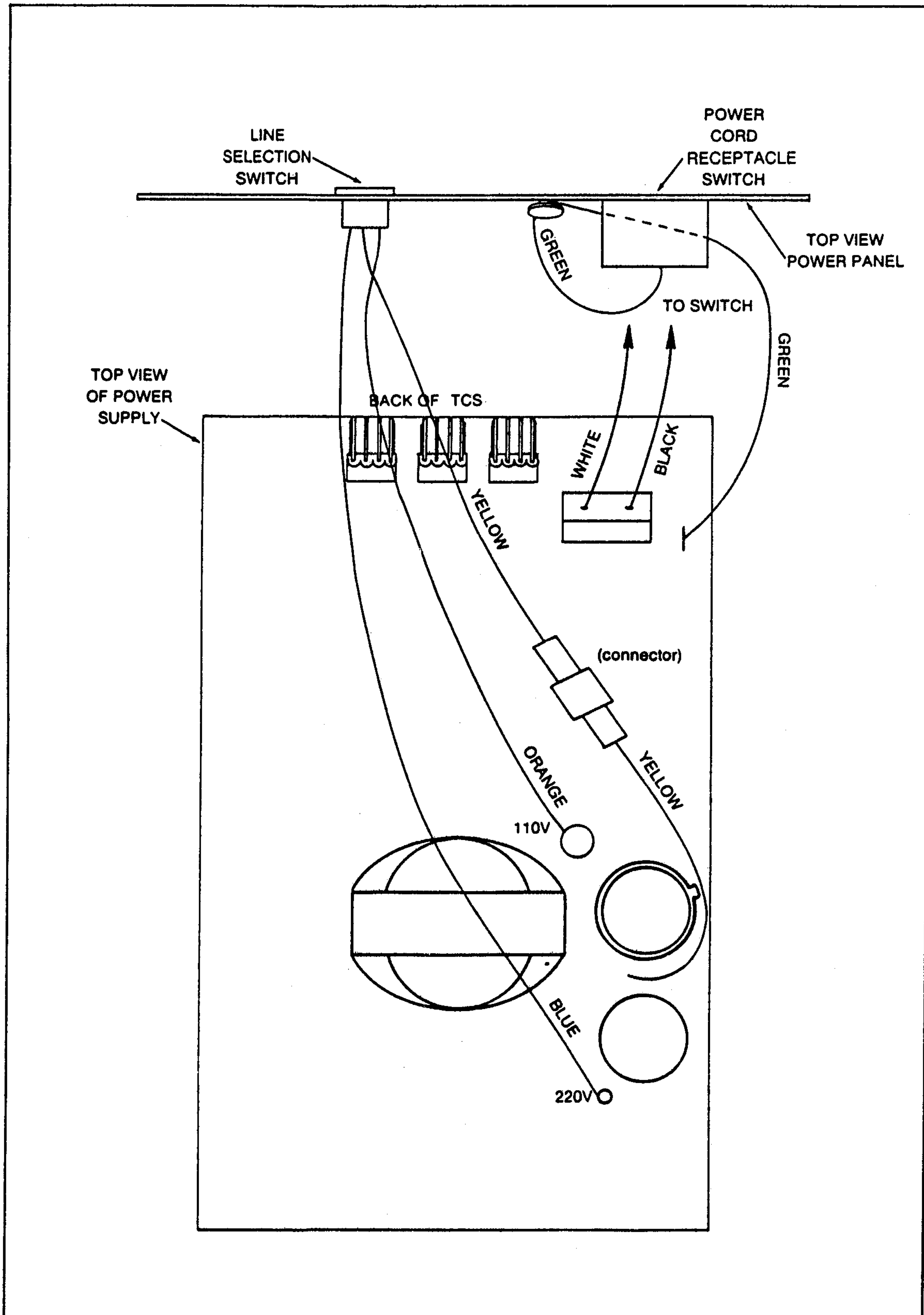


Figure 4-5. Power Supply Lead Connections

Monitor Display PCA

REMOVING THE DISPLAY PCA

NOTE

Fluke recommends replacing the crt when the Display PCA is replaced.

WARNING

TO REDUCE THE RISK OF ELECTRIC SHOCK ALWAYS TURN OFF THE TCS, DISCONNECT THE POWER CORD FROM THE PANEL ON THE REAR OF THE CHASSIS, AND WAIT ONE MINUTE BEFORE PROCEEDING WITH DISPLAY PCA REMOVAL.

WARNING

THE HIGH VOLTAGE SUPPLY MAY RETAIN A HIGH VOLTAGE CHARGE EVEN AFTER THE INSTRUMENT HAS BEEN TURNED OFF FOR SOME TIME. A CHARGE CAN BUILD UP ON THE CRT ANODE EVEN AFTER IT HAS BEEN DISCHARGED. THE CHARGE CAN DELIVER A SHOCK THAT COULD CAUSE THE CRT TO BE DROPPED, RESULTING IN AN IMPLOSION AND DANGEROUS FLYING GLASS.

1. Open the chassis as described under the heading, "Accessing the Monitor Chassis".

NOTE

Although the Display PCA uses a bleeder resistor, as a safety precaution assume that the resistor is nonfunctional.

2. Discharge the anode to the crt through a 1-megohm resistor as follows:

   a. Connect one end of the resistor to the chassis with one clip lead.

   b. Connect the other end of the resistor to the shaft of a 5-inch or longer screwdriver with a 1/4-inch tip, using another clip lead.

   c. Hold the screwdriver by its plastic handle, and gently slip the tip under the edge of the anode connector on the crt end of the high-voltage lead; keep the blade flat against the glass envelope.

   d. Slide the blade forward until the screwdriver blade touches the metallic clip at the end of the high-voltage lead. Be careful not to scratch the surface of the crt.

3. Remove the power/video cable connector from the Display PCA. Use both hands to pull the cable vertically away from the Display PCA.

   Be careful not to bend the Display PCA. Refer to Figure 4-6 for the location of the power/video cable.

   CAUTION

   Bending the Display PCA can break solder joints and result in unreliable operation.

4. Working from the chassis exterior, remove the five standoff-securing screws for the Display PCA.

5. Locate the single black ground wire that attaches to the crt mounting bracket in the upper corner of the chassis. Pull the ground wire off the tab in the mounting bracket.

6. Gently pull the crt socket away from the end of the crt.

7. Disconnect the yoke wire connectors from the Display PCA.

8. Use a side-to-side motion to pry the anode on the crt loose from the anode connector. If necessary, use a non-conductive tool to help disengage the connector.

9. Remove the four PCA standoffs.

10. Remove the Display PCA with the anode and drive wires attached.

INSTALLING THE DISPLAY PCA

NOTE

Fluke recommends replacing the crt when the Display PCA is replaced.

WARNING

TO REDUCE THE RISK OF ELECTRIC SHOCK ALWAYS TURN OFF THE 9100A/9105A, DISCONNECT THE POWER CORD FROM THE PANEL ON THE REAR OF THE CHASSIS, AND WAIT ONE MINUTE BEFORE PROCEEDING WITH DISPLAY PCA INSTALLATION.

1. Open the chassis as described under the heading, "Accessing the Monitor Chassis".

2. Use a Phillips screwdriver to remove the two screws on the power panel. Disconnect the six wires that connect the power panel to the power supply. Refer to Figure 4-5 for wire locations. Remove the power panel.

3. Install the Display PCA using four standoffs. Be careful not to bend the Display PCA.

CAUTION

Do not bend the Display PCA. Doing so can break the solder joints and result in unreliable operation.

4. Replace the power/video cable connector in the Display PCA.

5. Snap the anode connector to the top of the crt.

6. Reattach the crt neck connector to the top of the neck of the crt. The connector is keyed to the pins.

7. Reconnect the yoke connectors.

8. Reattach the black ground wire to the tab on the crt mounting bracket beneath the X-ray warning on the chassis.

9. Reconnect the six wires that connect the power panel to the power supply. Refer to Figure 4-5 for wire locations. Replace the power panel.

10. Close the chassis cover as described under the heading, "Accessing the Monitor Chassis".

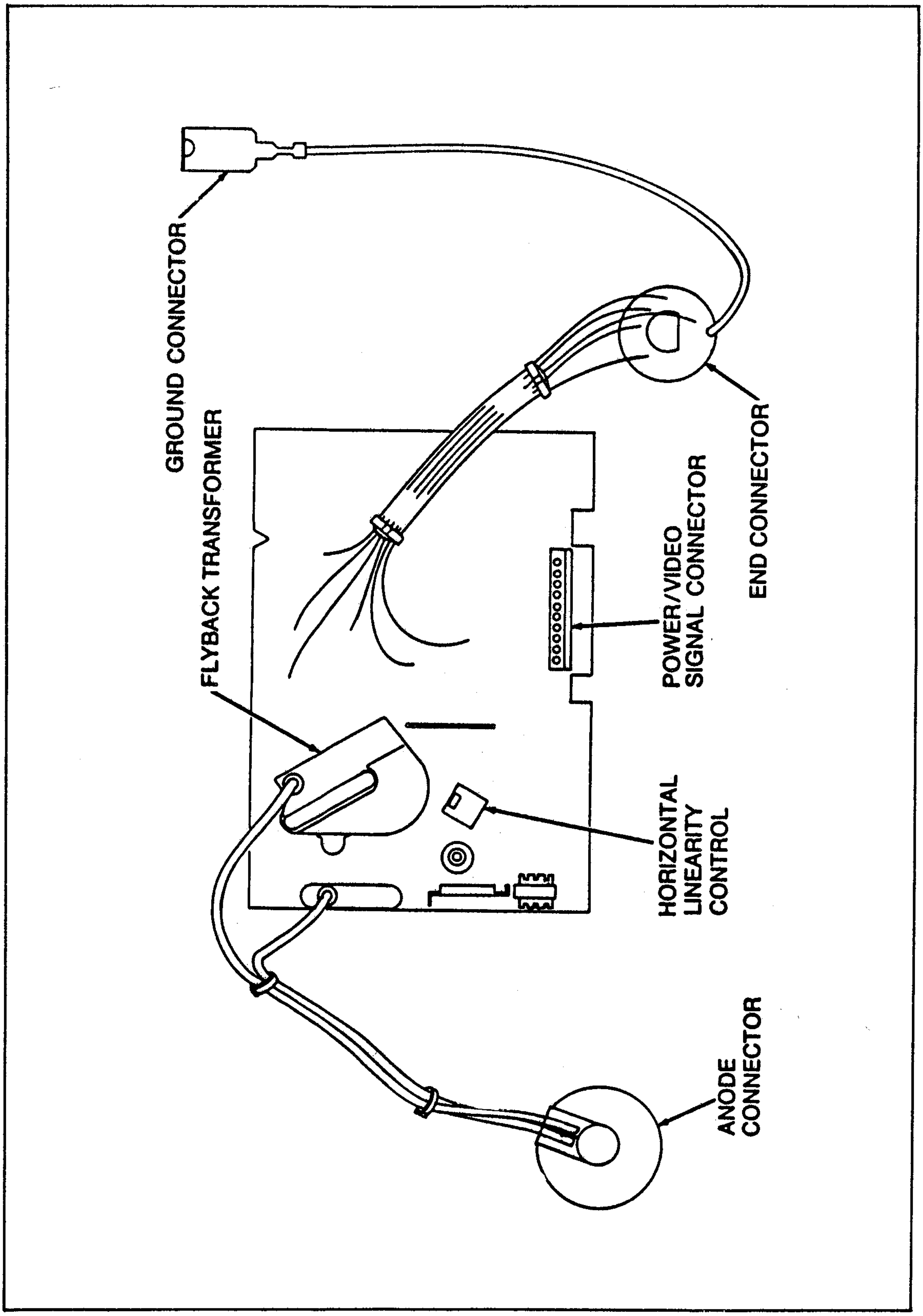


Figure 4-6. Display PCA

Crt and Yoke

REMOVING THE CRT AND YOKE

NOTE

Fluke recommends replacing the Display PCA when the crt is replaced.

WARNING

TO AVOID INJURY, USE CAUTION WHEN HANDLING THE CRT. WEAR PROTECTIVE CLOTHING AND SAFETY GLASSES OR A FULL FACE SHIELD. AVOID STRIKING THE CRT ON ANY OBJECT THAT MIGHT CAUSE IT TO CRACK OR IMPLODE. NEVER HANDLE THE CRT IN AN UNSAFE AREA, SUCH AS ONE WITH WET FLOORS OR HIGH ACTIVITY. NEVER HANDLE THE CRT AROUND OTHERS WHO MAY NOT BE PROPERLY PROTECTED. AVOID SCRATCHING THE TUBE OR CAUSING OTHER DAMAGE DURING INSTALLATION.

WARNING

TO REDUCE THE RISK OF ELECTRIC SHOCK ALWAYS TURN OFF THE 9100A/9105A, DISCONNECT THE POWER CORD FROM THE PANEL ON THE REAR OF THE CHASSIS, AND WAIT ONE MINUTE BEFORE PROCEEDING WITH CRT AND YOKE REMOVAL.

WARNING

THE HIGH VOLTAGE SUPPLY MAY RETAIN A HIGH VOLTAGE CHARGE EVEN AFTER THE INSTRUMENT HAS BEEN TURNED OFF FOR SOME TIME. A CHARGE CAN BUILD UP ON THE CRT ANODE EVEN AFTER BEING DISCHARGED. THE CHARGE CAN DELIVER A SHOCK THAT COULD CAUSE THE CRT TO BE DROPPED, RESULTING IN AN IMPLOSION AND DANGEROUS FLYING GLASS.

1. Discharge the anode to the crt through a 1-megohm resistor as follows:

   a. Connect a resistor end to the chassis with clip lead.

   b. Connect the other end of the resistor to the shaft of a 5-inch or longer screwdriver with a 1/4-inch tip, using another clip lead.

   c. Hold the screwdriver by its plastic handle, and gently slip the tip under the edge of the anode connector on the crt end of the high-voltage lead; keep the blade flat against the glass envelope. Slide the blade forward until the screwdriver blade touches the metallic clip at the end of the high-voltage lead. Be careful not to scratch the surface of the crt.

2. Disconnect and remove the Display PCA as follows:

   a. Gently pull the crt socket away from the end of the crt.

   b. Disconnect the yoke wire connectors from the Display PCA.

   c. Use a side-to-side motion to pry the anode on the crt loose from the anode connector. If necessary, use a non-conductive tool to help disengage the connector.

   d. Remove the four pca standoffs.

   e. Remove the Display PCA with the anode and drive wires attached.

3. Use a Phillips screwdriver to remove the two screws on the power panel.

4. Disconnect the six wires that connect the power panel to the power supply. Refer to Figure 4-5 for wire locations. Lift off the power panel.

5. Remove the front bezel (see "Removing the Front Bezel", earlier in this section.)

6. Use a Phillips screwdriver to remove the eight outside screws from the four crt mounting brackets. Remove the tab from the crt mounting bracket at the corner of the crt.

7. Remove the dust gasket.

8. With the crt face down (on a soft, level surface), lift the chassis off the crt. Be careful not to scratch any part of the crt!

9. Place the crt on a soft, level surface.

INSTALLING THE CRT AND YOKE

NOTE

Fluke recommends replacing the Display PCA when the crt is replaced.

WARNING

TO AVOID INJURY, USE CAUTION WHEN HANDLING THE CRT. WEAR PROTECTIVE CLOTHING AND SAFETY GLASSES OR A FULL FACE SHIELD. AVOID STRIKING THE CRT ON ANY OBJECT THAT MIGHT CAUSE IT TO CRACK OR IMPLODE. NEVER HANDLE THE CRT IN AN UNSAFE AREA, SUCH AS ONE WITH WET FLOORS, HIGH ACTIVITY, ETC. NEVER HANDLE THE CRT AROUND OTHERS WHO MAY NOT BE PROPERLY PROTECTED. AVOID SCRATCHING THE TUBE OR CAUSING OTHER DAMAGE DURING INSTALLATION.

WARNING

TO REDUCE THE RISK OF ELECTRIC SHOCK ALWAYS TURN OFF THE 9100A/9105A, DISCONNECT THE POWER CORD FROM THE PANEL ON THE REAR OF THE CHASSIS, AND WAIT ONE MINUTE BEFORE PROCEEDING WITH CRT AND YOKE INSTALLATION.

WARNING

THE HIGH VOLTAGE SUPPLY MAY RETAIN A HIGH VOLTAGE CHARGE EVEN AFTER THE INSTRUMENT HAS BEEN TURNED OFF FOR SOME TIME. THE CHARGE CAN DELIVER A SHOCK THAT COULD CAUSE THE CRT TO BE DROPPED, RESULTING IN AN IMPLOSION AND DANGEROUS FLYING GLASS.

The Display PCA and power panel must be removed prior to crt installation.

1. With the crt face down on a soft, level surface and the anode facing away from you, loosely install the four crt brackets to the four crt mounting ears and crt grounding clip (step 2).

CAUTION

Do not move the magnets on the crt yoke.

2. Insert the crt grounding clip under the screw on your right, closest to you. Insert the ground wire tab into the clip.

3. Carefully insert the chassis over the crt with the anode connection on the crt positioned toward the top of the unit.

4. Use a Phillips screwdriver to install and loosely tighten the eight exterior screws on the four crt mounting brackets.

5. Approximately center the crt. Use a long-bladed screwdriver to tighten the four screws that attach the crt to the crt mounting bracket.

6. Push the crt as far forward as possible into the chassis and tighten the exterior screws.

7. Clean the crt with alcohol or another suitable cleaner.

8. Reinstall the Display PCA as described above.

9. Reinstall the dust gasket.

10. Reinstall the front bezel.

11. Reconnect the six wires that connect the power panel to the power supply. Refer to Figure 4-5 for wire locations. Reinstall the power panel by replacing the two screws.

12. Perform the procedure under the heading "Monitor Adjustment."

13. Close the chassis cover.

MONITOR ADJUSTMENT

NOTE

Display tilt may be slightly affected by the orientation of the Monitor, especially in environments containing a high density of metal. Rotate the unit and try to find a position where the tilt is in the center between extreme clockwise tilt and extreme counterclockwise tilt. Perform alignment and adjustment in that position. If no difference is perceived between the two extremes, proceed in the most convenient orientation.

NOTE

Magnetic alignment is accomplished with alignment magnets. Magnets should not be removed or added to the crt yoke. The displays are prealigned. Due to handling, however, a magnet may be rotated off position. Rotate the magnets to improve alignment ONLY IF ABSOLUTELY NECESSARY. It should not be necessary to use the centering rings on the yoke to align the display.

CAUTION

Turning the Monitor on with line voltage higher than 132V ac when the line voltage selection switch is in the 110 position will damage the power supply. If the voltage is set for 180 to 264V and 90 to 132V is applied, the unit may not operate.

NOTE

Allow the Monitor to warm up for at least 10 minutes. During the first 5 minutes of operation, raster lines may be visible on the display. This is common to crt displays and is not a fault.

The display can be adjusted using a program-generated monitor alignment pattern. The pattern consists of four outlined boxes, two across and two down. Each box is 40 characters wide by 12 lines high. Table 4-3 contains the required monitor alignment program. An alignment pattern can also be generated by a program on the 9100A Service Utility disk, which is part of the 9100A Service Kit (see Troubleshooting).

This program is used with the Alignment Template, P/N 777144. When the display is properly adjusted, the four boxes displayed by the program fit evenly and symmetrically within the inner lines of the template.

Table 4-3. Monitor Alignment Program

```
program alignment

!***************************************************************************
!*  This program generates an alignment pattern on the monitor. The        *
!*  pattern consists of four outlined boxes, two across and two down;      *
!*  each box is 40 characters wide and 12 lines high.                      *
!***************************************************************************

HL9 = "\8A"+"\8A"+"\8A"+"\8A"+"\8A"+"\8A"+"\8A"+"\8A"+"\8A" ! 9 horiz. lines
Top_s = "\86"+"\8A"+ HL9 + HL9 + HL9 + HL9 +"\8A"+"\8C"  ! top of box string
Bot_s = "\83"+"\8A"+ HL9 + HL9 + HL9 + HL9 +"\8A"+"\89" ! bottom of box string
Ctr_s = "\85                                      \85" ! center of box string
EoS_s = "\1B[2;30H Monitor \1B[4C Alignment \1B[10B"  ! End of Screen string
L12_s = ""                                         ! Line 12 string

open device "/term2", as "output"       ! open channel to print to monitor

print using "\1B[H\1B[J"        ! cursor to top left, and clear monitor screen

loop for s = 0 to 1             ! do top half and then bottom half of pattern
  print Top_s,Top_s             ! print top line of left and right boxes
  loop for l = 2. to 11.
    print Ctr_s,Ctr_s           ! fill in center of left and right boxes
  end loop
  if s > 0 then L12_s = EoS_s   ! if this is the End of the Screen, then
                                !   need to print title and position cursor.
  print Bot_s,Bot_s,L12_s       ! print bottom line of left and right boxes

end loop                        ! if this was the top half, do the bottom

end program
```

Alternately, any monitor display pattern can be used when the programmed pattern is not available. This method involves display and adjustment of the monitor screen for a centered display of the correct size. The alternate pattern used must measure 80 columns wide by 24 rows high to allow for correct adjustment.

The monitor display is adjusted using the following seven controls:

- Vertical Linearity
- Vertical Size
- Brightness
- Focus
- Horizontal Phase
- Horizontal Size
- Horizontal Linearity
- Contrast

The first six of these controls can be adjusted externally through holes in the monitor chassis (shown in Figure 4-7). Adjusting horizontal size requires hex adjustment tool (P/N 572321). Contrast is an external operator adjustment. Adjusting all other controls requires the use of an adjustment tool (P/N 800540).

The monitor chassis must be opened to adjust the Horizontal Linearity control. Refer to "Accessing the Monitor Chassis". Adjusting the Horizontal Linearity control requires the use of the hex adjustment tool (P/N 572321).

As some adjustments may interact with others, repeating the procedure may be necessary. For either display method, use the following steps to adjust the display:

1. If necessary, remove the monitor cover. Then, locate the external display adjustment holes. See Figure 4-7.

2. Cover a flat surface with a soft cloth to protect the monitor screen. Place the Monitor face down.

3. Open the Monitor by using a Phillips screwdriver to remove the five screws on the rear panel. Swing the bottom chassis cover down. Do not remove the power panel.

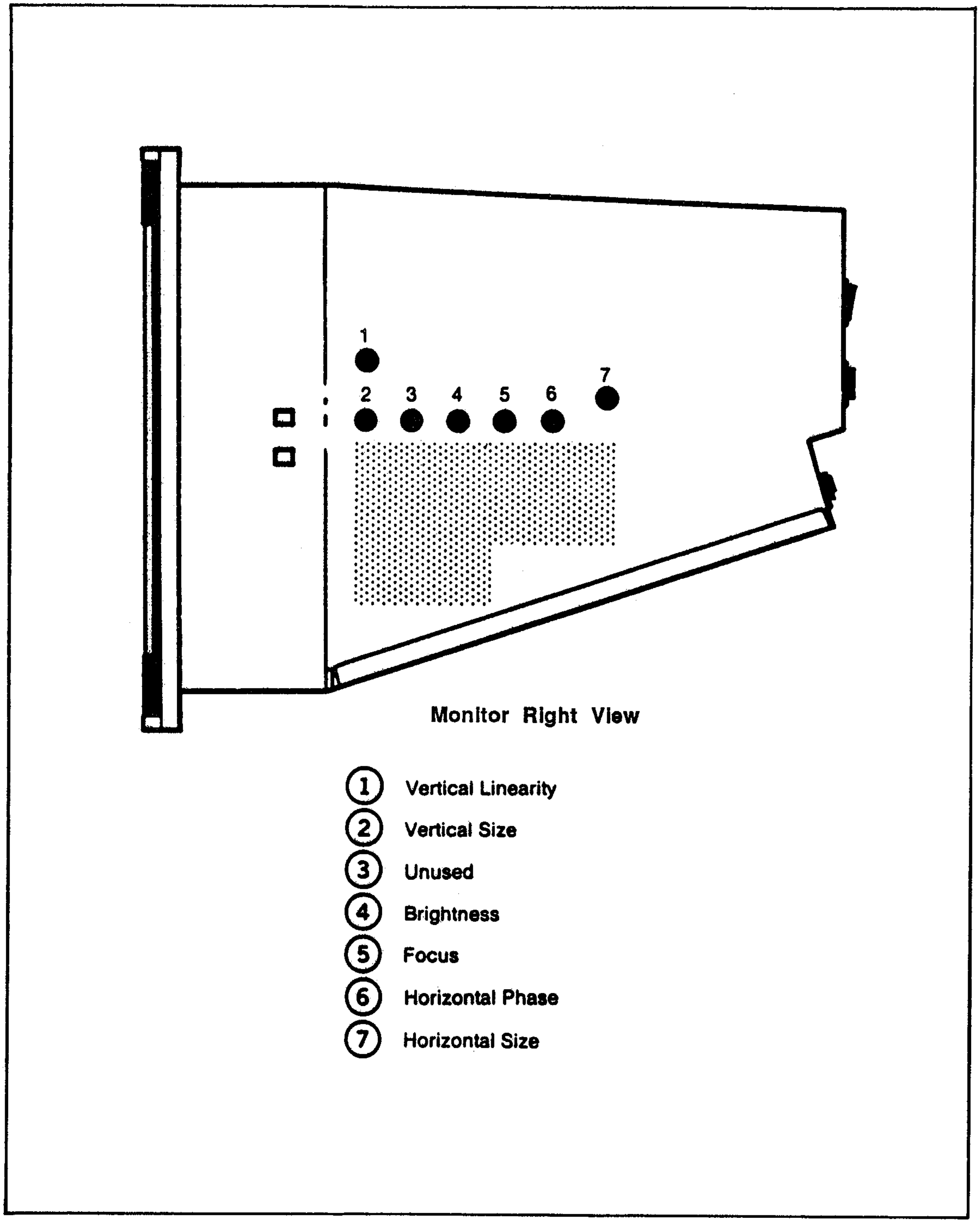


Figure 4-7. External Display Adjustment Locations

4. Perform the following yoke adjustment only if the screen appears tilted.

   a. Loosen the clamp around the yoke of the crt using a 3/16-inch nut driver.

   b. Turn the Monitor so that the display can be seen.

   c. Rotate the yoke slightly to adjust for the screen tilt.

d. Check that the tightening screw is easily accessible, then tighten the clamp to a torque of 6 inch-pounds (0.678 n-m). Do not overtighten the screw, or the neck of the crt may crack.

WARNING

TO AVOID INJURY, USE CAUTION WHEN HANDLING THE CRT. WEAR PROTECTIVE CLOTHING AND SAFETY GLASSES OR A FULL FACE SHIELD. AVOID STRIKING THE CRT ON ANY OBJECT THAT MIGHT CAUSE IT TO CRACK OR IMPLODE. NEVER HANDLE THE CRT IN AN UNSAFE AREA, SUCH AS ONE WITH WET FLOORS, HIGH ACTIVITY, ETC. NEVER HANDLE THE CRT AROUND OTHERS WHO MAY NOT BE PROPERLY PROTECTED. AVOID SCRATCHING THE TUBE OR CAUSING OTHER DAMAGE DURING INSTALLATION.

NOTE

Display tilt may be slightly affected by the orientation of the Monitor, especially in environments containing a high density of metal. Rotate the unit and try to find a position where the tilt is in the center between extreme clockwise tilt and extreme counterclockwise tilt. Perform alignment in that position. If no difference is perceived between the two extremes, proceed in the most convenient orientation.

5. Locate the Horizontal Linearity control on the Display PCA (see Figure 4-7.) Adjust Horizontal Linearity so that the left half of the display is the same size as the right half of the display. Since the open chassis cover has a slight effect on Horizontal Linearity, close the chassis cover to verify Horizontal Linearity and keep it closed for the remainder of the procedure. Linearity is also slightly affected by the unit being upside down.

6. Adjust Horizontal Phase to line up the center gaps between the boxes with the alignment centering marks on the bezel. If an alternate pattern is being used, use Horizontal Phase to center the display.

7. Adjust Vertical Linearity so that the boxes (or regions of the alternate pattern) appear the same.

8. Adjust Vertical Size to make the alignment pattern (or alternate pattern) about 5 1/8 inches (130 mm) high.

9. Adjust Horizontal Size to make the alignment pattern (or alternate pattern) about by 7 3/4 inches (195 mm) wide.

10. Set the Brightness control for a slight amount of "blooming" with the Contrast (external operator control) set to maximum.

11. Adjust the Focus control with Contrast set for normal viewing.

12. Use a Phillips screwdriver to replace the five rear panel screws.

NOTE

If the Monitor was adjusted with the unit upside down, a final Horizontal Phase adjustment will probably be necessary.

13. Reinstall the monitor cover.

DECIDING ON CRT REPLACEMENT

The crt should be replaced if any of the following occur:

- If an image has been burned into the phosphor and the image on the display is unacceptably altered.
- If scratches are detectable by a pass of the finger. (Scratches can create a safety hazard that lessens the ability of the crt to withstand implosion.)

The crt may require replacement when any of the following occur:

- Ghost images appear on the display.
- Brightness levels are unacceptable.

NOTE

Insufficient brightness can be caused by several factors. After 10,000 hours of continuous excitation of the phosphor, crt brightness can be expected to have dropped by approximately 50 percent. Failures in the Display PCA can also cause loss of brightness.

A properly functioning crt requires ten minutes to warm up completely. During the first five minutes, raster lines may appear on the display. This is common to crt displays and is not a fault. If the display takes more than five minutes to achieve full brightness, suspect either a crt or Display PCA failure.

NOTE

Monitors are preset at the factory for the same brightness at maximum contrast. Due to crt variations, the Display PCA brightness control will not be in the same position for all units and the raster may be visible for varying amounts of time, if at all.

NOTE

Because the maximum brightness of the crt will vary from unit to unit, the decision to replace a display on the basis of insufficient brightness is subjective.

SELF TEST ROUTINES

Power-Up Self Test

At power-up, the 9100A/9105A sequences through a series of self tests. A display response is presented for any test that fails. These responses (and related meanings) are presented in Table 4-4. In addition, a Mainboard ROM and Display Response test is run. A failed test in this instance is evidenced by simultaneously flashing RUN UUT and DISK ACCESS LEDs.

Probe Self Test

The Probe Self Test verifies that the Probe is connected and is communicating with the system. Use the following procedure:

1. Press the MAIN MENU key.

2. Press the left arrow (<--) key until the cursor rests on the first (left-most) field. Then, with the cursor on this field, press the SELFTEST key.

3. Press the right arrow (-->) key to move the cursor to select the next field, then press the PROBE key. Check that the display reads:

   MAIN: SELFTEST PROBE

4. Press the ENTER key to initiate the self test.

   - If the self test fails, a failure message is displayed. Check the probe connection and repeat the test.
   - If the test fails a second time, the Probe requires service.

Table 4-4. Power-Up Self Test Responses

selftest: testing memory . . .

This message is displayed during the simple read/write test of the RAM.

------Press any key to continue test------
or the RESET key for the next test

If an error was detected during the RAM test, pressing the RESET key aborts the RAM test and sequences the 9100A/9105A to the next test in the power-up self test series. Pressing any other key continues the test at the next higher RAM location.

selftest: ram read/write error @

A RAM read/write test has failed at the specified address. The memory test itself is extremely primitive. A long word with a value of '5a5a5a5a' is written and read back, followed by a long word with the value 'a5a5a5a5'. Any bit that cannot be written either high or low is considered defective.

selftest: r/w error on pod cmd port:

Of the command bits that are tested on the pod port, one or more have failed a read/write test. The mask of the failing bit(s) is displayed in hex.

selftest: r/w error on pod data port:

One or more bits in the pod data port have failed a read/write test. An error mask of the offending bit(s) is displayed in hex.

selftest: data error in uart u7
should be: xxxx not: xxxx

An error occurred while the UART was in its digital loopback self-test mode. The data written has not matched the data read in device U7, and the two datum are displayed on the second line of the display.

selftest: data error in uart u12
should be: xxxx not: xxxx

An error occurred while the UART was in its digital loopback self-test mode. The data written has not matched the data read in device U12, and the two datum are displayed on the second line of the display.

selftest: timed out waiting for uart

One of the UART transmit registers has not cleared in a reasonable amount of time. The UART clock could be disabled, or the chip itself could be bad.

Table 4-4. Power-Up Self Test Responses (cont)

selftest: probe i/o board not responding

A simple read/write test to both of the gate array chips on the Probe I/O PCA has failed.

selftest: ram test bus error@

An unexpected bus error occurred during the power up RAM test. This could be a result of setting the RAM size in the EEPROM too large, or it could be a problem with the memory decoding circuitry.

selftest: front display not responding

The front panel display processor has not returned the expected character within a reasonable amount of time.

selftest: probe i/o stop counter failure

The high speed stop counter in the start-stop logic has failed. To test the stop counter on the Probe I/O PCA the counter is soft clocked and checked for proper response. The counter is preset to a value of two. The clock is soft stepped once and the stop counter is checked to insure it has not triggered. Another clock is produced and the stop counter is checked for an active condition.

selftest: probe i/o logic chip inactive

In the process of setting up the stop counter test, it is necessary to set the start-stop state machine inside the U19 gate array to state 1 (start received, waiting for stop). If the state machine is not in state 1 after clocking, an error is assumed somewhere in the start-stop logic subsection.

selftest: floppy controller failure

A simple read/write test to several of the floppy controller registers has failed.

selftest: floppy controller not responding

A bus error occurred while trying to read or write the floppy controller.

Table 4-4. Power-Up Self Test Responses (cont)

selftest: stuck vector:

The floppy controller is given a force interrupt command. If the resultant vector is not the floppy controller interrupt vector, then it is assumed that another interrupt is active. At this point in the self test, no interrupts should be active, and this is considered an error. The force interrupt command is followed by a reset interrupt command. After this command no interrupts should be active, and any active interrupts are again considered error conditions. In both conditions the number reported is the actual physical vector address.

selftest: uarts not responding

A bus error occurred while trying to read or write either of the UART devices.

selftest: front display ram test failure

An error code was returned by the front panel display when asked to perform an internal RAM test.

Pod Self Test

This test performs a comprehensive pod check. Test failure is evidenced by an error message. (See the respective pod manual for full error descriptions). Proceed as follows:

1. Make all connections. Ensure that the Pod is attached to the mainframe and that the pod UUT connector is inserted and locked into the pod self-test socket. The pod manual and the 9100A/9105A Getting Started guide illustrate these connections further.

2. On the 9100A/9105A, first press MAIN MENU, then move the cursor to the first (left-most) field using the left arrow (<--) key.

3. Press the SELFTEST key.

4. Move the cursor one field to the right and press POD. Check that the display reads:

   MAIN: SELFTEST POD

5. Press ENTER to initiate the self test.

   o If the self test fails, a failure message is displayed. Check the pod connection and repeat the test.

   o If the test fails a second time, the Pod requires service.

I/O Module Self Test

The I/O Module Self Test verifies that the I/O Module is connected and is communicating with the system. Use the following procedure:

1. Press MAIN MENU, then move the cursor to the first (left-most) field using the left arrow (<--) key.

2. Press SELFTEST.

3. Move the cursor one field to the right and press I/O MOD.

4. Move the cursor one more field to the right, and press the number of the I/O Module to be tested. Check that the display reads:

   MAIN: SELFTEST I/O MOD <n>

   (where <n> signifies the number of the I/O Module)

5. Press ENTER to initiate the self test.

   - If the self test fails, a failure message is displayed. Check the I/O Module connection and repeat the test.

   - If the test fails a second time, the I/O Module requires service.

Display Self Test

Several software tests aid in testing the Display Board. Each test can be selected by a command sent through the display processor serial port. The "Test" command, 0x0e, followed by a test number ascii 1-9 (or 0x31-0x39) selects the test.

The tests are available through a program in the 9100A Service Kit. They can also be initiated using a 68000 Pod plugged into the mainframe. The Pod must initialize the DUART before sending the serial command to the Display Board. These tests are not available through TL/1; the Control N (0x0e) command is not sent to the display.

Tests 1 (ROM) and 2 (RAM) are also performed by mainframe software during the mainframe self test following a reset. At this time, the mainframe also performs Test 9 (look for Synchronous Special Function key) to determine if a boot should be forced off the floppy drive instead of the hard disk.

Tests 4, 5, and 6 are useful for troubleshooting the keyscan and display refresh hardware. They are available by grounding Test Point 6 (TP6) during a reset, as well as by software control.

All display tests are listed and described in Table 4-5.

Table 4-5. Display Self Test

Test 0 - Sends Out Software Revision Number

The number is returned to the serial port just like a key press.

Test 1 - Verifies ROM Internal Checksum

Returns 0x70 (p) to the serial port if test passed, 0x71 (q) if it didn't.

Test 2 - Performs Quick RAM Test

This is a non-destructive test of the Display RAM. It writes the compliment of the present data, reads it back, re-writes the original data, and then reads that back. Returns 0x72 (r) to the serial port if the test passed, 0x73 (s) if it didn't.

Test 3 - Performs Long RAM Test

This is a more complete, destructive test of the Display RAM. It performs a test similar to the 9100 RAM FAST on the RAM and returns 0x74 (t) to the serial port if the test passed, or 0x75 (u) if the test did not pass.

NOTE

Tests 4, 5, and 6 cause the software to exit mainframe control. The Display Board does not respond to further commands or data until the test is exited by keyboard control or by a reset. All three tests are destructive, in that they write over the present display.

Also, tests 4, 5, and 6 can be accessed by grounding the TEST testpoint and resetting (or powering on) the display.

Test 4 - Jump to Key Test Routine

This is the mode entered when TP6 is grounded during a reset. This test displays the row and column of the key being pressed on the display.

The RESET key causes this test to terminate and Test 5 to start.

Table 4-5. Display Self Test (cont)

Test 5 - Jump to Display Lines Routine

The following key-pattern relationships are applicable during this test:

- Keys 1, 2, and 3 each display a vertical bar in every third column. For example, key 1 display bars in columns 1, 4, 7, and so on. Keys 2 and 3 control columns beginning at 2 and 3, respectively.

- Keys 4, 5, and 6 display a series of horizontal bars, also spaced three lines apart.

- Key 0 turns all lines off (blank display).

- Key 7 turns all lines on and is the default when test 5 is entered.

NOTE

This mode is useful if the display has a "burned in" problem. Since this mode does not time out, leaving the display in this mode overnight makes for a more even display.

- The EXEC Key returns to Test 4.

- The ALPHA Key jumps to Test 6.

- The RESET Key exits these tests entirely and returns the display to mainframe control.

Test 6 - Jump to V-H Lines Routine

This routine identifies the bad grid drivers or row drivers. The arrow keys are used to move among the displayed cross hairs. Pressing the HELP key displays the names of the two grids and one row driver which should be on to illuminate the dot at the intersection of the cross hairs. The RESET Key returns to Test 5.

Test 7 - Unlock Keyboard

If the keyboard has been locked by test 8, this command re-enables the key scan. It returns 0x76 (v) as an acknowledge byte.

Table 4-5. Display Self Test (cont)

Test 8 - Lock Keyboard

This command disables key scan and prevents the display board from sending any key press information. It is used by the mainframe to ensure that only test routine data is received. It returns 0x77 (w) as an acknowledge byte.

Test 9 - Report Synchronous Special Function Key

This function returns a 0x79 (y) if the processor has seen the special function key press since the last inquiry or reset. It returns a 0x78 (x) if it has not seen it. The Special function results from the SOFT KEYS, F2, and F4 keys being pressed simultaneously.

CALIBRATION

Individual level and time delay variations associated with the Probe, I/O Module, and Pod can be compensated for with the calibration adjustments presented in the following paragraphs. The following six calibrations are covered:

- Probe offset correction calibration
- Probe compensation calibration
- Probe to external clock module calibration
- Probe to Pod calibration
- I/O Module external calibration
- I/O Module to Pod calibration

The calibrations listed above fall into three categories. Offset correction calibration stores a correction value in non-volatile memory. Compensation calibration matches impedances. Data against clock delay calibration, performed in software, ensures that both data and the signal clocking the data arrive at the receiving hardware at the same time.

Probe compensation remains stable and is necessary only when a Probe is first connected to the mainframe. The software calibration procedures are intended to be performed by the system operator and do not require any test equipment.

Software calibration should be performed when the system is first set up and at regular intervals (at least monthly) thereafter. Calibration is also necessary whenever devices attached to the system are changed or repaired.

The system can also be calibrated by restoring data generated by previous calibrations. This process, described under "Saving and Restoring Calibration Data" later in this section, should be performed after each power-up or reset and before UUT testing or troubleshooting.

Probe Offset Correction

Probe offset correction calibration calculates the offset voltage of the Probe input circuitry and stores the value in an EEPROM. This procedure is required only if the Probe I/O or Main PCAs are repaired or replaced.

A utility program is required to perform the probe offset correction calibration. This utility program is included on the 9100A Service Utility disk, which is part of the 9100A Service Kit (see Troubleshooting).

Probe Compensation

This calibration procedure matches the impedance of the Probe to that of the cable connecting the Probe to the system. Probe impedance is adjusted with COMP ADJ, a trimmer capacitor located on the side of the system.

Figure 4-8 shows oscilloscope connections used during probe compensation. To compensate the Probe, use the following steps:

1. Ensure that the oscilloscope and its Probe are properly calibrated.

2. Connect the oscilloscope probe tip to the system CAL OUT post. Then connect the oscilloscope probe common to the system GND post. Both posts are accessible through labeled holes in the side of the mainframe.

3. Press the MAIN MENU key, and use the left arrow key to move the cursor to the left-most field.

4. Press the CAL softkey.

5. Use the right arrow key to move the cursor to the next field, and press the PROBE softkey.

6. Move the cursor to the next field, and press the COMP softkey. The display should now read:

   MAIN: CAL PROBE COMP

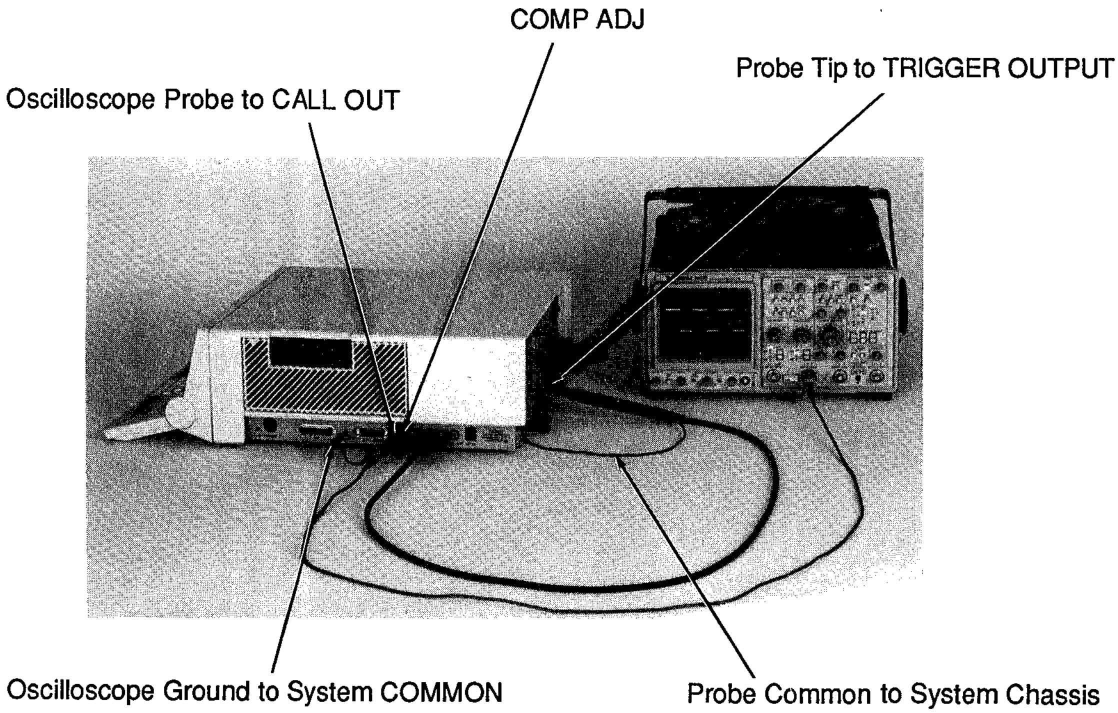


Figure 4-8. Oscilloscope Use in Probe Compensation

7. Press the ENTER key. The display should read:

```
MAIN: CAL PROBE COMP
CONNECT PROBE TO TRIGGER OUTPUT
ADJUST COMP, PRESS STOP WHEN DONE
```

8. Insert the probe tip into the central (innermost) conductor of the TRIGGER OUTPUT at the rear of the 9100A/9105A. Leave the Probe in this position.

9. Adjust the oscilloscope's horizontal and vertical settings until an approximate square wave is displayed. Then use an adjustment tool on COMP ADJ to obtain an underdamped square wave with 10% overshoot. For the adjustment tool, use Fluke Part Number 800540. The square wave should bear similarity to Figure 4-9.

10. When you have finished the square wave adjustment, press the STOP key on the operator's keypad. The display should read:

```
MAIN: CALIBRATION COMPLETE
```

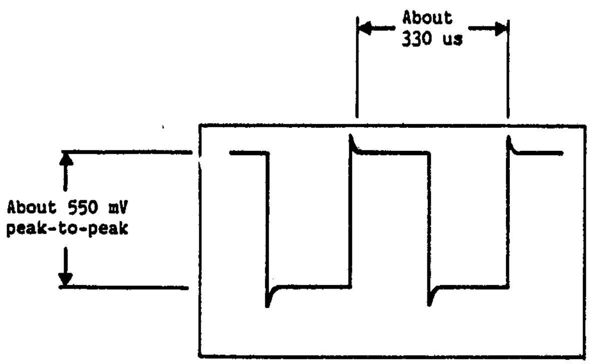


Figure 4-9. Probe Compensation Square Wave

Software Calibration

The Probe Compensation adjustment and the Probe Offset Calibration are the only hardware calibrations required for the 9100A/9105A. All other calibration is performed in software and is lost if the system is turned off, restarted, or reset. The software calibration data can be saved on disk and restored from disk to recalibrate the system. However, the restored calibration data must only be used with the system on which the calibration was performed. Any change in system hardware (Interface Pod, I/O Module(s) Clock Module, or Probe) requires system recalibration; the resulting new calibration data should be saved.

All of the software calibration procedures are intended to be performed by the system operator and do not require test equipment. Pod-related calibration procedures require the use of a known good Unit Under Test (UUT).

PROBE TO EXTERNAL (CLOCK MODULE)

This calibration automatically calibrates the Probe's internal data delay to the external clock delay. The clock signal input is through the Clock Module, which must be connected to the system. Perform the calibration as follows:

1. Press the MAIN MENU key, and use the left arrow key to move the cursor to the left-most field.

2. Press the CAL softkey.

3. Move the cursor to the next field, and press the PROBE softkey.

4. Move the cursor to the next field, and press the TO EXT softkey. The display should read:

   MAIN: CAL PROBE TO EXT

5. Press the ENTER key. The display should read:

   MAIN: CAL PROBE TO EXT
    CONNECT EXTERNAL CLOCK TO PROBE TIP AND
    COMMON LINES TOGETHER. PRESS BUTTON.

6. Connect the Probe to the Clock Module CLOCK line.

7. Connect the probe ground clip to the Clock Module COMMON line.

8. Press the probe ready button (side of Probe). The display should read:

   MAIN: CALIBRATION COMPLETE

PROBE TO POD

This procedure automatically calibrates the Probe's internal data delay to the Pod's PodSync line, which the system sometimes uses as a clock signal. Use the following steps to perform the calibration:

1. Connect the Pod to a UUT.

2. Press the MAIN MENU key, and use the left arrow key to move the cursor to the left-most field.

3. Press the CAL softkey.

4. Move the cursor to the next field, and press the PROBE softkey.

5. Move the cursor to the next field, and press the TO POD softkey. The display should read:

   MAIN: CAL PROBE TO POD ADDR

   The last field is pod dependent and softkey selectable.

6. Press the ENTER key. The display asks you to probe the UUT at a point where the selected PodSync appears. The message is pod dependent, a possible example being:

   MAIN: CAL PROBE TO POD ADDR
    CONNECT PROBE TO ALE
    PRESS PROBE BUTTON WHEN READY

7. Connect the probe common clip to the UUT common.

8. Probe the specified pod line as directed. You may need to refer to the UUT schematic for convenient probing locations.

9. With the probe tip touching the point being probed, push the probe ready button.

10. You may have to repeat steps 8 and 9, probing at different locations each time. When calibration is complete, the display should read:

    MAIN: CALIBRATION COMPLETE

11. Repeat steps 5 through 10 for each SYNC mode in which the 9100A/9105A is to be operated.

I/O MODULE TO EXTERNAL

This procedure calculates the proper setting for the I/O Module's internal clock delay for use whenever the SYNC I/O MOD TO EXT command is entered. This calibration requires the use of the Calibration Module supplied with the I/O Module. To perform the calibration:

1. Press the MAIN MENU key, and use the left arrow key to move the cursor to the left-most field.

2. Press the CAL softkey.

3. Move the cursor to the next field, and press the I/O MOD softkey.

4. Move the cursor to the next field, and press the EXT softkey. The display should read:

    MAIN: CAL I/O MOD TO EXT

5. Press the ENTER key. The display should read:

    MAIN: CAL I/O MOD TO EXT
    INSTALL CAL HEADER IN DESIRED I/O MODULE
    PRESS BUTTON WHEN READY

6. Fit the Calibration Module over the I/O Module to be tested.

7. Press the ready button on the Calibration Module. When the calibration is complete, the BUSY light should go off, and the display should read:

    MAIN: CALIBRATION COMPLETE

I/O MODULE TO POD

This procedure calculates the proper settings for the I/O Module's internal clock delay for use with the SYNC I/O MOD TO EXT and the SYNC I/O MOD TO POD commands. When either is entered, the appropriate delay is selected. This calibration procedure requires use of the Calibration Module. Perform the calibration as follows:

1. Connect the Pod to a UUT.

2. Press the MAIN MENU key, and use the left arrow key to move the cursor to the left-most field.

3. Press the CAL softkey.

4. Move the cursor to the next field, and press the I/O MOD softkey.

5. Move the cursor to the next field, and press the POD softkey.

6. Move the cursor to the next field, and press the desired softkey. For example, if you intend to use the 9100A/9105A in SYNC I/O MOD TO POD ADDR mode, press the ADDR softkey. In this case, the display should read:

   ```
   MAIN: CAL I/O MOD TO POD ADDR
   ```

7. Press the ENTER key. This display should read:

   ```
   MAIN: CAL I/O MOD TO POD ADDR
    INSTALL CAL HEADER IN DESIRED I/O MODULE
    PRESS BUTTON WHEN READY
   ```

8. Plug the Calibration Module into the I/O Module, and press the Calibration Module ready button. Make sure the calibration lead on the Calibration Module is unconnected when pressing the ready button.

9. After a few seconds, a pod dependent message is displayed. For example, the display may read:

   ```
   COMPLETED EXT CAL PRIOR TO CAL POD
    NOW CONNECT CAL LEAD TO ~S1
    PRESS BUTTON WHEN READY
   ```

10. Refer to a schematic of the UUT and locate the specified signal. At a suitable point on the UUT, attach the calibration lead to this signal.

11. Press the Calibration Module ready button. After several seconds, the display should read:

   ```
   MAIN: CALIBRATION COMPLETE
   ```

12. Repeat steps 6 through 11 for each SYNC mode in which the 9100A/9105A is to be operated.

SAVING AND RESTORING CALIBRATION DATA

Calibrating the 9100A/9105A at every power-up or reset is not necessary. A more convenient procedure is to restore calibration data from the user disk after the self tests have been performed and the system configured.

Each calibration generates data, which can be saved on the user disk using the SETUP MENU key. Once the system is calibrated for a given Pod, Probe, Clock Module, and I/O Module, the data is good until one or more of those devices is changed.

Invalid Calibration Data

The calibration data restored from the user disk may be invalid if any of the following conditions apply:

- After the data was saved, one or more system components (Pod, Probe, I/O Module, Clock Module) were changed. This condition includes moving or exchanging I/O Modules, such as moving an I/O Module from connector 1 to connector 2.
- The system has never been calibrated.
- The system was last calibrated more than one month ago.

Saving Calibration Data

Save calibration data on the disk as follows:

1. Press the SETUP MENU key, and use the left arrow key to move the cursor to the left-most field.
2. Press the SAVE softkey.
3. Move the cursor to the next field, and press the CALDATA softkey.
4. Move the cursor to the next field, and press one of the following softkeys:

   USERDISK — This key is used if the user disk does not contain a UUT directory. The resulting display should read:

   SAVE CALDATA IN USERDISK

   UUT FILE — This key is used if the user disk contains a directory for the UUT.
5. If you pressed the UUT FILE softkey in step 4, type the UUT directory name. For example, type DEMO. The display should read:

   SAVE CALDATA IN UUT FILE DEMO
6. Press ENTER to save calibration data.

Restoring Calibration Data

Use the following procedure to restore calibration data from a user disk:

1. Press the SETUP MENU key, and use the left arrow key to move the cursor to the left-most field.

2. Press the RESTORE softkey.

3. Move the cursor to the next field, and press the CALDATA softkey.

4. Move the cursor to the next field, and press one of the following softkeys:

   USERDISK — Use this softkey if the calibration data was saved in the USERDISK directory. The resulting display should read:

   RESTORE CALDATA FROM USERDISK

   UUT FILE — Use this softkey if the calibration data was saved in a UUT directory.

5. If you pressed the UUT FILE softkey in step 4, type the UUT directory name. For example, type DEMO. The display should read:

   RESTORE CALDATA FROM UUT FILE DEMO

6. Press ENTER to restore the previously saved calibration data.

TROUBLESHOOTING

This manual does not contain troubleshooting procedures. Component level troubleshooting is supported by the 9100A Service Kit, P/N 818948. The Service Kit uses Guided Fault Isolation (GFI) programs to assist in troubleshooting 9100A/9105A systems. The Service Kit contains GFI and utility programs, an extender board, and instructions. To use the Service Kit, another 9105A or 9100A, an I/O Module (9100A-003), and a 9000A-68000 Interface Pod are required.

REPAIR

General Repairs

STATIC AWARENESS

Improper handling of components or assemblies may cause instantaneous or delayed electrostatic discharge damage. The yellow "Static Awareness" sheet inserted near the front of this manual explains some of the hazards associated with static electricity and sensitive components.

COMPONENTS

Several of the assemblies in the 9100A/9105A are built with surface mount components. See the following Surface Mount Repair information concerning mechanical design and repair of these components.

Surface Mount Repair

SURFACE MOUNT TECHNOLOGY

Surface Mount Technology (SMT) is a new component packaging and manufacturing technique that continues the trend towards miniaturization of electronic components. Although the "chip" inside the component package is the same as used with other techniques, the package is much smaller. The leads of an SMT component are soldered to the surface of a circuit assembly, rather than being inserted and soldered into holes in the circuit assembly.

Component Packages

Most common electronic components are available in Surface Mount Technology. The SMT component packages used in the 9100A are illustrated and described in the following paragraphs.

The Small Outline Integrated Circuit (SOIC) package is rectangular with gull wing shaped leads, spaced 0.05 inches on center. The SOIC comes in a narrow body package with 8 to 16 leads, and in a wide body package with 14 to 28 leads. See Figure 4-10.

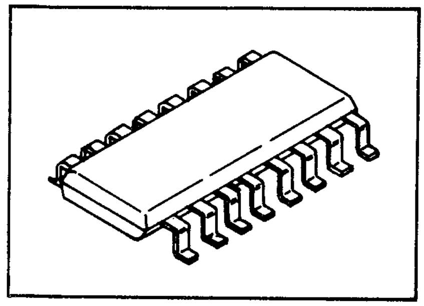


Figure 4-10. Small Outline Integrated Circuit (SOIC)

The Plastic Leaded Chip Carrier (PLCC) package is square or rectangular in shape, with 0.05 inch on-center leads located on all four sides. The leads are formed in a "J" shape, wrapping underneath the body. The PLCC is used for for large devices with 20 to 84 leads. See Figure 4-11.

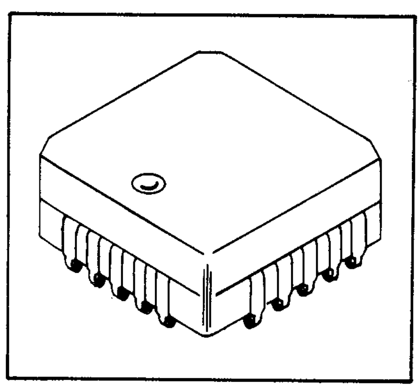


Figure 4-11. Plastic Leaded Chip Carrier (PLCC)

Not all ICs are available in surface mount packages. Therefore, some printed circuit assemblies use a mixture of DIP packages and SMT devices. A DIP packaged IC that has been modified for surface mounting (leads cut short) is called a butt-soldered dual inline package. See Figure 4-12.

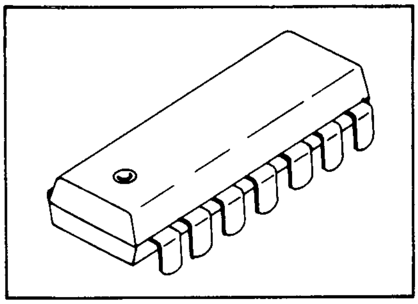


Figure 4-12. Butt-Soldered DIP

Transistors and diode pairs are packaged in several sizes of Small Outline Transistor (SOT) packages. The SOT-23 package, shown in Figure 4-13, is the most common package for small signal transistors; the leads are grouped with the collector on one side and the base and emitter leads on the opposite side.

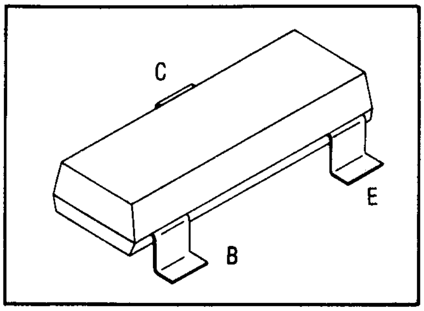


Figure 4-13. Small Outline Transistor (SOT)

Signal diodes, rectifiers, and zeners are packaged in a cylindrical Metal Electrode Face bonded (MELF) package. The stripe indicates the cathode end. See Figure 4-14.

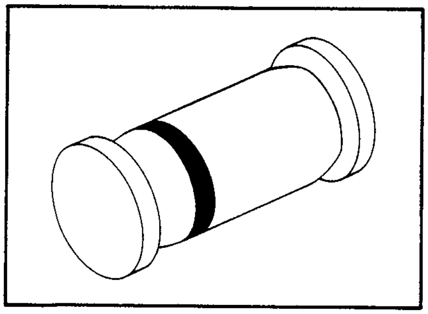


Figure 4-14. Metal Electrode Face (MELF)

Resistors and capacitors are packaged in rectangular ceramic leadless bodies, commonly called chips. See Figure 4-15.

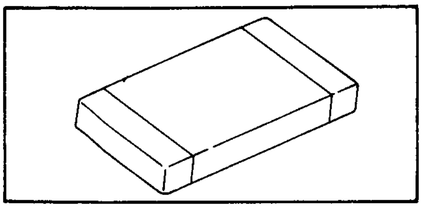


Figure 4-15. Chip Component

Printed Circuit Assembly Design

Surface Mount Technology impacts the way printed circuit assemblies are designed. Assembly layout is simplified because conductive traces do not have to be routed around protruding component leads. As a result, surface mount assemblies typically have fewer layers. The assembly layers are interconnected with plated through-holes called vias. The reduction of component lead spacing from 0.1 to 0.05 inches has shrunk traces and spacings to approximately half the previous size.

Fluke has developed a circuit pad "footprint" for surface mount components that aids both test and repair. This circuit layout uses staggered test pads and vias to make room for test probes. A probe can make contact with either a test pad or a via, avoiding the component lead and preventing an open solder connection from being temporarily closed and hidden by direct pressure on a component lead. Most signal paths do not appear on the outer surfaces of the assembly; vias connect the component pads to the signal paths on the inner layers. See Figure 4-16.

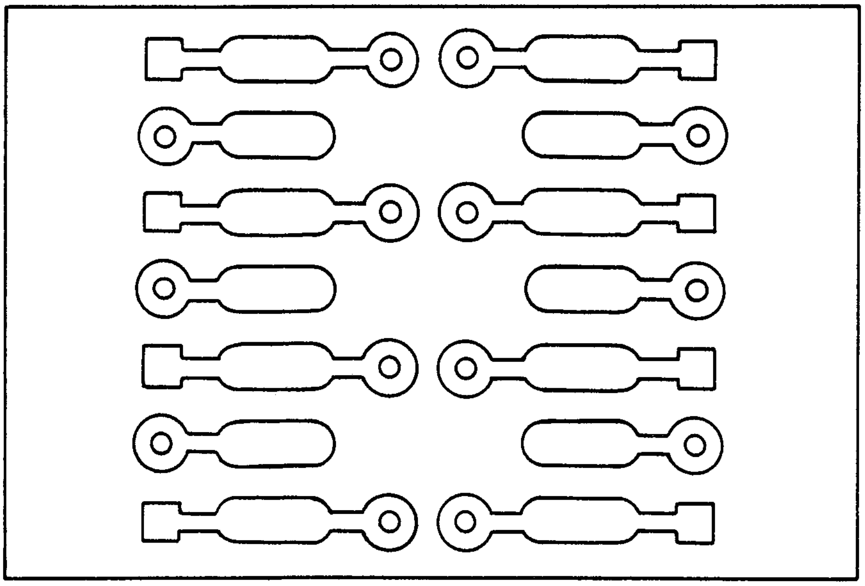


Figure 4-16. Surface Mount Footprint

SMT and Serviceability

SMT offers increased quality and reliability. When it becomes necessary, servicing can be accomplished quickly and reliably. Surface mount assemblies have a high component density, making replacement costly. However, the component level repair of these assemblies is not difficult and does not require involved training or large expense. Repair techniques for surface mount assemblies are described later in this section.

Troubleshooting SMT

Functionally, there is no difference between an IC in a DIP package and the same device in a surface mount package. Therefore, related troubleshooting techniques are very similar. Any differences in troubleshooting are related to size and mechanical construction.

When troubleshooting an SMT assembly, the circuit should be probed on the test pads or vias next to the component leads, rather than directly on the lead. This prevents disguised failures resulting from probe pressure on the lead closing a defective solder connection.

Special servicing precautions must be followed because of the reduced lead spacing on components and smaller printed circuit assembly pads and traces. Special care must be taken in the following areas:

- Ordinary test probes can easily short two adjacent leads or pads.
- Standard soldering irons and desoldering tools can damage the small pads of a SMT assembly.

Component Identification

Do not allow components to become mixed. Due to their size, chip components are often not marked. It is even difficult to distinguish a resistor from a capacitor. Use a clean work area, and keep the chip components in labeled packages. With limited space available, the assemblies seldom provide silk-screened reference designators for chip components. Technicians must rely on the circuit assembly layout drawings and parts lists for chip component locations and values.

Surface mount ICs are marked with the device number, but their leads are indexed differently from those on DIP packages. On the PLCC package, pin number one is indicated by a dimple in the plastic called an index dot. See Figure 4-17.

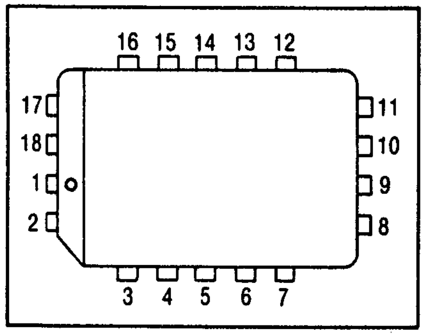


Figure 4-17. PLCC Lead Index

Pin number one on the SOIC package is located on the far left of the beveled side. SOIC packages do not have a notch or dimple to indicate pin one. See Figure 4-18.

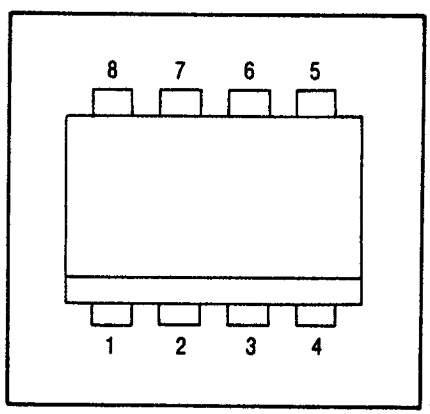


Figure 4-18. SOIC Lead Index

REPAIR TECHNIQUES

Although surface mount assemblies are repaired with somewhat different tools and techniques than through-hole printed circuit assemblies, the techniques and tools required are not complicated. In fact, a surface-mounted IC can be removed and replaced much faster and easier than a DIP package. Surface mount repair is simpler in that no through-hole solder must be removed.

Solder flux is used chemically to clean both the component lead and the solder. The flux removes oxides from the metals and acts as a wetting agent. With SMT, only enough solder to make a positive metallic contact is necessary; too much solder can cause bridging. Also, solder provides the only mechanical fastening for SMT; too little solder can cause weak or open solder joints.

Rework of SMT assemblies is often performed under a five-inch illuminated magnifier lamp. The lamp is used when applying the solder, positioning the component, or inspecting the finished rework.

Hot air from a heat gun is used to reflow the solder. This technique, called convection reflow, requires careful application of controlled heat. Excess heat can damage components, other solder joints, and the board. To prevent components from being overheated, temperature sensitive paint is applied to the top of the component. The paint liquefies when the proper reflow temperature of the solder has been reached. An adapter or reducing nozzle is used on the heat gun to direct heat to a specific component without disturbing adjacent components.

CAUTION

The fine, closely-spaced traces and pads that are used in SMT are fragile and easily separated from the surface mount assembly. Care must be taken when removing a component. Make sure the solder has reflowed on all the pins before removing the component. Wait until the temperature sensitive paint liquefies and changes color, then remove the component. Attempting component removal before the solder has melted can result in separation of the pad and possibly the trace.

Removal of Integrated Circuits

Use the following procedure to remove surface mounted ICs:

1. Apply a drop of temperature sensitive paint to the top of the IC. The paint dries quickly.

2. Use the heat gun with adapter or nozzle to heat the component, taking care to aim the hot air only at the leads. The paint turns to a clear liquid when the component reaches 400 ^{o}F, the reflow temperature of the solder.

3. When the solder has reflowed, carefully lift the component off the board. Attempting to move the component before the solder has melted can damage the circuit assembly.

Removal of Chip Components and Transistors

Chip components and transistors can be removed as outlined above. Since it is easier to see the solder reflow on two- and three- terminal components, paint application is not necessary. However, in some cases it is easier to use a low wattage soldering iron with slot tip adapters instead of the heat gun. For component removal with the iron, apply the slotted tip so that the tinned surface touches the solder fillet between the component lead and the assembly pads. Do not press on the assembly while heating. Contact the assembly gently and let the heat of the tip do the work. As soon as the solder melts completely, remove the component from the assembly with a slight twisting action of the iron tip. The component adheres to the wetted surface of the tip through capillary action.

Installing Integrated Circuits

Use the following procedure to install surface mounted ICs:

1. Once the defective component has been removed, prepare the assembly for the replacement component.

   a. If sufficient solder remains on the pads, brush them with liquid flux, and continue to the next step.

   b. If sufficient solder does not remain on the pads, add solder to the pads with small diameter solder, using a low wattage or temperature-controlled soldering iron. If the amount of solder on the pads is not even, gently brush a wide tip soldering iron across the pads. This technique removes solder from pads that have an excess and adds solder to pads that have less. To prevent damage to the board, perform all work quickly using a light iron pressure and no rubbing.

2. Apply a drop of temperature sensitive paint to the top of the IC.

3. Place and align the component on the pads. Perfect alignment is not necessary. Once the leads are partially placed on the correct pads, the molten solder pulls then onto the center of the pad.

4. Use the gun to heat the component, taking care to aim the hot air only at the leads. The paint becomes liquid when the component reaches the reflow temperature of the solder.

5. Once the component has reached the reflow temperature, remove the heat. If the component is not aligned perfectly on the pads, tap the board very gently while the solder is still molten. This procedure allows the surface tension of the solder to pull the component leads on to the pad centers. Allow the assembly to cool. Clean and inspect the solder joints as outlined in the following paragraphs.

Cleaning

The flux residue must be washed off immediately after repair. The longer the flux remains, the harder it is to clean. Flux residue also makes inspection and future repairs very difficult and can cause shorts. An aerosol freon spray flux remover/cleaner is sufficient to clean the reworked area.

Inspection of Rework

SMT miniaturization allows for closely spaced solder joints that must be carefully inspected for defects. A lighted magnifying glass is required to inspect the working area adequately.

A good solder joint exhibits the following qualities:

- Absence of excess solder. The shape of the lead is clearly outlined in the joint.
- The joint is completely covered with solder.
- Filled areas have a concave contour.
- Edges are feathered.

Inspect each component for the following characteristics:

- On a chip component the solder should wick three quarters across the face and two thirds up the side of the contact surface. See Figure 4-19.

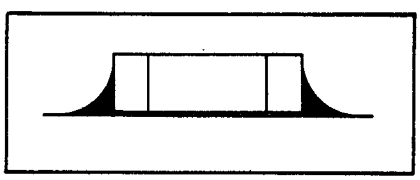


Figure 4-19. Chip Soldering

- On a PLCC device the solder should fill both outside rounded areas of the "J" lead with a smooth, concave contour. See Figure 4-20.

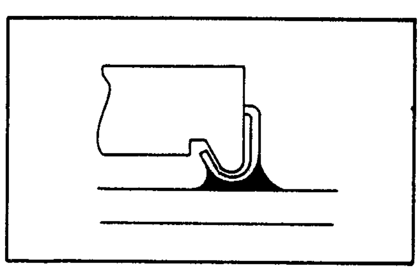


Figure 4-20. PLCC Soldering

- On an SOIC or flatpack device the solder joint should extend the full length of the portion of the lead that makes contact with the pad. The lead outline should be clearly visible under the solder. See Figure 4-21.

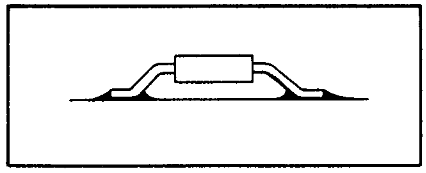


Figure 4-21. SOIC Soldering

Inspect each solder joint for the following defects:

- Solder balls. The solder should reflow into a single mass on the pad. However, some smaller solder spheres may not combine with the main sphere of solder. Remove solder balls by cleaning the solder connections with a small brush.

- Solder bridges. Solder may bridge two adjacent pads if applied in excess. A solder bridge may be removed with a soldering iron.

- Missing solder. If the solder joints are weak or incomplete, the component must be removed and resoldered correctly.

- Cold joints. Cold solder joints have a frosted, gritty appearance. They are caused by insufficient heat or by moving the component before the solder has cooled. A component with cold solder joints must be removed and resoldered correctly.

- Lifted pads. Pads that separate from the board cannot be repaired, and the board must be scrapped. The best way to prevent board damage is to avoid excessive heat and allow the solder to reflow completely before removing components.

- Flux residues. Any flux residues remaining on the board after cleaning must be removed with further cleaning.

TOOLS AND SUPPLIES

The tools and supplies mentioned in Table 4-6 have been carefully selected for efficient and reliable rework. Substitutions of the heat gun must be made with care. The correct solder and proper application of heat are critical for reliable repair of SMT assemblies.

Table 4-6. SMT Rework Tools and Supplies

DESCRIPTION	MODEL NUMBER
Hot air rework station, solder nozzle adapters	Leister Labor "S", Model 7A #31D6, for 14- and 16-pin SOICs #31D5, for 28-, 44-, and 68-pin PLCCs
- or -	
Heat gun with reducing baffle 750^{o}F nozzle temperature	Ungar heat gun, Model 6966C Reducing baffle, Model 6958
Soldering iron, 15W	Soldermaster Model SMD10
Soldering iron tips for chip components and transistors	Soldermaster number S102 and S203
Solder, Multicore	Xersin 2055 Fluke P/N 715565
Temperature indicating paint 400^{o}F/204^{o}C	Omega Omegalaq, 2 oz bottle
T.M.C. Cleaner (rosin flux remover)	Sprayon Number 2009
Flux	Xersin 2005 Fluke P/N 715573

Repair Information

GENERAL

Many of the assemblies in the 9100A/9105A use Surface Mount Technology (SMT). The repair techniques for these printed circuit assemblies (PCAs) are different than those used for the older-style printed circuit boards that use throughhole mounted components. For more information on SMT, see the Surface Mount Repair information in this manual.

Some of the assemblies in the 9100A/9105A are Original Equipment Manufacturer (OEM) modules; each of these modules is treated as a single part. This Service Manual does not contain component level parts lists for these modules, since they are not manufactured or supported to the component level by Fluke.

MAIN PCA

The Main PCA almost exclusively uses surface mount technology. Many of the other assemblies in the 9100A/9105A mainframe connect directly to the Main PCA. These assemblies include the Power Supply, Floppy Disk Drive(s), RAM Modules, Display PCA, Probe I/O PCA, Multi-Function Interface PCA, and Video Controller PCA. The fan and serial Ports 1 and 2 plug into the Main PCA. Also, an Interface Pod and the Programmer's Keyboard plug into external connectors on the Main PCA.

The Main PCA includes an EEPROM, U11, that contains characterizing data for the instrument and stores certain parameters. If this EEPROM is to be replaced, the replacement must be ordered as a programmed part. Certain characteristics must be programmed into it after the replacement EEPROM is installed; this can be done by a Fluke Technical Center, or with a utility program that is included with the 9100A Service Kit. Also, certain other hardware changes require that the EEPROM be reprogrammed.

CAUTION

When reinstalling the Main PCA (or rear panel) take care to connect the cables from the RS-232 ports to the correct connectors on the pca. Improper connections can cause a short to earth ground. Proper connections are: RS-232 Port 1 to J3 on the Main PCA and RS-232 Port 2 to J2 on the Main PCA.

DISPLAY AND KEYPAD

The Display PCA uses surface mount technology. The Keypad PCA connects to the Display PCA.

Display and Keypad PCAs have several built in self tests and diagnostics; these are described under "Display Self Test" earlier in this section. The self tests allow checking and some troubleshooting of the display and operator keypad functions.

The Display PCA contains a vacuum fluorescent display tube. This display tube has a glass envelope and is susceptible to breakage. Caution should be taken to prevent sharp blows or direct pressure to the glass envelope or to leads of the vacuum fluorescent tube.

The display tube is driven with high voltage (approximately 70 volt pulses at the grids and anodes). Attempting to measure the outputs of the driving circuitry or the inputs to the display tube with a logic probe or other low voltage measuring device can cause equipment damage.

The Keypad PCA's only active components are the key switches and a single light-emitting diode.

PROBE I/O

The Probe I/O PCA uses surface mount technology extensively. It includes several custom LSI components. The I/O Connector PCA and Trigger Output connector plug into this assembly. The Clock Module, Single-Point Probe, and the External Switch plug into external connectors. The Probe fuse holder is also mounted on the Probe I/O PCA.

The Probe I/O PCA contains the logic probe signal input circuitry. Changes to portions of this circuitry cause calibration changes. Probe compensation should be performed after any changes in the probe input circuit, including replacing or changing the Single-Point Probe. Any changes in the probe threshold or DAC (digital to analog) circuits require reprogramming the probe offset level in the EEPROM (U11 on the Main PCA); this can be done by a Fluke Technical Center, or with a utility program that is included with the 9100A Service Kit.

I/O CONNECTOR

There is no special repair information for the I/O Connector PCA.

SINGLE-POINT PROBE

The Single-Point Probe primarily uses surface mount technology. Repair or replacement of the probe, or use of another probe, requires that the probe compensation adjustment be performed.

CLOCK MODULE

The Clock Module is partially based on surface mount technology.

When reinstalling the Clock Module case or flying lead wires, take care to install them correctly. The case should be installed with the signal name "COMMON" next to the black lead wire; the flying lead wires should be installed with the black lead wire on the same side of the assembly as the fuse holder. Remember to install the plug in the case hole (opposite the fuse holder).

The operating software can be loaded on a formatted hard disk even if the 9100A is not able to boot up from the hard disk. Use the following procedure:

1. Put the System Disk 1 floppy disk in the floppy disk drive.

2. Hold down the "SOFT KEYS", "F2", and "F4", and turn on the 9100A power (or press the Restart button on the right side panel if the power is already on).

3. When the display message indicates that it is booting from the floppy disk, release the three keys.

4. Change to System Disk 2 when instructed by the display.

5. When the 9100A displays the READY message, the software can be loaded on the hard disk by using the COPY function in the Main Menu to copy the System and User disks (and Programmer's software, if applicable) from the floppy disks to the hard disk. See Section 3 of the Technical User's manual for more information on copying disks.

MULTI-FUNCTION INTERFACE

The Multi-Function Interface PCA is standard only in the 9100A. This assembly plugs into J6 on the Main PCA (the 96-pin connector on the right). The Hard Disk Controller is connected through a cable to a connector on the Multi-Function Interface; the assembly also contains the Real-Time Clock circuit. The Multi-Function Interface PCA may have several empty component spaces on the board that have been reserved for special features.

The 9105A Real-Time Clock option uses a version of the Multi-Function Interface PCA with only clock circuitry installed.

VIDEO CONTROLLER

The Video Controller PCA uses mainly surface mount technology. The Monochrome Video Interface and the Color Video Interface use the same assembly, with jumpers to select the mode. The Video Controller plugs into J5 on the Main PCA (the 64 pin connector between J4 and J6); it has an external connector that passes through the rear panel for connection to a monitor.

For the Monochrome video interface, jumper block Z1 is installed on the Video Controller PCA; jumper block Z2 is installed for the Color video interface.

MONOCHROME MONITOR

The Monochrome Monitor contains two OEM modules. The power supply is an OEM module that is replaced as a single part. The crt and Video Display Electronics PCA is an OEM set; both the crt and Video Display PCA are replaced at the same time.

I/O MODULE

The I/O Module consists of two assemblies. The I/O Main PCA uses surface mount technology, with components mounted on both sides of the board. The I/O Module Top PCA has interface connectors and a few other components.

Repair of the I/O Main PCA, which has SMT components mounted on both sides, is performed in the same way as with other SMT assemblies, except that extra care needs to be taken not to overheat the board. Too much heat applied to one side could cause nearby components on the other side to pull away from the pads or fall off the board.

Replacing the external mating connectors on the I/O Module Top PCA must be done carefully. The connectors are a high-reliability type, designed for a large number of insertion/removal cycles. Alignment of the connectors is critical to allow proper mating with the external interface modules. When replacing the connectors, align them in the same way as the mating connectors on the Clip or Flying Lead modules, below, using a full width interface module as an alignment fixture.

CLIP OR FLYING LEAD MODULES

The Clip and Flying Lead Modules interface the I/O modules to a Unit Under Test (UUT) using IC clips or flying leads. They are either half width modules, for up to 24 pins, or full width modules, for up 40 pins. The Calibration Module (used for software calibration of the I/O Module) is similar to the full width modules.

The Clip and Flying Lead modules use internal configuration switches that are read by the I/O Module to determine the type of module attached. The half-width modules use a four-bit switch, and the full-width modules use an eight-bit switch. See Table 4-9 for a list of switch settings. When servicing a clip or flying lead module, be sure that the configuration switches are set correctly.

Table 4-9. Clip and Flying Lead Module Configuration Switch Settings

4-BIT SWITCH 4321	MODULE
0000	14-Pin Clip
0001	16-Pin Clip
0010	18-Pin Clip
0011	20-Pin Clip
0100	24-Pin Clip
1101	20-Pin Flying Lead Set

0 = on (closed)
1 = off (open)

8-BIT SWITCH 8765 4321	MODULE
1110 0000	28-Pin Clip
1110 0001	40-Pin Clip
1110 0010	Calibration Module (hardwired)

The connectors and connector alignment posts that mate the Clip or Flying Lead modules to the I/O Module must be aligned precisely with the mating connectors on the I/O Module. Use the following procedure when installing the connectors:

1. Make sure the solder is removed from all the holes for the connector before attempting to install it. The connector should fit loosely in the holes.

2. Place the connector in the holes in the board, and place the connector posts though the large holes in either end. Be sure that the notches on the posts line up correctly.

3. Put on the nuts or screws loosely enough that the connector can move somewhat. Use an I/O Module as an alignment fixture; gently plug the module being repaired into an I/O Module, taking care that the connectors mate correctly. With the connectors completely seated, tighten the nuts or screws, and solder several pins on the connector (and the alignment posts, if necessary) to hold it in place. The module being repaired can be unplugged to solder the remaining pins.

TABLE OF CONTENTS

INTRODUCTION

Section 5 provides an illustrated parts list for the 9100A, 9105A, and related optional assemblies.

Components are listed alphanumerically by assembly. Both electrical and mechanical components are listed by reference designation. Each listed part is shown in an accompanying illustration.

The parts lists contain the following information:

- Reference Designator
- Description
- Fluke Stock Number
- Federal Supply Code for Manufacturers (MFRS SPLY CODE)
- Manufacturer's Part Number
- Total Quantity of Components per Assembly (TOT QTY)
- Recommended Spare Quantity (RSQ)

The number in the RSQ column represents the number of spare parts necessary to support one to five instruments for a period of 2 years. This quantity assumes that common electronic parts are available at the maintenance site. To maintain the instrument for 1 year or more at an isolated site, it is recommended that at least one of each assembly in the instrument be stocked. In the case of optional subassemblies, plug-ins, etc., that are not always part of the instrument or are deviations from the basic instrument model, the RSQ column lists the recommended spare quantity for the items in that particular assembly.

HOW TO OBTAIN PARTS

Components may be ordered directly from the manufacturer's part number, or from the John Fluke Manufacturing. Co., Inc. or an authorized representative by using the Fluke Stock Number. In the event the part ordered has been replaced by a new or improved part, the replacement will be accompanied by an explanatory note and installation instructions if necessary.

To ensure prompt and efficient handling of your order, please include the following information:

- Quantity
- Fluke Stock Number
- Description
- Reference Designation
- Printed circuit assembly (PCA) number and revision letter
- Instrument Model Number and Serial Number

Parts price information is available from the John Fluke Manufacturing Co., Inc. or its representative. Prices are also found in the Fluke Replacement Parts Catalog, which is available on request.

CAUTION

An asterisk in the "S" (static) column indicates a device or component subject to damage by static discharge.

Table 5-1 identifies the parts lists applicable to your 9100 Series model. For example, for the 9100A Digital Test System, Tables 5-2, 5-3, 5-4, 5-6, 5-7, 5-10, 5-11, 5-12, and 5-17 would be used.

Table 5-1. Model Configurations

RELATED PARTS LISTS:

Table	Assembly/Option	9105A Digital Test Station	9100A-011 Video, Color (Table 5-24)	9100A-009 Video, Monochrome (Table 5-23)	9100A-005 Programmer's Station, Color (Table 5-21)	9100A-004 Programmer's Station, Mono	9100A-003 Parallel I/O Module	9100A Digital Test System	9100A/SYS Digital Test Programming Station
5-2	Final Assembly	X						X	X
5-3	A1 Main PCA	X						X	X
5-4	A2 Display Interface PCA	X						X	X
5-5	A4 Video Controller PCA		X	X	X	X			X
5-6	A5 Probe PCA	X						X	X
5-7	A6 Clock Module PCA	X						X	X
5-8	A7 I/O Module (Main) PCA						X		X
5-9	A8 I/O Module (Top) PCA						X		X
5-10	A9 Probe I/O PCA	X						X	X
5-11	A10 Multi-Function I/F PCA							X	X
5-12	A11 I/O Connector PCA	X						X	X
5-13	A12 Half-Width Clip Module								X
5-14	A13 Full-Width Clip Module								X
5-15	A14 Calibration Module						X		X
5-16	A15 Flying Lead Module						X		X
5-17	A16 512K RAM Module*	X						X	X
5-18	A19 Monochrome Monitor			X		X			X
5-19	-003 Parallel I/O Module								X
5-20	-004 Programmer's Station, Mono								X
5-22	-008 Real-Time Clock PCA (optional)	X							
5-25	-013 Programmer's Keyboard				X	X			X

* -007 512K Memory Expansion is included in Table 5-17.

Table 5-2. 9100 Series Final Assembly
(See Figure 5-1.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
A	1	*	MAIN PCA	768754	89536	768754	1		
A	2	*	DISPLAY INTERFACE PCA	768689	89536	768689	1		
A	3		KEYPAD ASSEMBLY	846357	89536	846357	1		
A	5	*	PROBE ASSEMBLY	773911	89536	773911	1		
A	6	*	CLOCK MODULE ASSEMBLY	768812	89536	768812	1		
A	9	*	PROBE I/O INTERFACE PCA	768796	89536	768796	1		
A	10	*	MULTI-FUNCTION INTERFACE PCA	767988	89536	767988	1		1
A	11	*	I/O CONNECTOR PCA	767996	89536	767996	1		
A	16	*	512K RAM MODULE	822858	89536	822858	4		3
A	101		PWR SUP,150W,+5V,(2)+12V,-5V	772988	89536	772988	1		
A	102	*	DISK DRIVE,FLOPPY,3.5"	829671	89536	829671	1		2
A	104	*	DISK DRIVE,HARD,3.5",FRMTD,20MBYTS	834234	89536	834234	1		1
A	105	*	WINCHESTER HARD DISK CONTROLLER	780940	89536	780940	1		1
CR	1	*	LED,RED,PCB MNT,LUM INT=0.5MCD	369777	28480	5082-4480	1	1	
E	1		TERM,FASTON,REC,18-22AWG,CRIMP,INSUL	655001	59730	RAD20377	1		
F	1		FUSE,1/4 X 1-1/4,SLOW,2A,250V	109181	71400	MDX2	1	5	
F	1		FUSE,5X20MM,SLOW,1A,250V	808055	89536	808055	1	5	
H	1		SPACER,HEX,ALUM,4-40X0.500	192872	89536	192872	1		
H	2		SCREW,MACH,PHP SEMS,STL,4-40X1/4	185918	89536	185918	2		
H	3		SCREW,MACH,PHP,STL,4-40X1/2	558825	89536	558825	4		
H	4		SCREW,MACH,PH,P,STL,6-32X0.250	152140	89536	152140	1		
H	5		NUT,WELD TAB,FLOATING,STEEL,10-32	743393	89536	743393	2		
H	6		SCREW,MACH,PH,P,STL,6-32X0.250	152140	89536	152140	5		
H	7		SCREW,MACH,PH,P,STL,10-32X0.750	114306	89536	114306	2		
H	8		SCREW,MACH,PH,P,STL,6-32X0.250	152140	89536	152140	14		
H	9		SCREW,MACH,PH,P,STL,8-32X0.375	114124	89536	114124	2		
H	10		CONN ACC,D-SUB,LATCH BLOCK,SHORT,SLOT	811653	89536	811653	12		
H	11		SCREW,MACH,FIHS,STL,4-40X3/8	129916	89536	129916	12		
H	12		CONN ACC,D-SUB,SLIDING LOCK,POST ASSY	353201	89536	353201	2		
H	13		CONN ACC,D-SUB,JACK SCREW,4-40	448092	89536	448092	4		
H	14		SCREW,MACH,PH,P,STL,6-32X0.250	152140	89536	152140	4		
H	15		RIVET,PUSH,UNIV,NYL,.16,.32	799957	89536	799957	4		
H	16		SCREW,MACH,PH,P,STL,6-32X0.375	152165	89536	152165	2		
H	17		NUT,CAP EXT LW,STL,6-32X7/64	152819	89536	152819	2		
H	18		DUST FILTER, SET	773994	89536	773994	1		
H	19		WASHER,SHLDR,NYLON,.320X.141X.065	733345	89536	733345	4		
H	20		RIVET,POP,DOME,AL,0.125X0.440	800763	89536	800763	4		
H	21		FASTENER,STUD REC,TUBLR,0.187 X 0.46	783134	89536	783134	2		
H	22		SCREW,MACH,PH,P,STL,6-32X0.250	152140	89536	152140	8		
H	23		SCREW,MACH,PH,P,STL,8-32X0.375	114124	89536	114124	4		
H	24		SCREW,MACH,SEMS,PH,P,STL,6-32X0.375	177022	89536	177022	4		
H	25		SCREW,MACH,PHS,M3 X 12	799502	89536	799502	4		
H	26		SCREW,MACH,PH,P,STL,6-32X0.500	152173	89536	152173	4		
H	27		SCREW,MACH,PH,P,STL,6-32X0.250	152140	89536	152140	2		
H	28		SCREW,MACH,PH,P,STL,6-32X0.250	152140	89536	152140	3		
H	29		SCREW, SHOULDER	775999	89536	775999	2		
H	30		CONN ACC,D-SUB,DUST CAP,37 SCKT	615138	89536	615138	4		
H	31		CONN ACC,D-SUB,DUST CAP,25 PIN	816371	89536	816371	2		
H	32		SCREW,MACH,PH,P,STL,4-40X0.250	129890	73734	19022	1		
J	1		CONN,COAX,BNC(F),PANEL	152033	95712	30355-1	1		
MP	1		BOX,MAILER,CONVOLUTED FOAM INSIDE	707851	89536	707851	2		
MP	2		DISPLAY WINDOW, SHIELD	784009	89536	784009	1		
MP	3		9100A ACCESSORIES	788554	89536	788554	1	1	
MP	5		SHIELD, CLOCK MODULE	755793	89536	755793	1		
MP	6		CASE, CLOCK MODULE	755827	89536	755827	1		
MP	7		COVER	755686	89536	755686	1		
MP	8		CASE, CLOCK MODULE	755652	89536	755652	1		
MP	10		KEYPAD CASE TOP	765008	89536	765008	1		
MP	11		KEYTOP, SET	775858	89536	775858	1		
MP	12		KEYPAD, ELASTOMERIC	764910	89536	764910	1	1	
MP	13		CORD,LINE,5-15/IEC,3-18AWG,SVT	343723	89536	343723	1		
MP	14		TORSION SPRING	784025	89536	784025	2	1	
MP	15		KEYPAD CASE BOTTOM	765016	89536	765016	1		
MP	16		SPRING DETENT	765032	89536	765032	2		
MP	17		NAMEPLATE	787275	89536	787275	1		
MP	18		FRONT PANEL, PAINTED	764894	89536	764894	1		
MP	19		LENS	783993	89536	783993	1		4
MP	20		KEYPAD OPENING SHIELD	767889	89536	767889	1		
MP	21		HINGE/DETENT HOUSING	765024	89536	765024	2		
MP	22		MAINFRAME BASE	767848	89536	767848	1		

An * in 'S' column indicates a static-sensitive part.

Table 5-2. 9100 Series Final Assembly (cont.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	------DESCRIPTION------	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
MP 24		DECAL, CHASSIS CONNECTOR	803221	89536	803221	1		
MP 25		FOOT,VINYL,NYL.PUSH RIVET,0.787X0.236	801001	89536	801001	4		
MP 26		REAR PANEL	767855	89536	767855	1		
MP 27		HLDR PART,FUSE,CAP,1/4X1-1/4	460238	61935	031.1666	1		
MP 29		EXPANSION SLOT COVER	768010	89536	768010	1		
MP 30		VIDEO SLOT COVER	768655	89536	768655	1		
MP 31		HLDR PART,FUSE,CAP,5X20MM	461020	89536	461020	1		
MP 32		CABLE TIE,MOUNT,ADHESIVE,0.19" WIDTH	565036	89536	565036	1		
MP 33		CABLE TIE,4"L,0.100"W,0.75 DIA	172080	89536	172080	1		
MP 34		SLEEV,POLYOL,SHRINK,.750-.375ID,BLACK	226365	89536	226365	4		
MP 35		MAINFRAME TOP COVER	773986	89536	773986	1		
MP 36		SHIELD, RFI	768028	89536	768028	1		5
MP 37		LOUVER	787846	89536	787846	1		6
MP 38		POWER SUPPLY SHIELD ASSEMBLY, PLATED	830398	89536	830398	1		
MP 39		CABLE TIE,MOUNT,ADHESIVE,0.19" WIDTH	565036	89536	565036	1		
MP 40		CABLE TIE,3.62"L,0.091"W,5/8 DIA	381533	06383	PLT1M	1		
MP 41		HARD DISK AND FLOPPY HOUSING	802033	89536	802033	1		7
MP 42		MOUNT,VIBRATION,GROMMET	782623	89536	782623	8		
MP 43		SPACER,NYLON,0.195X0.300	782631	89536	782631	8		
MP 44		SPACER,PWB,NYL,.125	806703	89536	806703	2		1
MP 45		NAMEPLATE, SERIAL -REAR PANEL-	472795	89536	472795	1		
MP 46		SYSTEM SOFTWARE, SLEEVED	809103	89536	809103	1		
MP 47		MFI SLOT ESD COVER	819680	89536	819680	1		10
MP 48		REC.MEDIA,DISK,3.5",DSDD,BOX.OF 10	757229	89536	757229	1		
MP 49		CARTON, 9100A	809038	89536	809038	1		
MP 50		END CAP SET, 9100A	809046	89536	809046	1		
MP 51		TRAY/DIVIDERS, 9100A	809053	89536	809053	1		
MP 52		CARTON, PADDED DISK	809129	89536	809129	1		
SW 1		SWITCH,ROTARY,LINE SEL.,DPDT,2 POS.	799551	89536	799551	1	1	
SW 2		SWITCH,ROCKER,DPST	800649	89536	800649	1	1	
TM 1		9100 SERIES GETTING STARTED MANUAL	787960	89536	787960	1		
TM 2		9100 SERIES AUTOMATED OPERATIONS MAN	809228	89536	809228	1		
TM 3		9100 SERIES TECHNICAL USER'S MANUAL	813832	89536	813832	1		
TM 4		9100 SERIES APPLICATIONS MANUAL	813840	89536	813840	1		
TM 5		SUPPLEMENTAL POD INFO FOR 9100A/9105A	822866	89536	822866	1		
W 3		CABLE, A C POWER CONNECT	749903	89536	749903	1		
W 4		CABLE ASSEMBLY, LINE SELECT	773267	89536	773267	1		
W 5		LINE FILTER ASSEMBLY	773424	89536	773424	1		
W 6		CABLE, PROBE I/O INTERFACE	773432	89536	773432	2		
W 7		CABLE,DISK DRIVE	773846	89536	773846	1		8
W 8		CABLE,DISPLAY INTERFACE	773853	89536	773853	1		
W 9		CABLE,KEYPAD INTERFACE	773861	89536	773861	1		
W 10		CABLE ASSEMBLY, D C HARNESS	773887	89536	773887	1		
W 11		CABLE ASSY, CLOCK MODULE	783969	89536	783969	1		
W 12		CABLE ASSEMBLY, RS232 M	787838	89536	787838	2		
W 13		CABLE ASSEMBLY, HARD DISK TO MFI	787895	89536	787895	1		1
W 15		CABLE, HARD DISK TO CONTROLLER	788448	89536	788448	1		1
W 16		CABLE, HARD DISK TO CONTROL DATA	788455	89536	788455	1		1
W 17		FAN ASSEMBLY	788471	89536	788471	1		
W 18		CABLE ASSEMBLY, BNC	801944	89536	801944	1		
W 19		CABLE ASSEMBLY, MICRO-CLIP	809178	89536	809178	1		
W 21		CABLE, DISK DRIVE POWER	788430	89536	788430	1		9
XF 1		HLDR PART,FUSE,BODY 1/4X1-1/4,5X20MM	460329	89536	460329	1		

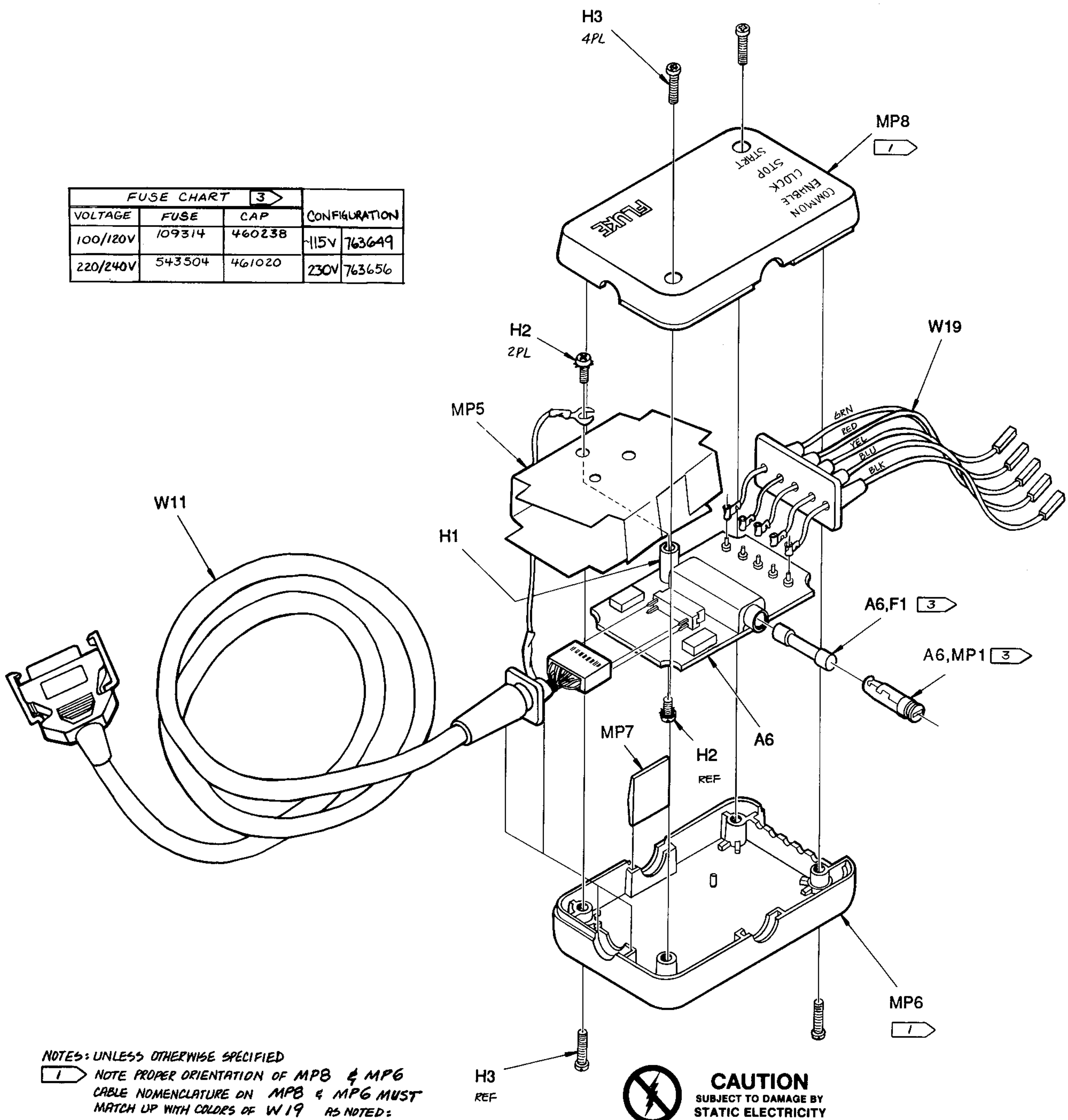
An * in 'S' column indicates a static-sensitive part.

NOTES:

1 = Not used on 9105A.
2 = For 9105A, quantity is 2.
3 = For 9105A S/Ns prior to 4352000, two 512K + two 256K (799833) were used.
4 = For 9105A, order p/n 805721.
5 = For 9105A, order p/n 805713, quantity 2.
6 = For 9105A, order p/n 787853.
7 = For 9105A, order p/n 788521.
8 = For 9105A, order p/n 788547.
9 = For 9105A, order p/n 805705.
10 = For 9105A, order p/n 802009.

A101 through A105 are Original Equipment Manufacturer (OEM) assemblies.
List of replaceable parts is not available.

FUSE CHART 3			CONFIGURATION	
VOLTAGE	FUSE	CAP		
100/120V	109314	460238	~115V	763649
220/240V	543504	461020	230V	763656



NOTES: UNLESS OTHERWISE SPECIFIED

1. NOTE PROPER ORIENTATION OF MP8 & MP6 CABLE NOMENCLATURE ON MP8 & MP6 MUST MATCH UP WITH COLORS OF W19 AS NOTED:
   - COMMON - BLACK WIRE
   - UNABLE - BLUE WIRE
   - CLOCK - YELLOW WIRE
   - STOP - RED WIRE
   - START - GREEN WIRE
2. **WARNING:** Ⓢ INDICATES USAGE OF MOS DEVICE(S) WHICH MAY BE DAMAGED BY STATIC DISCHARGE. USE SPECIAL HANDLING PER S.O.P. 19.1
3. FUSE & FUSE CAP VARY FOR DIFFERENT VOLTAGE CONFIGURATIONS: SEE FUSE CHART FOR FUSE & CAP PART NO.S.

9100A T&B
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Figure 5-1. 9100 Series Final Assembly

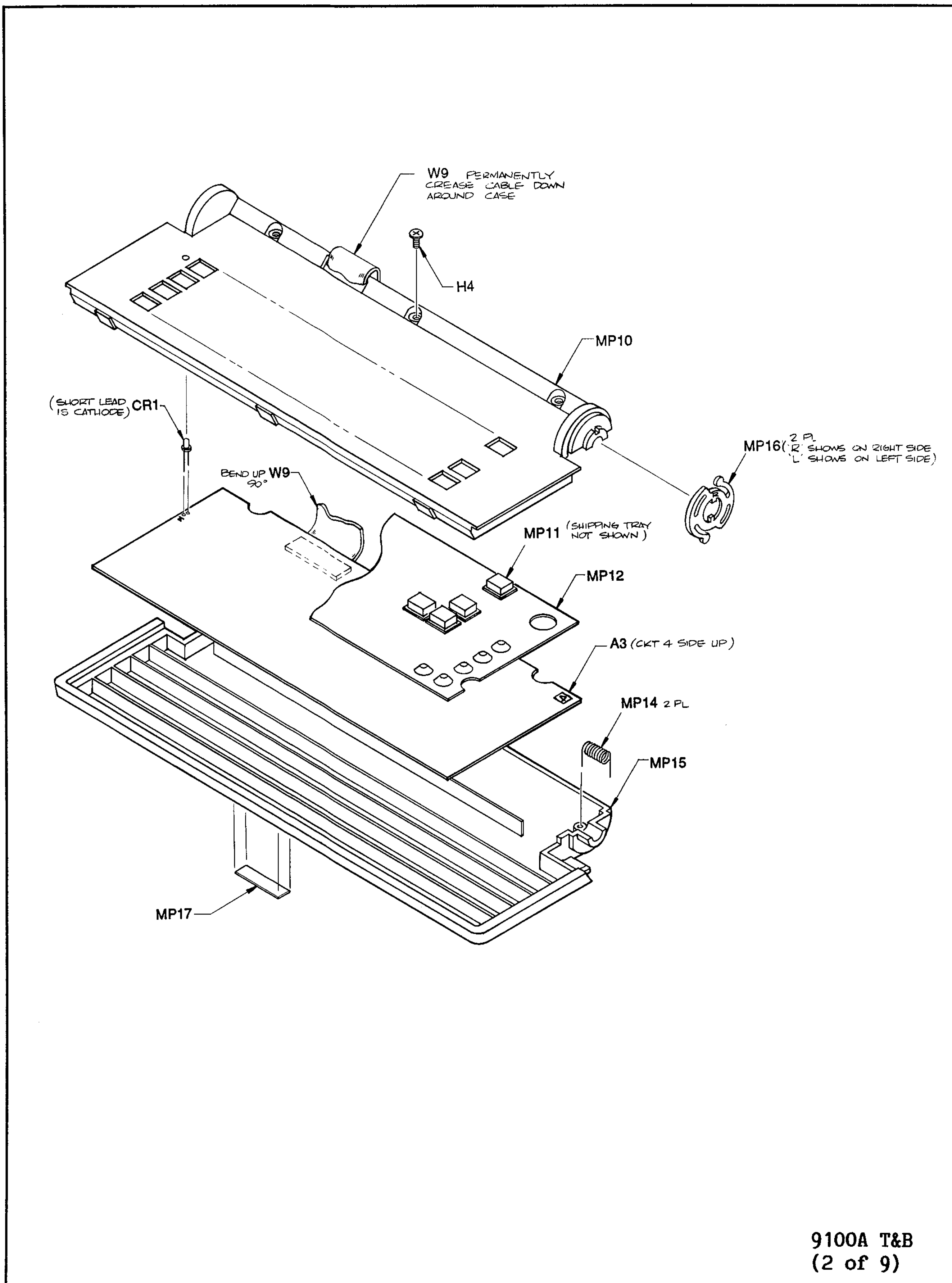


Figure 5-1. 9100 Series Final Assembly (cont.)

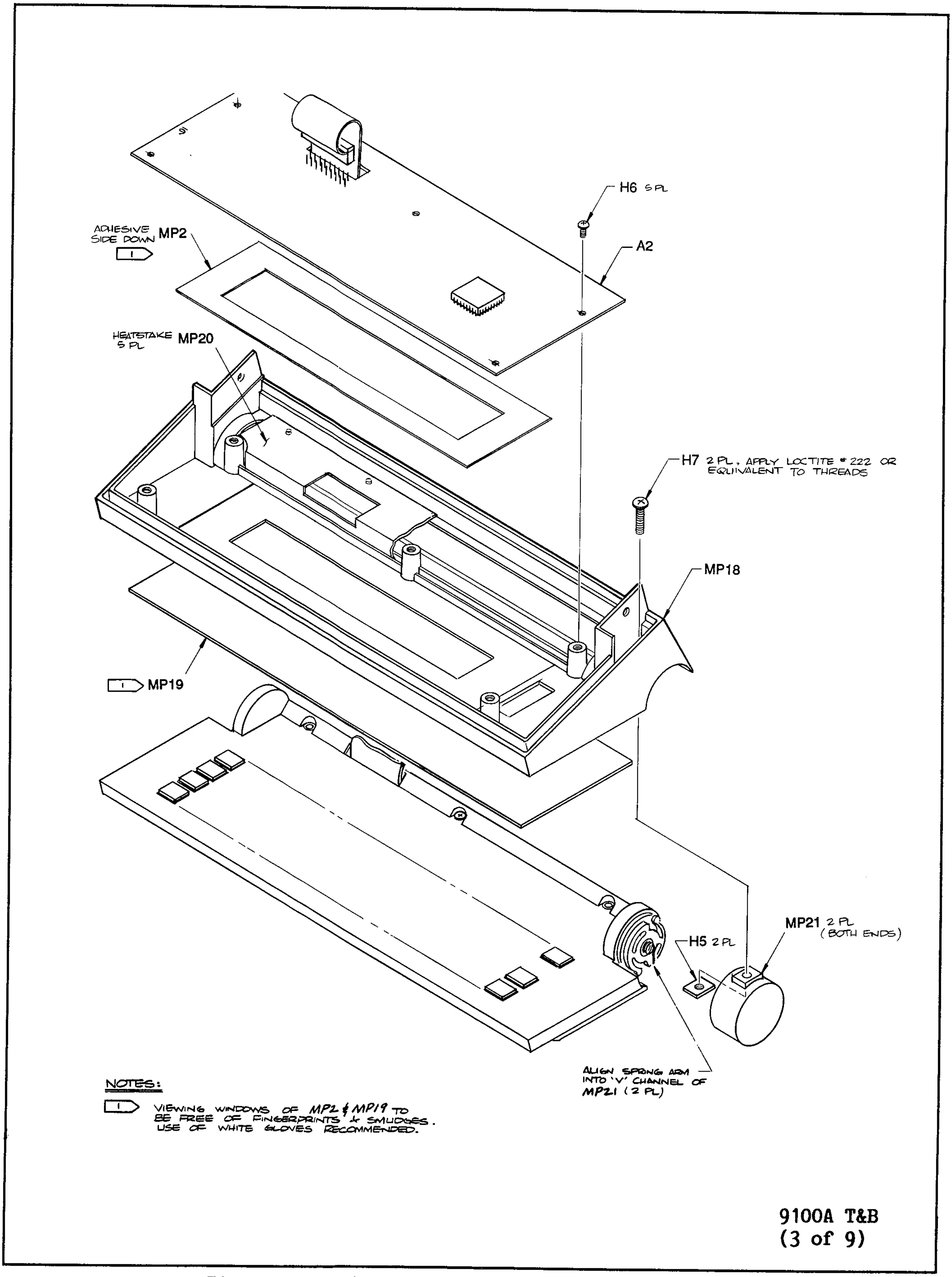
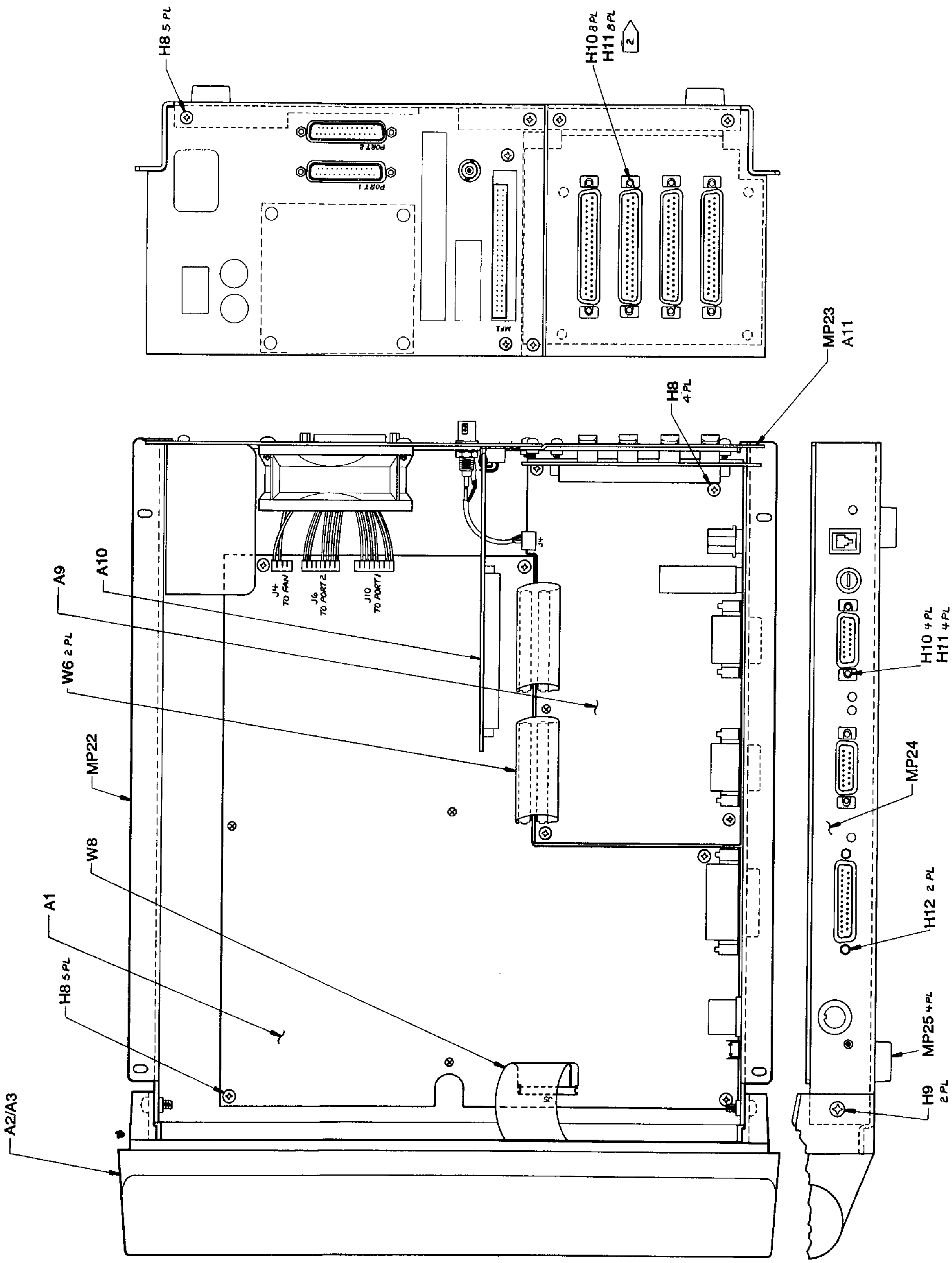


Figure 5-1. 9100 Series Final Assembly (cont.)



9100A T&B
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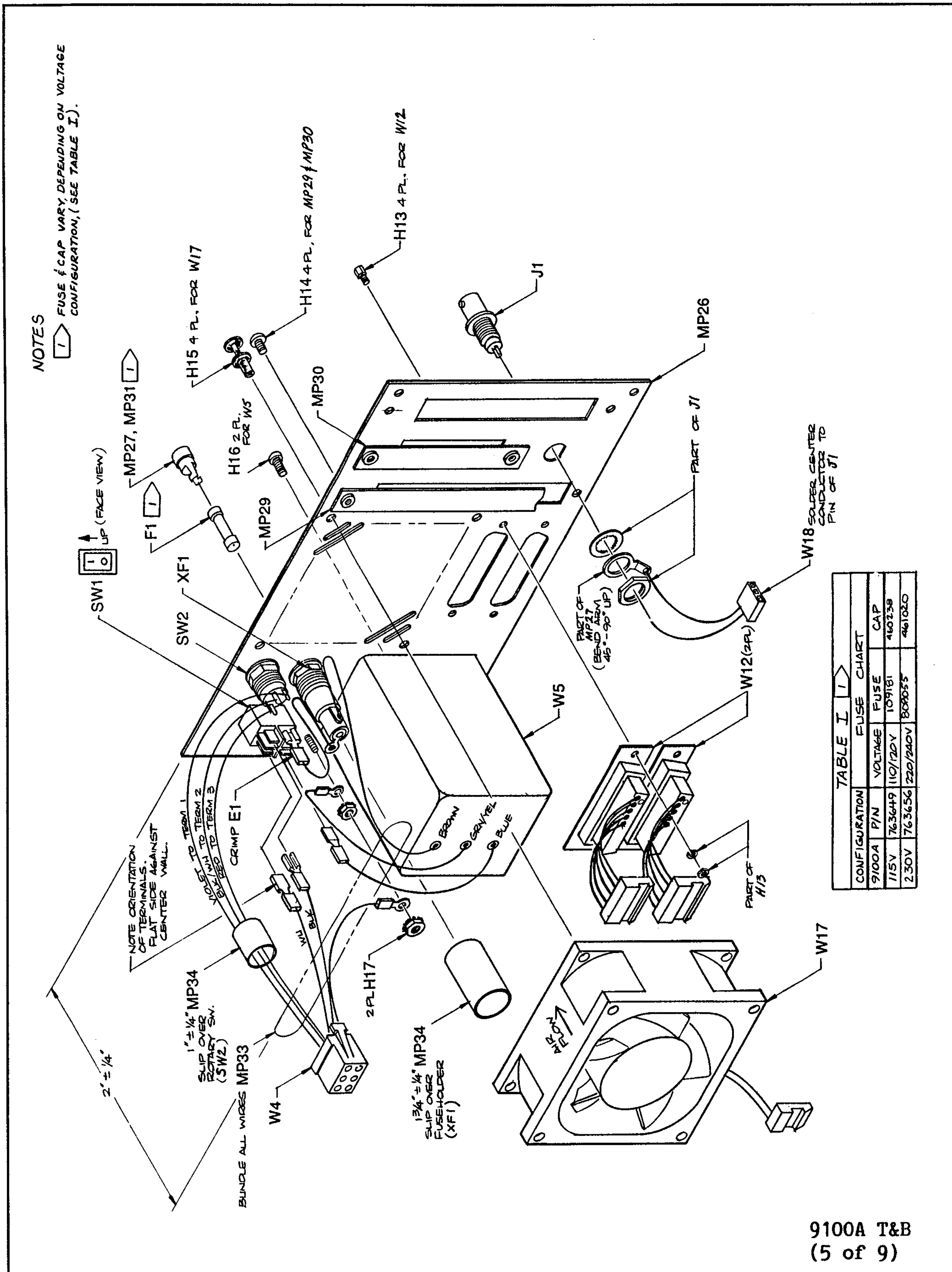
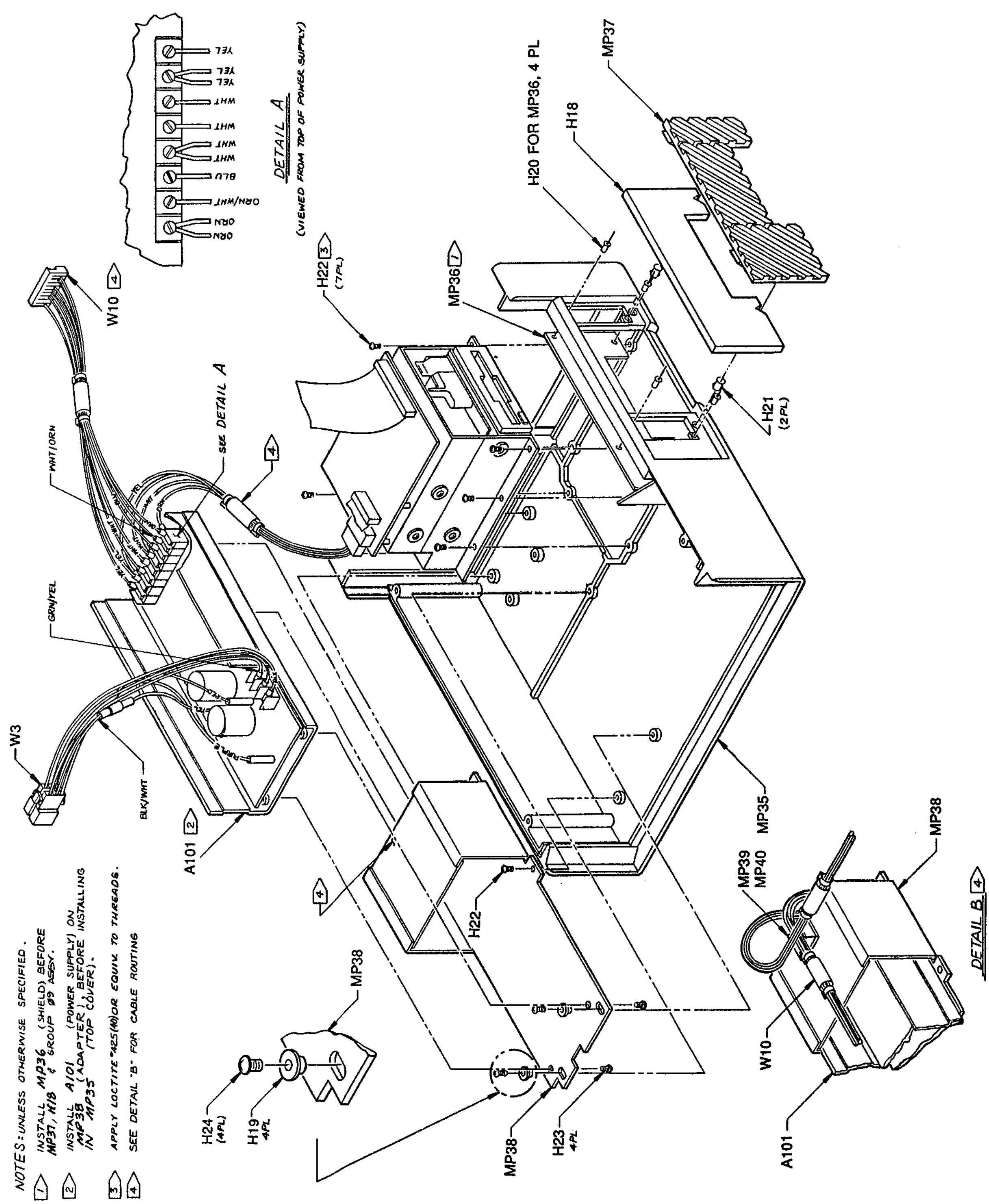
Figure 5-1. 9100 Series Final Assembly (cont.)



CONFIGURATION		FUSE	
9100A	P/N	VOLTAGE	FUSE	CAP
115V	763649	110/120V	109181	460238
230V	763656	220/240V	809055	461020

Figure 5-1. 9100 Series Final Assembly (cont.)



9100A T&B
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Figure 5-1. 9100 Series Final Assembly (cont.)

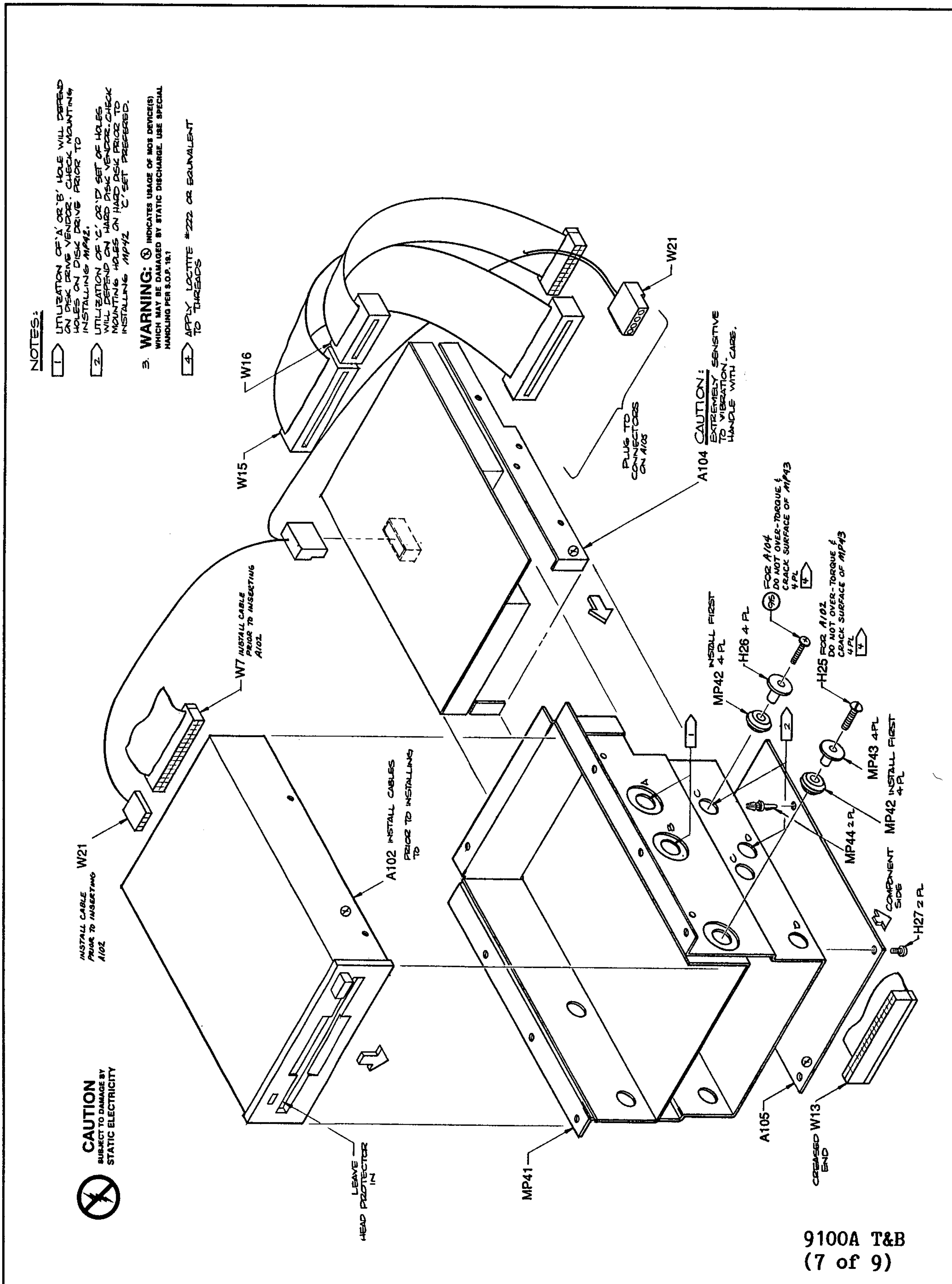


Figure 5-1. 9100 Series Final Assembly (cont.)

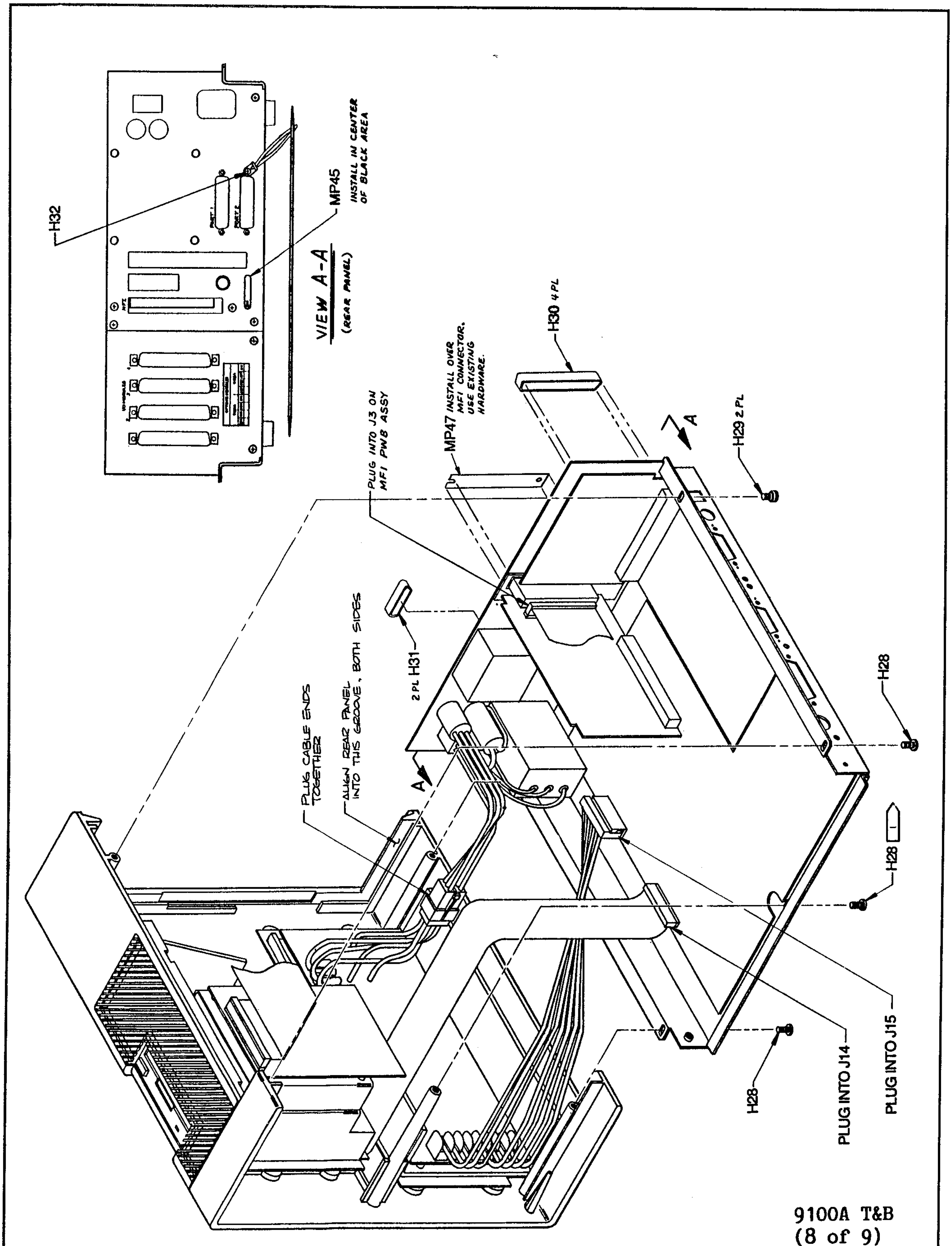
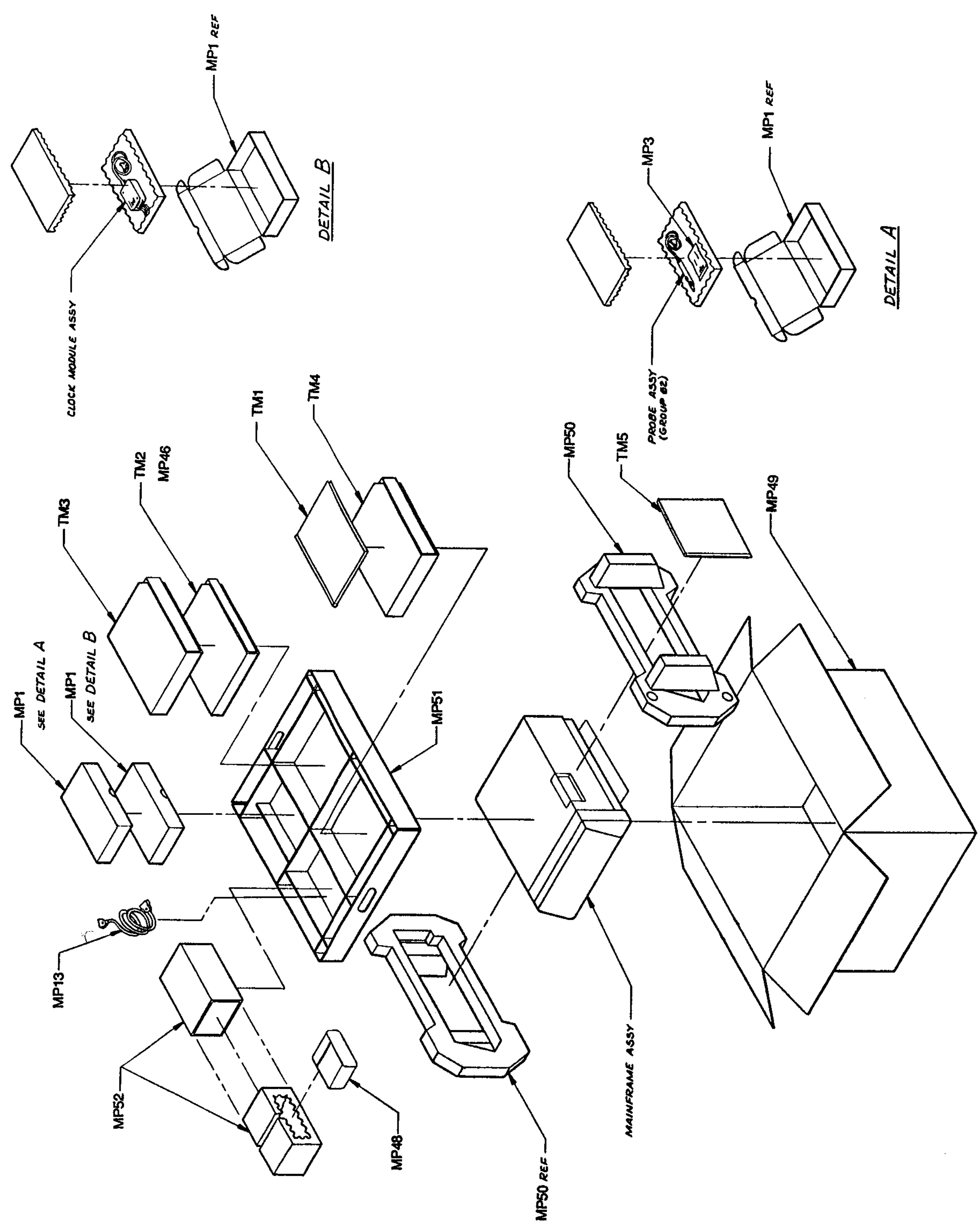


Figure 5-1. 9100 Series Final Assembly (cont.)



9100A T&B
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Figure 5-1. 9100 Series Final Assembly (cont.)

Table 5-3. A1 Main PCA
(See Figure 5-2.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C	1- 4, 6,		CAP,TA,10UF,+-20%,25V	772491	89536	772491	10		
C	23,100-103			772491					
C	5		CAP,TA,3.3UF,+-20%,25V	780486	89536	780486	1	1	
C	10, 11, 18,		CAP,CER,0.01UF,+-10%,50V,X7R,1206	747261	89536	747261	121		
C	19, 24,110-			747261					
C	113,120,121,			747261					
C	130,131,200-			747261					
C	288,300-310,			747261					
C	320,321,340-			747261					
C	343,360,361			747261					
C	12		CAP,CER,1000PF,+-10%,50V,COG,1206	747378	89536	747378	1		
C	13		CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	89536	747287	1		
C	14		CAP,CER,10PF,+-10%,50V,COG,1206	747311	89536	747311	1		
C	16, 17, 20,		CAP,CER,47PF,+-10%,50V,COG,1206	747352	89536	747352	4		
C	21			747352					
C	380		CAP,CER,0.01UF,+-20%,100V,X7R,1206	742981	89536	742981	1		
CR	1- 3, 6-		DIODE,SI,BV=200V,IO=10A,DUAL,SOT89	742973	89536	742973	6	1	
CR	8			742973					
CR	4, 5		DIODE,SI,BV=75.0V,IO=100MA,MLF	742064	89536	742064	2	2	
CR	9, 10		DIODE,SI,SCHOTTKY,30V,1.1A,SOT89	782573	89536	782573	2	1	
F	1		FUSE, 5X20MM,FAST,0.125A,250V	573733	89536	573733	1	5	
J	1		HEADER,1 ROW,0.100CTR,4 PIN	631184	89536	631184	1		
J	2, 3		HEADER,1 ROW,0.100CTR,8 PIN	520502	22526	65502-408	2		
J	4, 6		CONN,DIN41612,TYPE R,96 PIN	747808	89536	747808	2		
J	5		CONN,DIN41612,TYPE R,64 PIN	782094	89536	782094	1		
J	7, 8		HEADER,2 ROW,0.100 CTR,40 PIN	603670	89536	603670	2		
J	9		CONN,D-SUB,PWB,RT ANG,25 SCKT	782144	89536	782144	1		
J	10		CONN,CIRC,DIN,RT ANG,PWB,5 PIN @ 180	772178	89536	772178	1		
J	11		HEADER,2 ROW,0.100CTR,20 PIN	782185	89536	782185	1		
J	14		HEADER,2 ROW,0.100CTR,34 PIN	658047	89536	658047	1		
J	15		HEADER,1 ROW,0.156 CTR,10 PIN	446724	27264	09-65-1101	1		
L	1, 2		CHOKE	502138	89536	502138	2		
Q	1, 2	*	TRANSISTOR, SI, N-MOS, 1W, 4 PIN DIP	800391	89536	800391	2	1	
R	1		RES,CHIP,CERM,56K,+-5%,0.125W,1206	746701	89536	746701	1		
R	2, 3, 6,		RES,CHIP,CERM,10K,+-5%,0.125W,1206	746610	89536	746610	42		
R	7, 11- 15,			746610					
R	27- 29, 31-			746610					
R	35, 40, 43,			746610					
R	45- 48, 56-			746610					
R	63, 67, 70,			746610					
R	75, 76, 80,			746610					
R	83- 85, 87,			746610					
R	89, 90			746610					
R	4,100-111,		RES,CHIP,CERM,10,+-5%,0.125W,1206	746214	89536	746214	14		
R	116			746214					
R	5, 8- 10,		RES,CHIP,CERM,4.7K,+-5%,0.125W,1206	740522	89536	740522	12		
R	21, 22, 30,			740522					
R	65, 69, 72,			740522					
R	82, 86			740522					
R	16, 17, 51-		RES,CHIP,CERM,1.2K,+-5%,0.125W,1206	746412	89536	746412	10		
R	55, 71, 78,			746412					
R	88			746412					
R	18, 19, 36,		RES,CHIP,CERM,39K,+-5%,0.125W,1206	746677	89536	746677	5		
R	37, 74			746677					
R	20, 38, 77		RES,CHIP,CERM,3K,+-5%,0.125W,1206	746511	89536	746511	3		
R	23, 24		RES,CHIP,CERM,390,+-5%,0.125W,1206	740498	89536	740498	2		
R	25, 26		RES,CHIP,CERM,220,+-5%,0.125W,1206	746347	89536	746347	2		
R	39, 44, 79		RES,CHIP,CERM,750,+-5%,0.125W,1206	746404	89536	746404	3		
R	41, 64, 66,		RES,CHIP,CERM,33,+-5%,0.125W,1206	746248	89536	746248	9		
R	68, 91,112-			746248					
R	115			746248					
R	42, 73		RES,CHIP,CERM,100K,+-5%,0.125W,1206	740548	89536	740548	2		
R	49, 50		RES,CHIP,CERM,510K,+-5%,0.125W,1206	746800	89536	746800	2		
R	81		RES,CHIP,CERM,2.2K,+-5%,0.125W,1206	746479	89536	746479	1		
S	1		SWITCH,PUSHBUTTON,SPST,MOMENTARY	782433	89536	782433	1		
T	1		TRANSFORMER,CONVERTER	775932	89536	775932	1		
TP	1- 11		TERM,UNINSUL,WIRE FORM,TEST POINT	781237	89536	781237	11		
U	1, 4	*	IC,BIPOLAR,DUAL RS-232 RECEIVER,SOIC	742395	89536	742395	2	1	
U	2, 3	*	IC,BIPOLAR,DUAL RS-232 DRIVER,SOIC	742403	89536	742403	2	1	
U	5, 6	*	ISOLATOR,HI-SPEED DUAL	742841	89536	742841	2	1	

An * in 'S' column indicates a static-sensitive part.

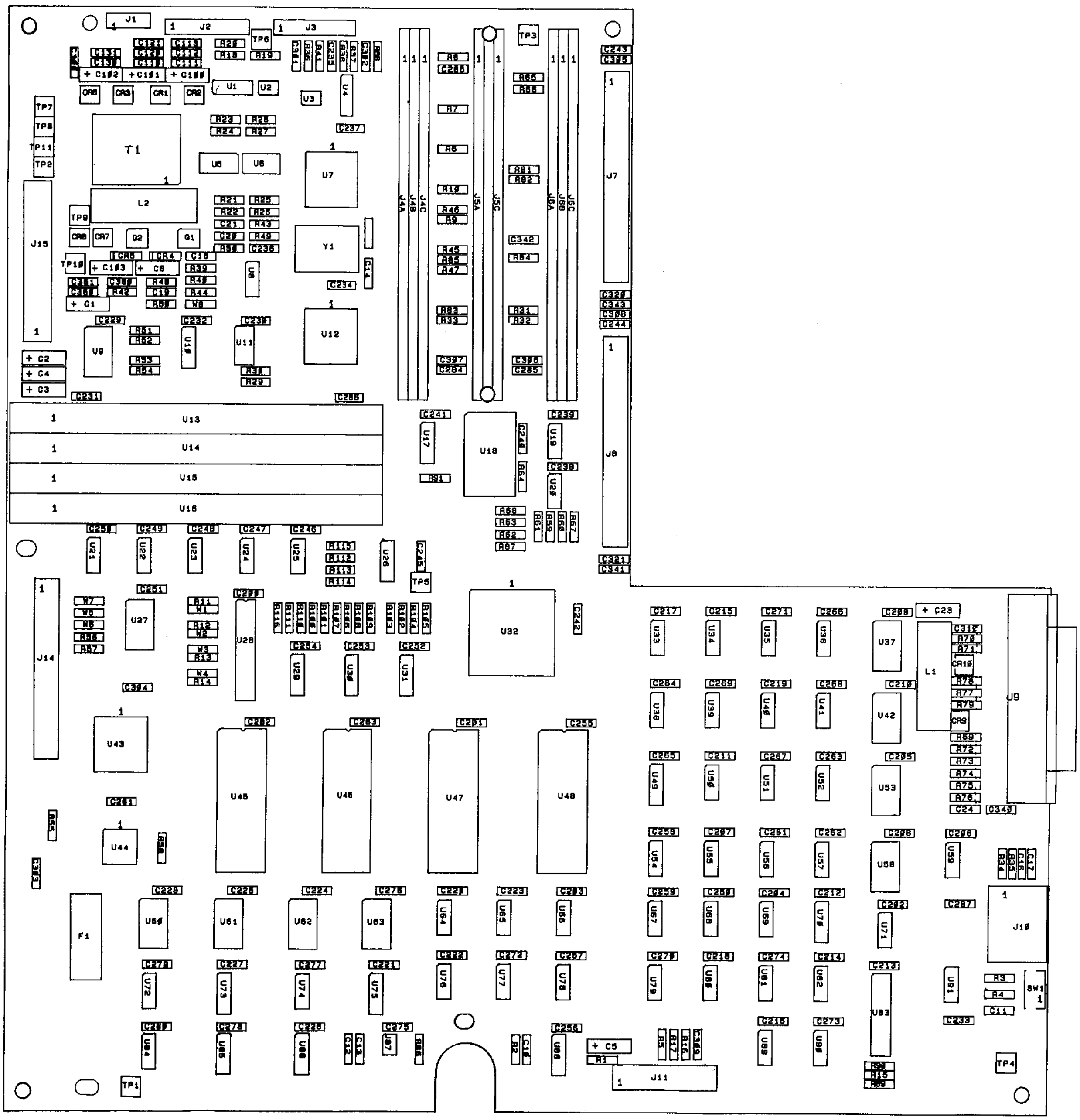
Table 5-3. A1 Main PCA (cont.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	--DESCRIPTION--	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
U 8, 35	*	IC,LSTTL,HEX INVERTER,SOIC	741017	89536	741017	2	1	
U 9	*	IC,CMOS,OCTL LINE DRVR,SOIC	742593	89536	742593	1	1	
U 10	*	IC,LSTTL,8BIT P/S-IN,S-OUT SHFT,SOIC	741983	89536	741983	1	1	
U 11	*	IC,NMOS,EEPROM 2444	834416	89536	834416	1	1	
U 13- 16	*	ASSEMBLY, RAM MODULE	809079	89536	809079	4		1
U 17	*	IC,ALSTTL,3-8 LINE DCDR W/ENABLE,SOIC	741686	89536	741686	1	1	
U 18		OSCILLATOR,32MHZ,TTL CLOCK	742338	89536	742338	1		
U 19	*	IC,FTTL,DUAL D F/F,+EDG TRG,SOIC	742163	89536	742163	1	1	
U 20	*	IC,ASTTL,QUAD 2 INPUT NAND GATE,SOIC	782250	89536	782250	1	1	
U 21, 57	*	IC,ALSTTL,QUAD 2 INPUT AND GATE,SOIC	741827	89536	741827	2	1	
U 22, 41, 82	*	IC,LSTTL,QUAD 2 INPUT OR GATE,SOIC	740878	89536	740878	3	1	
U 23, 24	*	IC,FTTL,9 BIT PARITY GEN/CHECKER,SOIC	742478	89536	742478	2	1	
U 25, 91	*	IC,ALSTTL,QUAD 2 INPUT NAND GATE,SOIC	782268	89536	782268	2	1	
U 26	*	IC,LSTTL,8-BIT BINARY CNTR W/REG,SOIC	782243	89536	782243	1	1	
U 27	*	IC,LSTTL,OCTAL BUFFER INVERTED,SOIC	742627	89536	742627	1	1	
U 28	*	IC, 16L8 LOGIC ARRAY	818203	89536	818203	1	1	
U 29- 31	*	IC,ASTTL,QUAD 2-INPUT MUX,SOIC	811984	89536	811984	3	1	
U 32	*	IC,NMOS,16 BIT MICROPROCESSOR,PLCC	742429	89536	742429	1	1	
U 33	*	IC,LSTTL,QUAD BUS,SOIC	740977	89536	740977	1	1	
U 34, 54	*	IC,LSTTL,DUAL 4 INPUT NAND GATE,SOIC	742528	89536	742528	2	1	
U 36, 67, 74	*	IC,ALSTTL,QUAD 2 INPUT NOR GATE,SOIC	782284	89536	782284	3	1	
U 37, 61- 63	*	IC,LSTTL,OCTAL D F/F,+EDG TRG,SOIC	741975	89536	741975	4	1	
U 38, 89	*	IC,ALSTTL,HEX INVERTERS,SOIC	782300	89536	782300	2	1	
U 39	*	IC,ALSTTL,QUAD 2 INPUT OR GATE,SOIC	742460	89536	742460	1	1	
U 40, 50, 81	*	IC,LSTTL,8BIT S-IN,P-OUT R-SHFT,SOIC	742106	89536	742106	3	1	
U 42, 58	*	IC,LSTTL,OCTL LINE DRVR,SOIC	742122	89536	742122	2	1	
U 43	*	IC,NMOS,FLOPPY DISK FORMTR CNTLR,PLCC	782870	89536	782870	1	1	
U 44	*	IC,NMOS,FLOPPY DISK INT CKT,PLCC	782888	89536	782888	1	1	
U 46	*	PROGRAMMED 27256 V3.0	828897	89536	828897	1	1	
U 47	*	PROGRAMMED 27256 V3.0	828905	89536	828905	1	1	
U 49, 75	*	IC,LSTTL,8 TO 3 LINE ENCODER,SOIC	782326	89536	782326	2	1	
U 51, 64	*	IC,LSTTL,QUAD 2 INPUT NAND GATE,SOIC	741033	89536	741033	2	1	
U 52	*	IC,LSTTL,TRIPLE 3-INPUT AND GATE,SOIC	741264	89536	741264	1	1	
U 53, 60	*	IC,LSTTL,OCTAL D F/F,+EDG TRG,SOIC	740928	89536	740928	2	1	
U 55, 90	*	IC,ALSTTL,8 INPUT NAND GATE,SOIC	782334	89536	782334	2	1	
U 56, 65, 78	*	IC,LSTTL,QUAD 2 INPUT NOR GATE,SOIC	741025	89536	741025	3	1	
U 59	*	IC,COMPARATOR,QUAD,14 PIN,SOIC	741561	89536	741561	1	1	
U 66	*	IC,LSTTL,TRIPLE 3 INPUT NOR GATE,SOIC	740993	89536	740993	1	1	
U 68	*	IC,ALSTTL,DUAL 4 INPUT NAND GATE,SOIC	741645	89536	741645	1	1	
U 69	*	IC,ALSTTL,TRIPLE 3INPUT NOR GATE,SOIC	782318	89536	782318	1	1	
U 70	*	IC,LSTTL,2-4 LINE DEMUX,SOIC	740951	89536	740951	1	1	
U 71	*	IC,CMOS,HEX INVERTER W/SCHT TRIG,SOIC	780965	89536	780965	1	1	
U 72	*	IC,TTL,HEX BUFFER W/OPEN COLL,SOIC	742387	89536	742387	1	1	
U 73	*	IC,LSTTL,DUAL JK F/F,-EDG TRIG,SOIC	741256	89536	741256	1	1	
U 76	*	IC,LSTTL,QUAD 2IN O/C NAND GATE,SOIC	782292	89536	782292	1	1	
U 77, 80	*	IC,LSTTL,DUAL D F/F,+EDG TRG,SOIC	740985	89536	740985	2	1	
U 79	*	IC,ALSTTL,DUAL D F/F,+EDG TRG,SOIC	742452	89536	742452	1	1	
U 83		SWITCH,MODULE,SPST,DIP,8 POS	414490	00779	435166-5	1		
U 84	*	IC,LSTTL,QUAD 2 INPUT AND GATE,SOIC	740860	89536	740860	1	1	
U 85	*	IC,LSTTL,DUAL J-F F/F,+EDG TRIG,SOIC	742502	89536	742502	1	1	
U 86	*	IC,LSTTL,DELAY ELEMENTS,SOIC	773077	89536	773077	1	1	
U 87	*	IC,VOLT SUPERVISOR,10V SENSE,SOIC	780502	89536	780502	1	1	
U 88	*	IC,LSTTL, MONOSTAB MULTIVB W/CLR,SOIC	742494	89536	742494	1	1	
XF 1		HOLDER,FUSE,5X20MM,PCB	772475	89536	772475	2		
XU 13- 16		CONN,PWB EDGE,REC,0.100CTR,30 POS	806828	89536	806828	4	1	
XU 18		SPACER,DIP SOCKET,14 PIN,PLASTIC	441865	32559	814-060	1		
XU 28		SOCKET,IC,20 PIN	454421	09922	DILB20P-108	1		
XU 45- 48		SOCKET,IC,28 PIN	448217	91506	328-AG39D	4		
Y 1		CRYSTAL,3.6864MHZ,+/-50PPM,SURF.MNT.	800193	89536	800193	1	1	

An * in 'S' column indicates a static-sensitive part.

NOTES:

1 = See A16 on the Final Assembly for quantities and part numbers.



CAUTION
SUBJECT TO DAMAGE BY
STATIC ELECTRICITY

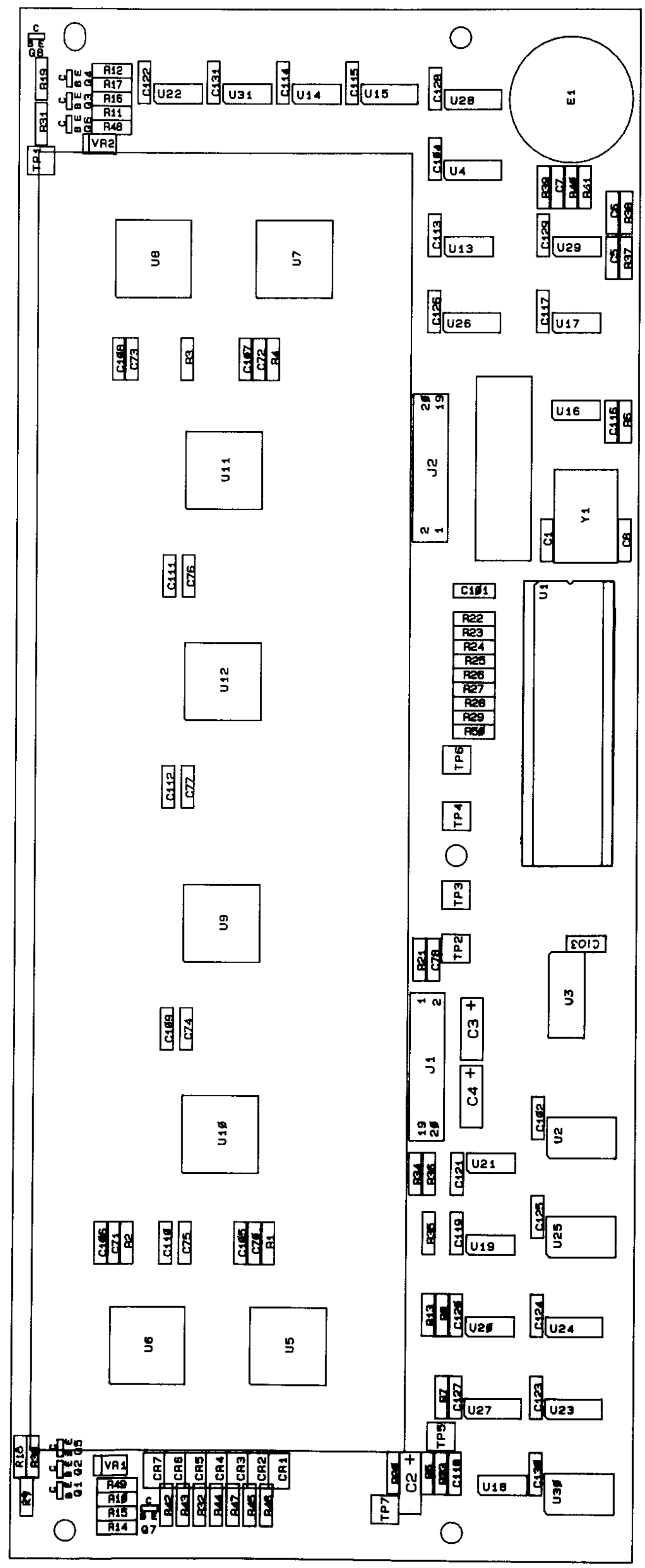
9100A-1601

Figure 5-2. A1 Main PCA

Table 5-4. A2 Display Interface PCA
(See Figure 5-3.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	----DESCRIPTION----	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C 1, 8		CAP,CER,5.6PF,+-10%,50V,COG,1206	782409	89536	782409	2		
C 2		CAP,TA,1.5UF,+-20%,50V	780478	89536	780478	1	1	
C 3, 4		CAP,TA,10UF,+-20%,25V	772491	89536	772491	2		
C 5, 70- 78,		CAP,CER,0.01UF,+-20%,100V,X7R,1206	742981	89536	742981	41		
C 101-131			742981					
C 6, 7		CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	89536	747287	2		
CR 1- 7	*	LED,RED,RECTANGLE,PCB MOUNT	504761	14936	MV57124	7	2	
E 1		AF TRANSD,PIEZO,24 MM	602490	51406	EFB-RD24C01	1		
J 1, 2		HEADER,2 ROW,0.100CTR,20 PIN	782185	89536	782185	2		
MP 1		DISPLAY ALIGNMENT FIXTURE	788570	89536	788570	1		
Q 1- 4		TRANSISTOR,SI,PNP,SMALL SIGNAL,SOT23	742023	89536	742023	4	1	
Q 5- 8		TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT23	742031	89536	742031	4	1	
R 1- 4, 6-		RES,CHIP,CERM,1.1K,+-5%,0.125W,1206	746008	89536	746008	16		
R 13, 15, 16,			746008					
R 48, 49			746008					
R 5		RES,CHIP,CERM,100K,+-5%,0.125W,1206	740548	89536	740548	1		
R 14, 17		RES,CHIP,CERM,6.8K,+-5%,0.125W,1206	746024	89536	746024	2		
R 18, 19		RES,CHIP,CERM,620,+-5%,0.125W,1206	745984	89536	745984	2		
R 20		RES,CHIP,CERM,330,+-5%,0.125W,1206	746370	89536	746370	1		
R 21		RES,CHIP,CERM,470,+-5%,0.125W,1206	740506	89536	740506	1		
R 22- 29		RES,CHIP,CERM,10K,+-5%,0.125W,1206	746610	89536	746610	8		
R 30, 31		RES,CHIP,CERM,6.2K,+-5%,0.125W,1206	746016	89536	746016	2		
R 32, 42- 47		RES,CHIP,CERM,180,+-5%,0.125W,1206	746321	89536	746321	7		
R 33, 34, 41,		RES,CHIP,CERM,4.7K,+-5%,0.125W,1206	740522	89536	740522	4		
R 50			740522					
R 35, 36		RES,CHIP,CERM,100,+-5%,0.125W,1206	746297	89536	746297	2		
R 37		RES,CHIP,CERM,3K,+-5%,0.125W,1206	746511	89536	746511	1		
R 38		RES,CHIP,CERM,7.5K,+-5%,0.125W,1206	746586	89536	746586	1		
R 39		RES,CHIP,CERM,2K,+-5%,0.125W,1206	746461	89536	746461	1		
R 40		RES,CHIP,CERM,1.8K,+-5%,0.125W,1206	746453	89536	746453	1		
TP 1- 7		TERM, UNINSUL,WIRE FORM,TEST POINT	781237	89536	781237	7		
U 1	*	IC,NMOS,8 BIT MICROCOMP W/SOCKET	800607	89536	800607	1	1	
U 1	*	PROGRAMMED 2732-2 V1.0	818187	89536	818187	1	1	
U 2	*	IC,LSTTL,OCTAL D F/F,+EDG TRG,SOIC	741975	89536	741975	1	1	
U 3	*	IC,2K X 8 STATIC RAM,120NSEC,SOIC	742783	89536	742783	1	2	
U 4	*	IC,LSTTL,DUAL DIV BY 2, 5 CNTR,SOIC	741967	89536	741967	1	1	
U 5- 12	*	IC,BIMOS,DISPLAY DRIVER,80V,PLCC	741231	89536	741231	8	2	
U 13, 14	*	IC,LSTTL,DUAL D F/F,+EDG TRG,SOIC	740985	89536	740985	2	1	
U 15, 27	*	IC,ALSTTL,DUAL JK F/F,-EDG TRG,SOIC	807578	89536	807578	2	1	
U 16	*	IC,LSTTL,QUAD 2 INPUT NAND GATE,SOIC	741033	89536	741033	1	1	
U 17, 31	*	IC,LSTTL,QUAD 2 INPUT NOR GATE,SOIC	741025	89536	741025	2	1	
U 18	*	IC,CMOS,HEX INVERTER,SOIC	742585	89536	742585	1	1	
U 19, 20	*	IC,LSTTL,TRIPLE 3-INPUT AND GATE,SOIC	741264	89536	741264	2	1	
U 21	*	IC,LSTTL,QUAD 2 INPUT OR GATE,SOIC	740878	89536	740878	1	1	
U 22	*	IC,TTL,HEX INVERTER,W/OPEN COLL,SOIC	741249	89536	741249	1	1	
U 23, 24	*	IC,CMOS,8 BIT P/S-IN,S-OUT SHFT,SOIC	782904	89536	782904	2	1	
U 25, 30	*	IC,ALSTTL,OCTL D F/F,+EDG TRG,SOIC	741769	89536	741769	2	1	
U 26	*	IC,LSTTL,BCD-DEC,DECODER/DRIVER,SOIC	742007	89536	742007	1	1	
U 28	*	IC,LSTTL,DIV BY 16 BINARY COUNTR,SOIC	741991	89536	741991	1	1	
U 29	*	IC,BPLR,DUAL TIMER,SOIC	741959	89536	741959	1	1	
VF 1		TUBE,DISPLAY,VAC FLUOR,PATTERN DIS	742056	89536	742056	1		
VR 1- 2		ZENER,UNCOMP,3.3V,5%,76MA,1W,MLF	800599	89536	800599	2	1	
XU 1		SOCKET,IC,40 PIN	429282	09922	DILB40P-108	1		
Y 1		CRYSTAL,9.8304MHZ,+-50PPM,SURFACE MT.	800383	89536	800383	1		

An * in 'S' column indicates a static-sensitive part.



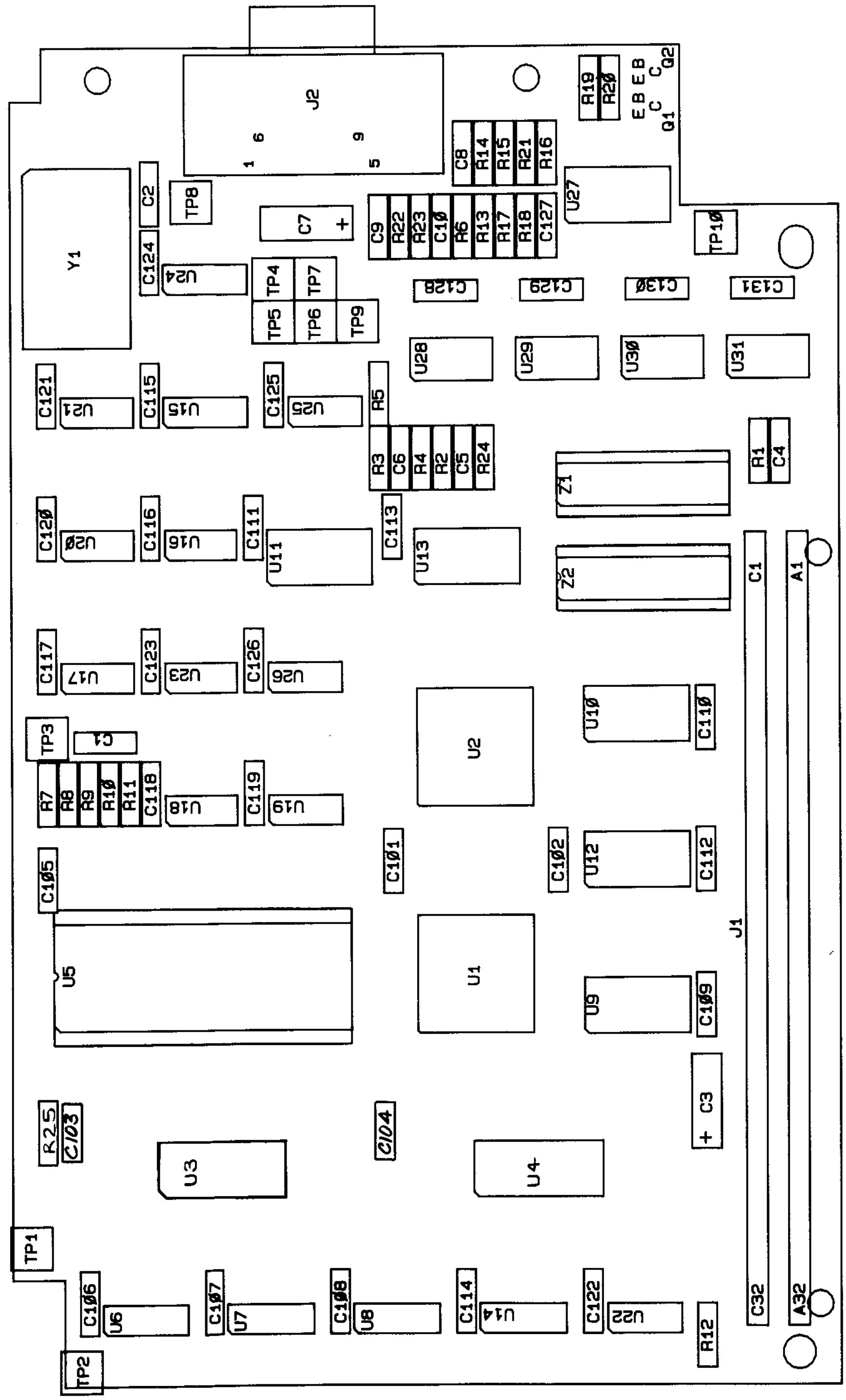
9100A-1602

Figure 5-3. A2 Display Interface PCA

Table 5-5. A4 Video Controller PCA
(See Figure 5-4.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C	1,101-131		CAP,CER,0.01UF,+-10%,50V,X7R,1206	747261	89536	747261	32		
C	2, 8		CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	89536	747287	2		
C	3, 7		CAP,TA,10UF,+-20%,25V	772491	89536	772491	2	1	
C	4- 6		CAP,CER,33PF,+-10%,50V,COG,1206	769240	89536	769240	3		
C	9, 10		CAP,CER,120PF,+-10%,50V,COG,1206	740589	89536	740589	2		
H	1		SCREW,THD CUT,PHP,S.STL,4-24X3/8	183574	89536	183574	2		
J	1		CONN,DIN41612,TYPE R,RT ANG,64 SCKT	782102	89536	782102	1		
J	2		CONN,D-SUB,PWB,RT ANG,9 SCKT	782789	89536	782789	1		
Q	1		TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT23	742676	89536	742676	1	1	
Q	2		TRANSISTOR,SI,PNP,SMALL SIGNAL,SOT23	742684	89536	742684	1	1	
R	1- 5, 14,		RES,CHIP,CERM,330,+-5%,0.125W,1206	746370	89536	746370	7		
R	15			746370					
R	6, 13		RES,CHIP,CERM,510,+-5%,0.125W,1206	746388	89536	746388	2		
R	7- 11		RES,CHIP,CERM,158,+-1%,0.125W,1206	769828	89536	769828	5		
R	12		RES,CHIP,CERM,1K,+-5%,0.125W,1206	745992	89536	745992	1		
R	16		RES,CHIP,CERM,470,+-5%,0.125W,1206	740506	89536	740506	1		
R	17		RES,CHIP,CERM,47,+-5%,0.125W,1206	746263	89536	746263	1		
R	18		RES,CHIP,CERM,220,+-5%,0.125W,1206	746347	89536	746347	1		
R	19		RES,CHIP,CERM,2.4K,+-5%,0.125W,1206	746495	89536	746495	1		
R	20		RES,CHIP,CERM,1.6K,+-5%,0.125W,1206	746446	89536	746446	1		
R	21		RES,CHIP,CERM,5.1K,+-5%,0.125W,1206	746560	89536	746560	1		
R	22, 23		RES,CHIP,CERM,22,+-5%,0.125W,1206	746230	89536	746230	2		
R	24, 25		RES,CHIP,CERM,10K,+-5%,0.125W,1206	746610	89536	746610	2		
TP	1- 10		TERM,UNINSUL,WIRE FORM,TEST POINT	781237	89536	781237	10		
U	1	*	IC,NMOS,ADV VIDEO DISPLAY CNTRLR,PLCC	742734	89536	742734	1	1	
U	2	*	IC,BIPOLAR,CLR/MONO ATTRI CNTRLR,PLCC	742742	89536	742742	1	1	
U	3, 4	*	IC,2K X 8 STATIC RAM,120NSEC,SOIC	742783	89536	742783	2	1	
U	5	*	PROGRAMMED 27128-150 V1.0	818195	89536	818195	1	1	
U	6- 8	*	IC,FTTL,QUAD 2-1 LINE MUX,SOIC	773028	89536	773028	3	1	
U	9, 10	*	IC,LSTTL,OCTL LINE DRVR,SOIC	742122	89536	742122	2	1	
U	11, 12	*	IC,LSTTL,OCTL D TRNSPRNT LATCHES,SOIC	742726	89536	742726	2	1	
U	13	*	IC,LSTTL,OCTAL D F/F,+EDG TRG,SOIC	741975	89536	741975	1	1	
U	14	*	IC,LSTTL,QUAD D F/F,+EDG TRG,SOIC	742619	89536	742619	1	1	
U	15	*	IC,STTL,QUAD D F/F,+EDG TRG,SOIC	742700	89536	742700	1	1	
U	16- 19	*	IC,LSTTL,QUAD 2 INPUT NAND GATE,SOIC	741033	89536	741033	4	1	
U	20, 21	*	IC,LSTTL,TRIPLE 3-INPUT AND GATE,SOIC	741264	89536	741264	2	1	
U	22	*	IC,LSTTL,HEX INVERTER,SOIC	741017	89536	741017	1	1	
U	23	*	IC,LSTTL,SINGLE 8-INP. NAND GATE,SOIC	742510	89536	742510	1	1	
U	24	*	IC,ALSTTL,DUAL JK F/F,-EDG TRG,SOIC	807578	89536	807578	1	1	
U	25	*	IC,STTL,QUAD 2 INPUT +OR GATE,SOIC	742692	89536	742692	1	1	
U	26	*	IC,LSTTL,QUAD 2 INPUT AND GATE,SOIC	740860	89536	740860	1	1	
U	27	*	IC,LSTTL,OCTAL BUFFER INVERTED,SOIC	742627	89536	742627	1	1	
U	28	*	ISOLATOR,OPTO,DUAL,DTL/TTL COMPATABLE	418285	28480	5082-4364	1	1	
U	29- 31	*	ISOLATOR, 20 MHZ OPTOCOUPLER	742817	89536	742817	3	1	
XU	5		SOCKET,IC,28 PIN	448217	91506	328-AG39D	1		
XY	1		SPACER,DIP SOCKET,14 PIN,PLASTIC	441865	32559	814-060	1		
XZ	1, 2		SOCKET,IC,16 PIN	276535	91506	316-AG39D	2		
Y	1		OSCILLATOR,31.9399 MHZ,TTL CLOCK	800029	89536	800029	1		

An * in 'S' column indicates a static-sensitive part.



9100A-1604

Figure 5-4. A4 Video Controller PCA

Table 5-6. A5 Probe Assembly
(See Figure 5-5.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C 1		CAP,CER,27PF,+-10%,50V,COG,1206	800508	89536	800508	1		
C 2, 5		CAP,CER,1000PF,+-10%,50V,COG,1206	747378	89536	747378	2		
C 3, 4		CAP,CER,0.22UF,+80-20%,50V,Y5V,1206	740597	89536	740597	2		
C 6		CAP,CER,0.22UF,+80-20%,50V,Y5V,1206	740597	89536	740597	1		
CR 1- 4		DIODE,SI,BV=75.0V,IO=100MA,MLF	742064	89536	742064	4	1	
CR 5		DIODE,SI,BV=75.0V,IO=100MA,MLF	742064	89536	742064	1	1	
L 1- 3		LAMP,SUB-MIN,5V,20MA	836239	89536	836239	3	5	
MP 1		CONNECTOR,GROUND CLIP,FINISHED	788026	89536	788026	1	1	
MP 2		COVER,PROBE	773309	89536	773309	1		
MP 3		KEYTOP	773333	89536	773333	1		
MP 4		BODY,PROBE	773317	89536	773317	1		
MP 5		DECAL,PROBE CONNECTOR	773929	89536	773929	1		
Q 1, 2		TRANSISTOR,SI,PNP,SMALL SIGNAL,SOT23	742023	89536	742023	2	1	
Q 3, 4		TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT23	742031	89536	742031	2	1	
R 1		RES,CHIP,CERM,220,+-5%,0.125W,1206	746347	89536	746347	1		
R 2		RES,CHIP,CERM,100K,+-1%,0.125W,1206	769802	89536	769802	1	1	
R 3, 8, 10		RES,CHIP,CERM,200,+-5%,0.125W,1206	746339	89536	746339	3		
R 4		RES,CHIP,CERM,330,+-5%,0.125W,1206	746370	89536	746370	1		
R 5, 7		RES,CHIP,CERM,470,+-5%,0.125W,1206	740506	89536	740506	2		
R 6		RES,CHIP,CERM,470,+-5%,0.125W,1206	740506	89536	740506	1		
R 9		RES,CHIP,CERM,205K,+-1%,0.125W,1206	769836	89536	769836	1	1	
R 11- 13		RES,CHIP,CERM,1K,+-5%,0.125W,1206	745992	89536	745992	3		
S 1		SWITCH,PUSHBUTTON,SPST,MOMENTARY	782656	89536	782656	1	3	
U 1	*	IC,FTTL,HEX INVERT W/SCHMT TRIG,SOIC	742825	89536	742825	1	1	
W 1		WIRE,TEF,E,28AWG,STRN,BLU	558320	89536	558320	1		
W 2		CABLE ASSY, PROBE	783951	89536	783951	1		

An * in 'S' column indicates a static-sensitive part.

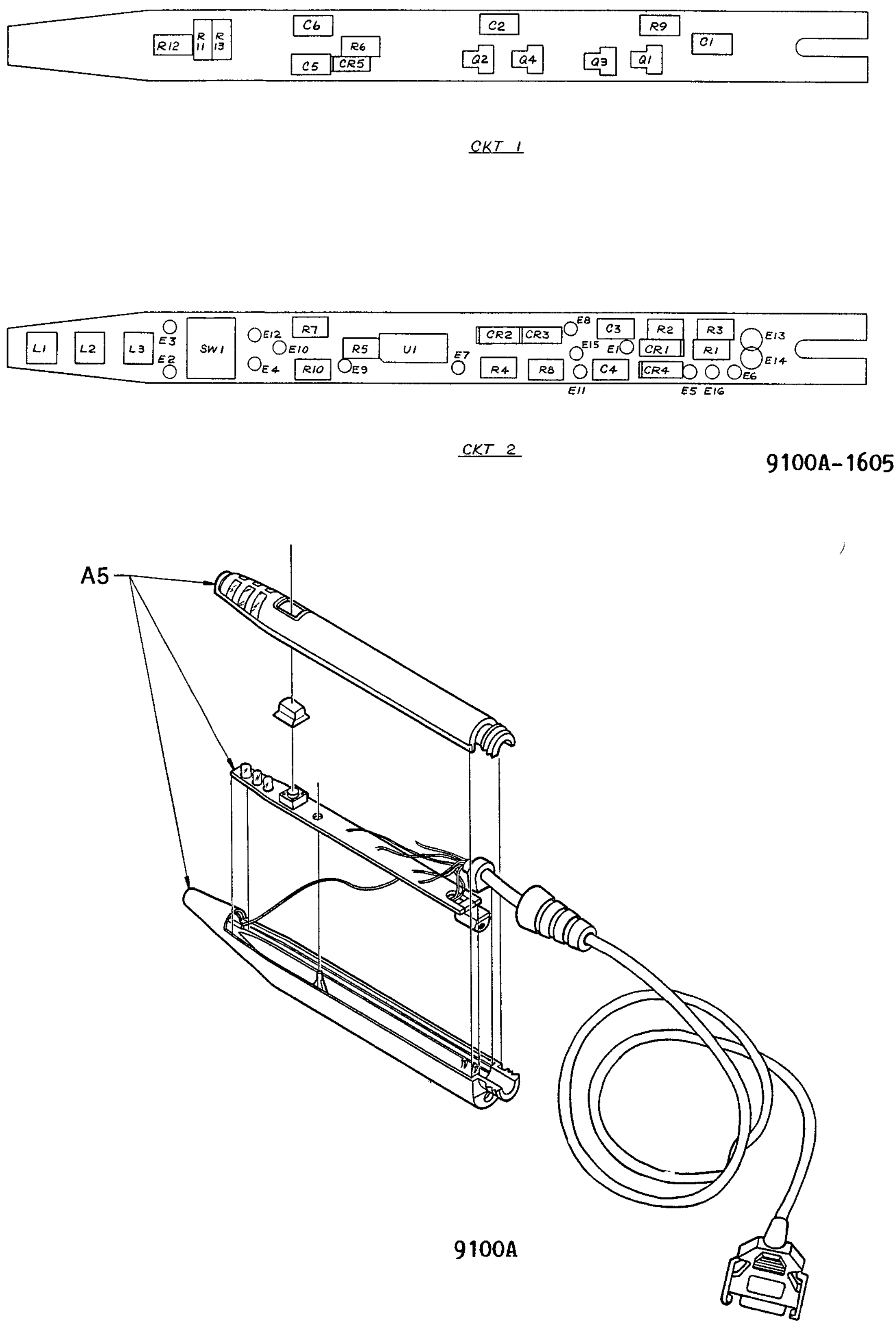


Figure 5-5. A5 Probe PCA

Table 5-7. A6 Clock Module PCA
(See Figure 5-6.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	--------------DESCRIPTION--------------	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C	1- 4		CAP,CER,8.2PF,+-10%,50V,COG,1206	747303	89536	747303	4		
C	5- 12, 14		CAP,CER,0.01UF,+-10%,50V,X7R,1206	747261	89536	747261	9		
C	13		CAP,TA,10UF,+-20%,25V	772491	89536	772491	1		
CR	1- 4		DIODE,SI,BV=70.0V,IO=50MA,DUAL,SOT23	742320	89536	742320	4		
F	1		FUSE,1/4X1-1/4,FAST,0.25A,250V	109314	71400	AGC1-4	1	5	
F	1		FUSE,5X20MM,FAST,0.25A,250V	543504	71400	GMA1-4	1	5	
J	1- 5		PIN,SINGLE,PWB,0.058 DIA	233411	00779	60599-3	5		
J	6		HEADER,2 ROW,0.100CTR,RT ANG,16 PIN	417030	89536	417030	1		
MP	1		FUSE CAP, 1/4 X 1-1/4	460238	61935	031.1666	1		
MP	1		FUSE CAP, 5 X 20 MM	461020	89536	461020	1		
R	1- 8		RES,CHIP,CERM,22K,+-5%,0.125W,1206	746651	89536	746651	8		
R	9- 12		RES,CHIP,CERM,11K,+-5%,0.125W,1206	769752	89536	769752	4		
R	13, 24- 27		RES,CHIP,CERM,100,+-5%,0.125W,1206	746297	89536	746297	5	1	
R	14		RES,CHIP,CERM,16K,+-5%,0.125W,1206	769745	89536	769745	1		
R	15- 22		RES,CHIP,CERM,330,+-5%,0.125W,1206	746370	89536	746370	8		
R	23		RES,CHIP,CERM,10K,+-5%,0.125W,1206	746610	89536	746610	1		
U	1, 2	*	IC,COMPRTR,DUAL,HI-SPEED,16 PIN DIP	782219	89536	782219	2	1	
XF	1		HLDR PART,FUSE,BODY,PWB MT	602763	89536	602763	1		
XU	1, 2		SOCKET,IC,16 PIN	276535	91506	316-AG39D	2		

An * in 'S' column indicates a static-sensitive part.

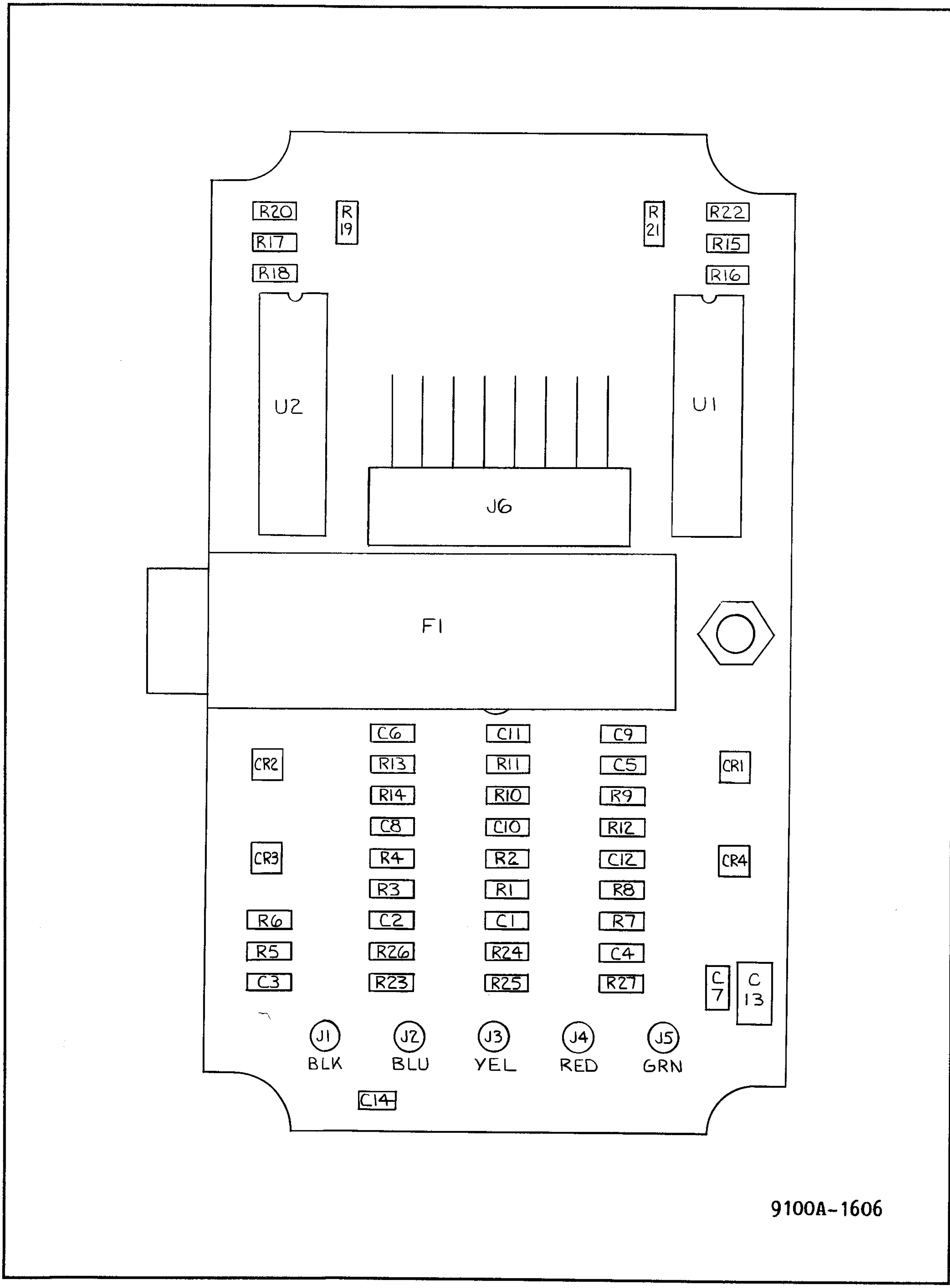


Figure 5-6. A6 Clock Module PCA

Table 5-8. A7 I/O Module Main PCA
(See Figure 5-7.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	--------------DESCRIPTION--------------	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C	1, 2, 9-		CAP,TA,10UF,+-20%,25V	772491	89536	772491	27		
C	24, 27, 37,			772491					
C	42- 44, 61,			772491					
C	62, 67, 68			772491					
C	3- 7, 28-		CAP,CER,0.01UF,+-10%,50V,X7R,1206	747261	89536	747261	31		
C	36, 38, 39,			747261					
C	46- 60			747261					
C	45		CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	89536	747287	1		
CR	1- 4, 7,		DIODE,SI,BV=70.0V,IO=50MA,DUAL,SOT23	742320	89536	742320	85	5	
CR	100-179			742320					
CR	5, 6		DIODE,SI,BV=75.0V,IO=100MA,MLF	742064	89536	742064	2	1	
CR	8		DIODE,SI,SCHOTTKY,30V,1.1A,SOT89	782573	89536	782573	1	1	
E	1- 5		PIN,SINGLE,PWB,0.058 DIA	233411	00779	60599-3	5		
F	1		FUSE,1/4 X 1-1/4,SLOW,1.0A,250V	109272	89536	109272	1	5	
F	1		FUSE,5X20MM,SLOW,1A,250V	808055	89536	808055	1	5	
H	1		SCREW,MACH,PHP SEMS,STL,6-32X1/4	178533	89536	178533	1		
J	1		HEADER,2 ROW,0.100CTR,RT ANG,38 PIN	782748	89536	89536	1		
J	2, 3		SOCKET,2 ROW,PWB,0.100CTR,30 POS	783795	89536	783795	2		
MP	1		SPACER,HEX,ALUM,6-32X0.625	104448	89536	104448	1		
P	1		HEADER,1 ROW,0.150CTR,RT ANG,6 PIN	783803	89536	783803	1		
Q	1, 2		TRANSISTOR,SI,PNP,SMALL SIGNAL,SOT23	742684	89536	742684	2	1	
R	1, 2		RES,CHIP,CERM,100,+-5%,0.125W,1206	746297	89536	746297	2		
R	3, 5, 6,		RES,CHIP,CERM,10K,+-1%,0.125W,1206	769794	89536	769794	4		
R	10			769794					
R	4, 9		RES,CHIP,CERM,42.2K,+-1%,0.125W,1206	769851	89536	769851	2		
R	7		RES,CHIP,CERM,7.5K,+-1%,0.125W,1206	811463	89536	811463	1		
R	8		RES,CHIP,CERM,825,+-1%,0.125W,1206	811455	89536	811455	1		
R	13, 14		RES,CHIP,CERM,9.1K,+-5%,0.125W,1206	746602	89536	746602	2		
R	15, 17		RES,CHIP,CERM,43K,+-5%,0.125W,1206	769299	89536	769299	2		
R	16, 18		RES,CHIP,CERM,910,+-5%,0.125W,1206	769257	89536	769257	2		
R	19, 20, 23-		RES,CHIP,CERM,4.7K,+-5%,0.125W,1206	740522	89536	740522	10		
R	30			740522					
R	21, 22, 31,		RES,CHIP,CERM,1K,+-5%,0.125W,1206	745992	89536	745992	7		
R	33, 34, 39,			745992					
R	40			745992					
R	32		RES,CHIP,CERM,11K,+-5%,0.125W,1206	769752	89536	769752	1		
TP	1- 8		TERM,UNINSUL,WIRE FORM,TEST POINT	781237	89536	781237	8		
U	1		OSCILLATOR,1 MHZ,TTL CLOCK	634113	89536	634133	1		
U	2	*	IC,OP AMP,QUAD,LOW POWER,SOIC	742569	89536	742569	1	1	
U	3, 5	*	IC,LSTTL,QUAD 2 INPUT AND GATE,SOIC	740860	89536	740860	2	1	
U	4	*	IC,CMOS,HEX INVERTER,SOIC	742585	89536	742585	1	1	
U	6	*	IC,LSTTL,3-8 LINE DCDR W/ENABLE,SOIC	740969	89536	740969	1	1	
U	7	*	IC,LSTTL,OCTL D TRNSPRNT LATCHES,SOIC	742726	89536	742726	1	1	
U	8	*	IC,CMOS,OCTAL BUS TRANSCEIVER,SOIC	742577	89536	742577	1	1	
U	9	*	IC,ECL,QUAD ECL-TTL TRANSLATOR	801274	89536	801274	1	1	
U	10	*	IC,LSTTL,QUAD 2 INPUT OR GATE,SOIC	740878	89536	740878	1	1	
U	11, 12	*	IC,LSTTL,DUAL JK F/F,-EDG TRIG,SOIC	741256	89536	741256	2	1	
U	13, 16, 17	*	IC,CMOS,OCTL LINE DRVR,SOIC	742593	89536	742593	3	2	
U	14	*	IC,LSTTL,OCTAL D F/F,+EDG TRG,SOIC	740928	89536	740928	1	1	
U	15	*	IC,LSTTL,SINGLE 8-INP. NAND GATE,SOIC	742510	89536	742510	1	1	
U	18	*	IC,CMOS,DUAL 4-1 SELECT/MUX,SOIC	780767	89536	780767	1	1	
U	100,110,120,	*	IC CMOS QUEST 9000 CHIP CERAMIC TEST	760785	89536	760785	5	1	
U	130,140	*		760785					
U	101,103,111,	*	TRANSISTOR,SI,P-DMOS,POWER FET,14 PIN	800185	89536	800185	10	2	
U	113,121,123,	*		800185					
U	131,133,141,	*		800185					
U	143	*		800185					
U	102,104,112,	*	TRANS,SI,N-DMOS PWR FET,QUAD	782557	89536	782557	10	2	
U	114,122,124,	*		782557					
U	132,134,142,	*		782557					
U	144	*		782557					
U	105,106,115,	*	IC,CMOS,OCTL LINE DRVR,SOIC	801043	89536	801043	10	1	
U	116,125,126,	*		801043					
U	135,136,145,	*		801043					
U	146	*		801043					
XF	1		HLDR PART,FUSE,BODY,PWB MT	602763	89536	602763	1		
XY	1		SPACER,DIP SOCKET,14 PIN,PLASTIC	441865	32559	814-060	1		
Z	1,100,110,		RES,NET,DIP,16PIN,8RES,100,+-5%	780460	89536	780460	6	1	
Z	120,130,140			780460					

An * in 'S' column indicates a static-sensitive part.

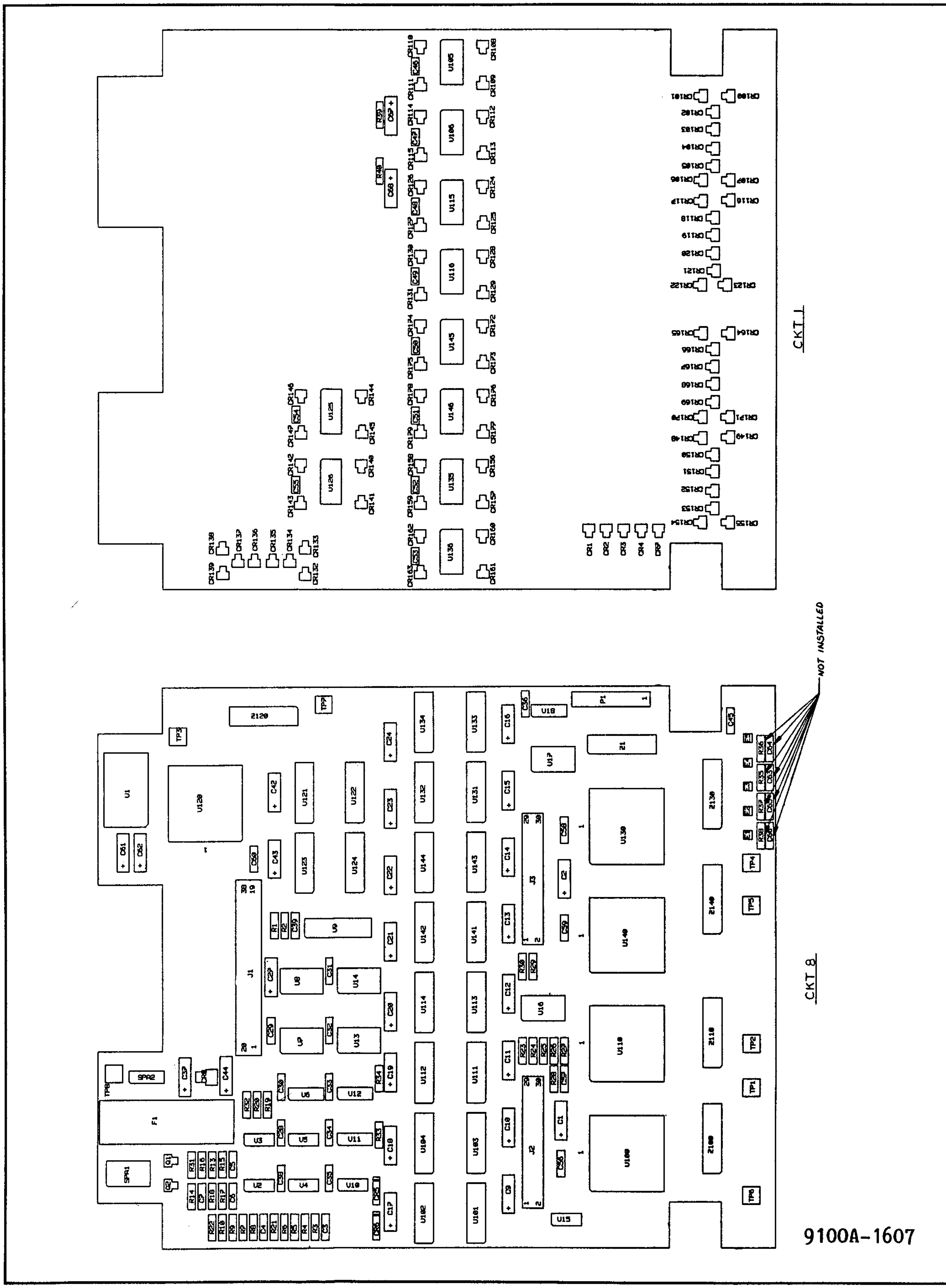


Figure 5-7. A7 I/O Module (Main) PCA

Table 5-9. A8 I/O Module (Top) PCA
(See Figure 5-8.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C 1- 4		CAP,AL,4700UF,+-20%,16V,SOLV PROOF	800904	89536	800904	4	1	
CR 1- 4	*	DIODE,SI,100 PIV,1.0 AMP	343491	01295	1N4002	4	1	
H 1		SCREW,MACH,PHP SEMS,STL,6-32X1/4	178533	89536	178533	2		
H 2		SCREW,MACH,PHP SEMS,STL,4-40X3/16	732750	89536	732750	4		
J 1, 4		HEADER,2 ROW,0.100CTR,30 PIN	801233	89536	801233	2		
J 2, 3		CONN,RECT,PWB,REC,33 POS	800672	89536	800672	2		
MP 1		COVER, SHIELD I/O MODULE	768036	89536	768036	1		
MP 2		SPACER,SWAGED,RND,BRASS,6-32X0.590	811224	89536	811224	5		
MP 3		SPACER,SWAGED,RND,BRASS,6-32X0.250	446351	89536	446351	2		
P 1- 4		GUIDE SOCKET	805648	89536	805648	4		

An * in 'S' column indicates a static-sensitive part.

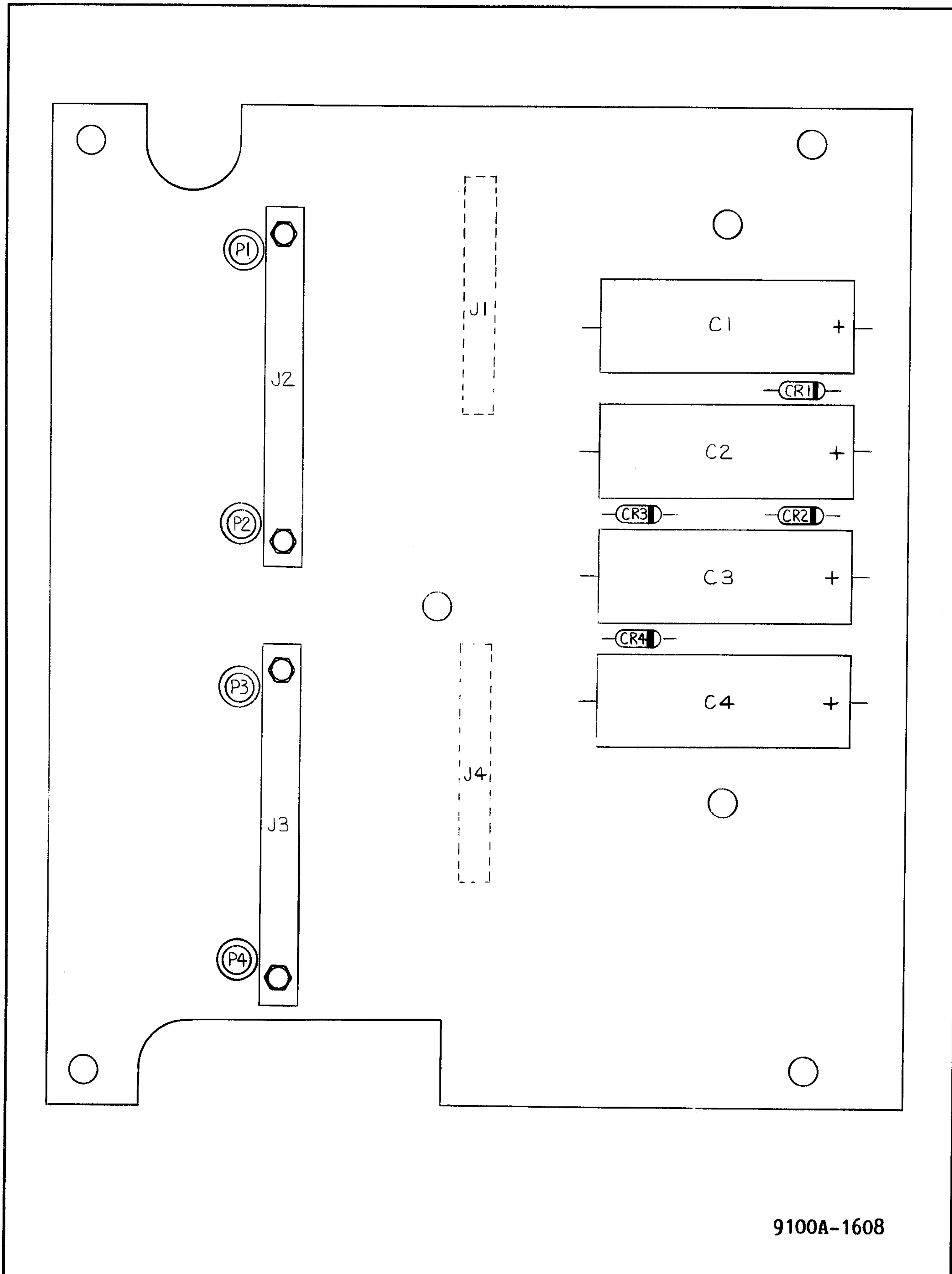


Figure 5-8. A8 I/O Module (Top) PCA

Table 5-10. A9 Probe I/O Interface PCA
(See Figure 5-9.)

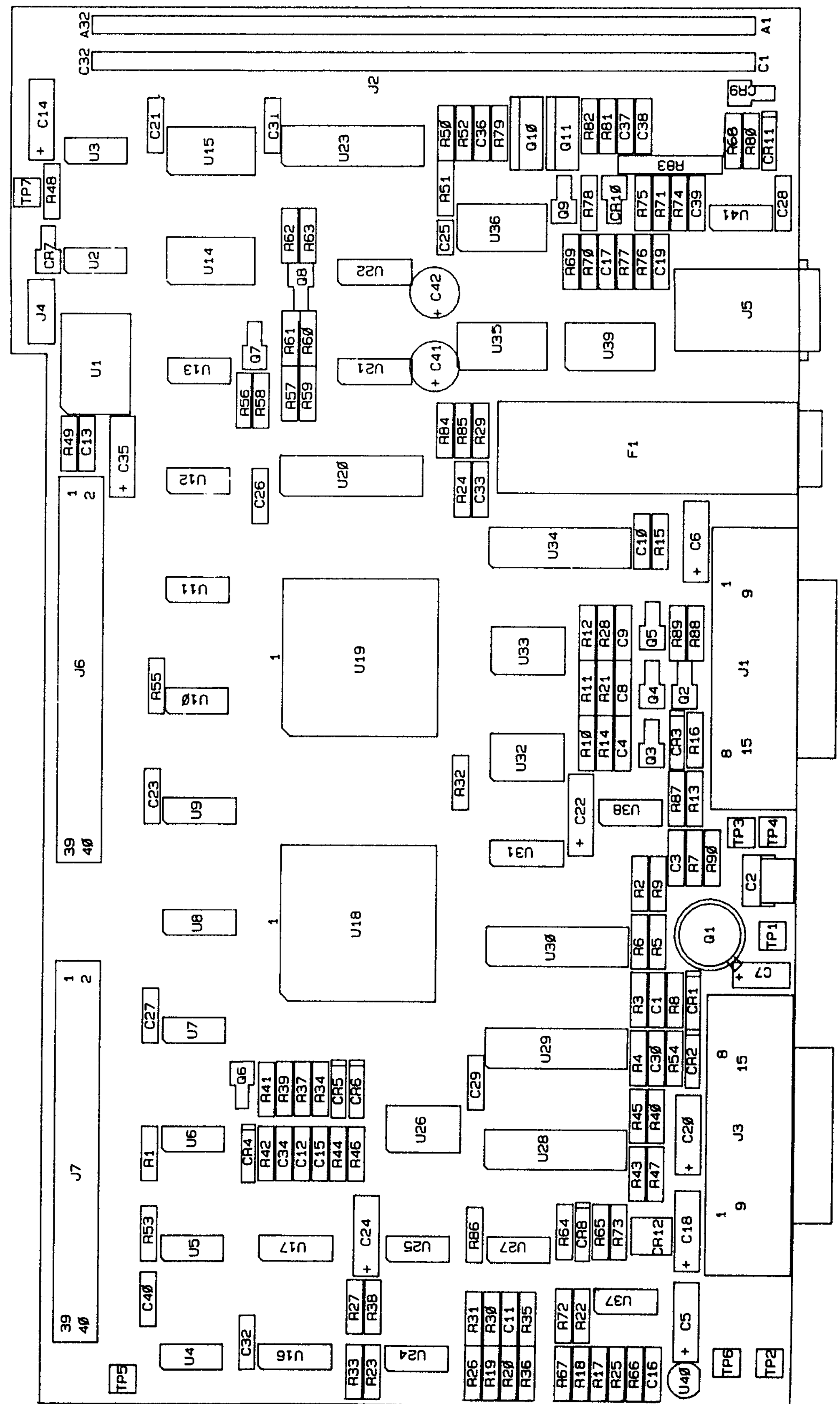
REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	--------------DESCRIPTION--------------	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C	1, 3, 4,		CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	89536	747287	23		
C	8- 11, 16,			747287					
C	17, 19, 21,			747287					
C	23, 25- 33,			747287					
C	39, 40			747287					
C	2		CAP,VAR,6-50PF,50V,CER	714618	89536	714618	1		
C	5, 7, 20,		CAP,TA,10UF,+-20%,25V	772491	89536	772491	6		
C	22, 24, 35			772491					
C	6, 14, 18		CAP,TA,1.5UF,+-20%,50V	780478	89536	780478	3		
C	12		CAP,CER,180PF,+-10%,50V,COG,1206	769778	89536	769778	1		
C	13		CAP,CER,33PF,+-10%,50V,COG,1206	769240	89536	769240	1		
C	15		CAP,CER,0.022UF,+-10%,50V,X7R,1206	747279	89536	747279	1		
C	34		CAP,CER,1500PF,+-10%,50V,COG,1206	781203	89536	781203	1		
C	36		CAP,CER,470PF,+-10%,50V,COG,1206	747360	89536	747360	1		
C	37, 38		CAP,CER,0.01UF,+-10%,50V,X7R,1206	747261	89536	747261	2		
C	41, 42		CAP,TA,47UF,+-20%,20V	348516	56289	196D476X0020TE4	2		
CR	1- 6, 8,		DIODE,SI,BV=75.0V,IO=100MA,MLF	742064	89536	742064	8	1	
CR	11			742064					
CR	7, 9, 10		DIODE,SI,BV=70.0V,IO=50MA,DUAL,SOT23	742320	89536	742320	3	2	
CR	12		DIODE,SI,SCHOTTKY,30V,1.1A,SOT89	782573	89536	782573	1	1	
F	1		FUSE,1/4X1-1/4,FAST,0.25A,250V	109314	71400	AGC1-4	1	5	
F	1		FUSE,5X20MM,FAST,0.25A,250V	543504	71400	GMA1-4	1	5	
J	1		CONN,D-SUB,PWB,RT ANG,15 SCKT	782169	89536	782169	1		
J	2		CONN,DIN41612,TYPE R,64 PIN	782094	89536	782094	1		
J	3		CONN,D-SUB,PWB,RT ANG,15 PIN	782151	89536	782151	1		
J	4		HEADER,1 ROW,0.100CTR,RT ANG,6 PIN	714154	89536	714154	1		
J	5		JACK,PWB,RT ANG,4 POS	782086	89536	782086	1		
J	6, 7		HEADER,2 ROW,0.100 CTR,40 PIN	603670	89536	603670	2		
MP	1		FUSE CAP 1/4X1-1/4	460238	61935	031.1666	1		
MP	1		FUSE CAP 5 X 20 MM	461020	89536	461020	1		
Q	1	*	TRANSISTOR,SI,N-JFET,DUAL,TO-78	478370	89536	478370	1	1	
Q	2, 6, 7,		TRANSISTOR,SI,PNP,SMALL SIGNAL,SOT23	742023	89536	742023	4	1	
Q	9			742023					
Q	3, 4, 5,		TRANSISTOR,SI,NPN,SMALL SIGNAL,SOT23	742031	89536	742031	4	1	
Q	8			742031					
Q	10, 11	*	TRANSISTOR,SI,BV= 45V, 30W,TO-220	325761	09214	D44C5	2	1	
R	1		RES,CHIP,CERM,33,+-5%,0.125W,1206	746248	89536	746248	1		
R	2		RES,CHIP,CERM,3.6K,+-5%,0.125W,1206	746537	89536	746537	1		
R	3- 6, 48,		RES,CHIP,CERM,330,+-5%,0.125W,1206	746370	89536	746370	6		
R	49			746370					
R	7		RES,CHIP,CERM,150,+-5%,0.125W,1206	746313	89536	746313	1		
R	8		RES,CHIP,CERM,15K,+-1%,0.125W,1206	769810	89536	769810	1		
R	9		RES,CHIP,CERM,22,+-5%,0.125W,1206	746230	89536	746230	1		
R	10- 12, 14,		RES,CHIP,CERM,470,+-5%,0.125W,1206	740506	89536	740506	6		
R	21, 28			740506					
R	13, 15		RES,CHIP,CERM,200,+-5%,0.125W,1206	746339	89536	746339	2		
R	16, 46, 51,		RES,CHIP,CERM,511,+-1%,0.125W,1206	769869	89536	769869	4		
R	59			769869					
R	17, 20, 26,		RES,CHIP,CERM,1K,+-5%,0.125W,1206	745992	89536	745992	8		
R	31, 36, 41,			745992					
R	54, 78			745992					
R	18, 22, 23,		RES,CHIP,CERM,4.7K,+-5%,0.125W,1206	740522	89536	740522	23		
R	27, 32- 34,			740522					
R	37, 38, 42,			740522					
R	52, 53, 55,			740522					
R	56, 58, 61-			740522					
R	63, 67, 72,			740522					
R	80, 82, 86			740522					
R	19, 35, 84,		RES,CHIP,CERM,47K,+-5%,0.125W,1206	746685	89536	746685	4		
R	85			746685					
R	24, 29, 30		RES,CHIP,CERM,9.1K,+-5%,0.125W,1206	746602	89536	746602	3		
R	25		RES,CHIP,CERM,3.9K,+-5%,0.125W,1206	746545	89536	746545	1		
R	39		RES,CHIP,CERM,470K,+-5%,0.125W,1206	746792	89536	746792	1		
R	40, 43, 45,		RES,CHIP,CERM,100,+-5%,0.125W,1206	746297	89536	746297	6		
R	47, 79, 81			746297					
R	44		RES,CHIP,CERM,300K,+-5%,0.125W,1206	746768	89536	746768	1		
R	50, 57		RES,CHIP,CERM,1.15K,+-1%,0.125W,1206	780981	89536	780981	2		
R	60		RES,CHIP,CERM,4.02K,+-1%,0.125W,1206	783266	89536	783266	1		
R	64		RES,CHIP,CERM,750,+-5%,0.125W,1206	746404	89536	746404	1		
R	65		RES,CHIP,CERM,39K,+-5%,0.125W,1206	746677	89536	746677	1		

An * in 'S' column indicates a static-sensitive part.

Table 5-10. A9 Probe I/O Interface PCA (cont.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	--------------DESCRIPTION--------------	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
R 68, 75		RES,CHIP,CERM,30.1K,+-1%,0.125W,1206	801258	89536	801258	2		
R 69		RES,CHIP,CERM,47,+-5%,0.125W,1206	746263	89536	746263	1		
R 70		RES,CHIP,CERM,3.4K,+-1%,0.125W,1206	769844	89536	769844	1		
R 71, 74, 76,		RES,CHIP,CERM,10K,+-1%,0.125W,1206	769794	89536	769794	4		
R 77			769794					
R 73		RES,CHIP,CERM,620,+-5%,0.125W,1206	745984	89536	745984	1		
R 83		RES,CF,2.2,+-5%,0.25W	354944	80031	CR251-4-5P2E2	1	1	
R 87		RES,CHIP,CERM,1.30K,+-1%,0.125W,1206	780999	89536	780999	1		
R 88		RES,CHIP,CERM,243,+-1%,0.125W,1206	810606	89536	810606	1	1	
R 90		RES,CHIP,CERM,22,+-5%,0.125W,1206	746230	89536	746230	1		
TP 1- 7		TERM,UNINSUL,WIRE FORM,TEST POINT	781237	89536	781237	7		
U 1		ISOLATOR, 20 MHZ OPTOCOUPLER	742817	89536	742817	1	1	
U 2	*	IC,FTTL,QUAD 2 INPUT XOR GATE,SOIC	742171	89536	742171	1	1	
U 3	*	IC,LSTTL,QUAD 2 INPUT NOR GATE,SOIC	741025	89536	741025	1	1	
U 4, 12	*	IC,FTTL,HEX INVERTER,SOIC	742148	89536	742148	2	1	
U 5	*	IC,FTTL,QUAD DUAL AND GATE,SOIC	780957	89536	780957	1	1	
U 6	*	IC,CMOS,HEX INVERTER W/SCHT TRIG,SOIC	780965	89536	780965	1	1	
U 7, 13	*	IC,LSTTL,QUAD 2 INPUT OR GATE,SOIC	740878	89536	740878	2	1	
U 8	*	IC,LSTTL,2-4 LINE DEMUX,SOIC	740951	89536	740951	1	1	
U 9	*	IC,FTTL,QUAD 2-1 LINE MUX,SOIC	773028	89536	773028	1	1	
U 10	*	IC,FTTL,DUAL D F/F,+EDG TRG,SOIC	742163	89536	742163	1	1	
U 11	*	IC,FTTL,QUAD 2 INPUT OR GATE,SOIC	743237	89536	743237	1	1	
U 14, 15	*	IC,LSTTL,OCTL LINE DRVR,SOIC	742122	89536	742122	2	1	
U 16	*	IC,FTTL,DUAL 4-1 LINE MUX,SOIC	772806	89536	772806	1	1	
U 17	*	IC,LSTTL,QUAD D F/F,+EDG TRG,SOIC	742619	89536	742619	1	1	
U 18	*	IC,STTL,600 GATE ARY,9100A-99100,PLCC	741546	89536	741546	1	1	
U 19	*	IC,STTL,600 GATE ARY,9100A-99101,PLCC	741553	89536	741553	1	1	
U 20, 23	*	IC,BIPOLAR,8-BIT DAL,UP-COMPATIBLE	743112	89536	743112	2	1	
U 21, 22	*	IC,LSTTL,8-BIT BINARY CNTR W/REG,SOIC	782243	89536	782243	2	1	
U 24, 37	*	IC,COMPARATOR,QUAD,14 PIN,SOIC	741561	89536	741561	2	1	
U 25	*	IC,LSTTL,QUAD BUS,SOIC	740977	89536	740977	1	1	
U 26, 32, 33	*	IC,LSTTL, 4 BIT UP/DOWN CNTR,SOIC	742114	89536	742114	3	1	
U 27	*	IC,LSTTL,DUAL D F/F,+EDG TRG,SOIC	740985	89536	740985	1	1	
U 28, 29	*	IC,ECL,QUAD ECL-TTL TRANSLATOR	801274	89536	801274	2	1	
U 30	*	IC,COMPRTR,DUAL,HI-SPEED,16 PIN DIP	782219	89536	782219	1	1	
U 31	*	IC,FTTL,QUAD D F/F,+EDG TRG,SOIC	801399	89536	801399	1	1	
U 34	*	IC,FTTL, 4 BIT UP/DOWN COUNTER	782235	89536	782235	1	1	
U 35, 36, 39	*	IC,LSTTL,OCTL BUS TRNSCVR W/3-ST,SOIC	781195	89536	781195	3	1	
U 38	*	IC,FTTL,DUAL 4 INPUT NAND GATE,SOIC	742155	89536	742155	1	1	
U 40	*	IC,VOLT REG,FIXED,+5 VOLTS,0.1 AMPS	429910	07263	uA78L05AWC	1	1	
U 41	*	IC,OP AMP,QUAD,LOW POWER,SOIC	742569	89536	742569	1	1	
XF 1		HLDR PART,FUSE,BODY,PWB MT	602763	89536	602763	1		

An * in 'S' column indicates a static-sensitive part.



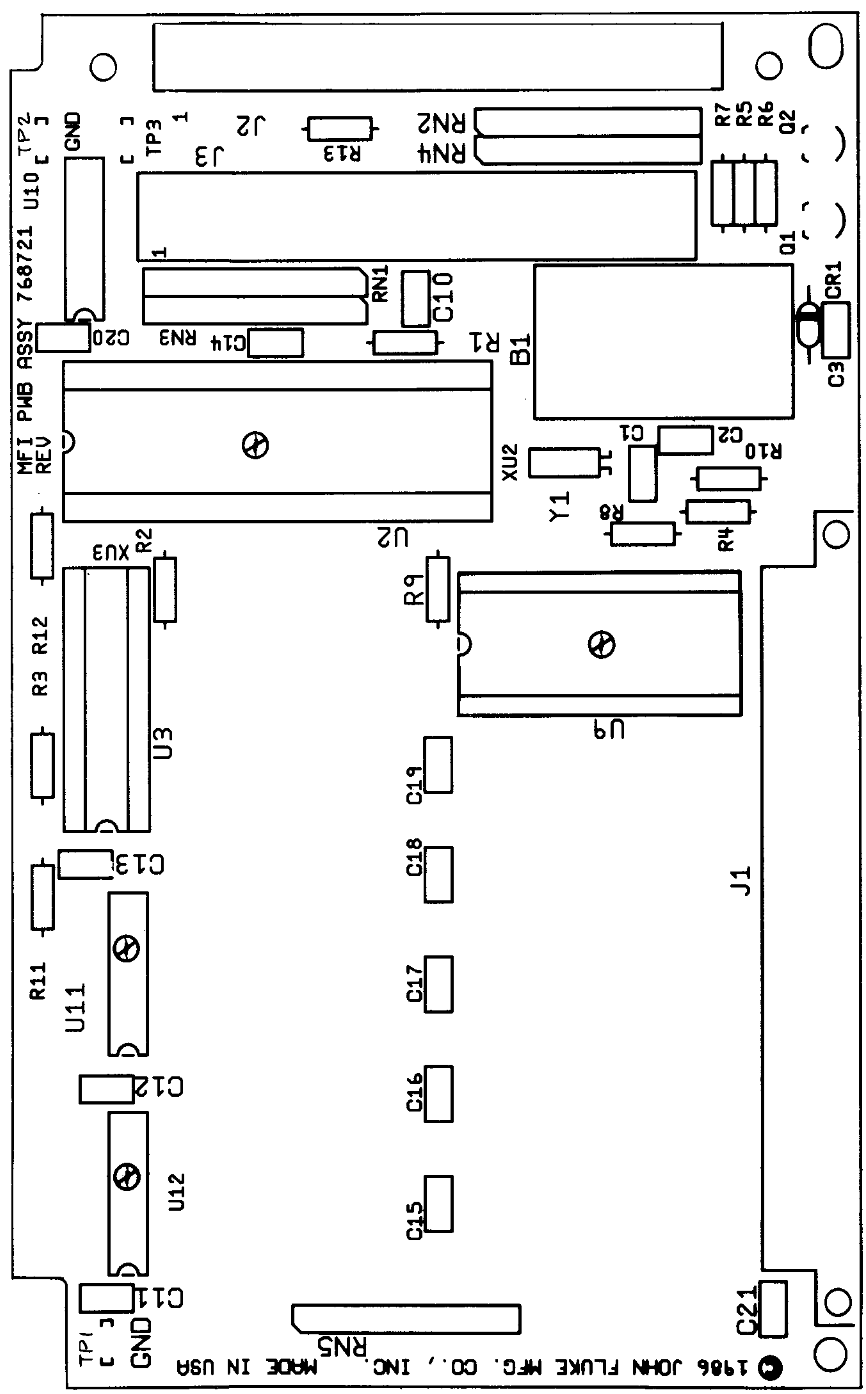
9100A-1609

Figure 5-9. A9 Probe I/O Interface PCA

Table 5-11. A10 Multi-Function Interface PCA
(See Figure 5-10.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
B 1		BATTERY,LITHIUM,3.5V,0.75AH	782953	89536	782953	1	1	
C 1, 2		CAP,CER,15PF,+-2%,100V,COG	369074	89536	369074	2	1	
C 3, 10- 21		CAP,CER,0.01UF,+-20%,100V,X7R	407361	72982	8121-A100-W5R-103M	13		
CR 1	*	DIODE,SI,BV= 75.0V,IO=150MA,500 MW	203323	07910	1N4448	1	1	
H 1		SCREW,THD CUT,PHP,S.STL.4-24X3/8	183574	89536	183574	2		
H 2		RIVET,POP,DOME,AL,0.125X0.316	423616	89536	423616	2		
J 1		CONN,DIN41614,TYPE R,RT ANG,96 SCKT	747816	89536	747816	1		
J 2		HEADER,2 ROW,0.100 CTR,RT ANG,50 PIN	783464	89536	783464	1		
J 3		HEADER,2 ROW,0.100CTR,50 PIN	782201	89536	782201	1		
MP 1		SCSI CONNECTOR BRACKET	768663	89536	768663	1		
Q 1	*	TRANSISTOR,SI,PNP,SMALL SIGNAL	195974	64713	2N3906	1	1	
Q 2	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	218396	04713	2N3904	1	1	
R 1- 3, 6,		RES,CF,10K,+-5%,0.25W	348839	80031	CR251-4-5P10K	7		
R 7, 9, 12			348839					
R 4		RES,CC,22M,+-5%,0.25W	221986	01121	CB2265	1		
R 5		RES,CF,51K,+-5%,0.25W	376434	80031	CR251-4-5P51K	1		
R 8, 10		RES,CF,200K,+-5%,0.25W	441485	80031	CR251-4-5P200K	2		
RN 1, 2		RES,NET,SIP,10PIN,9RES,220,+-2%	769356	89536	769356	2		
RN 3, 4		RES,NET,SIP,10PIN,9RES,330,+-2%	769364	89536	769364	2		
RN 5		RES,NET,SIP,10PIN,9RES,10K,+-2%	414003	80031	95081002CL	1		
TP 1- 3		TERM,UNINSUL,WIRE FORM,TEST POINT	781237	89536	781237	3		
U 2	*	IC,NMOS,SMALL COMPTR SYS INT	742858	89536	742858	1	1	
U 3	*	IC,20L8, PROGRAMMED LOGIC ARRAY	818211	89536	818211	1	1	
U 9	*	IC,CMOS,PARALLEL,I/O CALENDER & CLOCK	604181	12040	MM58167N	1	1	
U 10	*	IC,LSTTL,8BIT S-IN, P-OUT R-SHIFT RGS	408732	01295	SN74LS164N	1	1	
U 11	*	IC,CMOS,HEX INVERTERS	799924	89536	799924	1	1	
U 12	*	IC,CMOS,QUAD 2-INPUT NAND GATE	741280	89536	741280	1	1	
XU 2		SOCKET,IC,40 PIN	429282	09922	DILB40P-108	1		
XU 3		SOCKET,IC,24 PIN,	643999	89536	643999	1		
XU 9		SOCKET,IC,24 PIN	376236	91506	324-AG39D	1		
Y 1	*	CRYSTAL,32.768KHZ,+-0.003%	501817	89536	501817	1	1	

An * in 'S' column indicates a static-sensitive part.



9100A-1610

Figure 5-10. A10 Multi-Function Interface PCA

Table 5-12. A11 I/O Connector PCA
(See Figure 5-11.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	NOTE
C 1, 17		CAP,AL,1000UF,+50-20%,35V	641217	57640	SM/VB	2		
C 2- 15		CAP,CER,0.01UF,+-20%,100V,X7R	407361	72982	8121-A100-W5R-103M	14	1	
C 16		CAP,AL,10000UF,+-20%,6.3V,SOLV PROOF	800045	89536	800045	1		
CR 1, 2	*	DIODE,SI,100 PIV,1.0 AMP	343491	01295	1N4002	2	1	
H 1		SCREW,MACH,PH,P,STL,6-32X0.250	152140	89536	152140	2		
H 2		SCREW,THD CUT,PHP,S.STL,4-24X3/8	183574	89536	183574	2		
J 1		CONN,DIN41612,TYPE R,RT ANG,64 SCKT	782102	89536	782102	1		
J 2- 5		CONN,D-SUB,PWB,37 SCKT	782177	89536	782177	4		
MP 1		HEAT DISSIPATOR,1.000,FOR TO-66	799965	89536	799965	1		
R 1		RES,CF,10K,+-5%,0.25W	348839	80031	CR251-4-5P10K	1		
R 3		RES,WW,0.47,+-5%,2W	219360	89536	219360	1	1	
R 4		RES,MF,243,+-0.1%,0.125W,50PPM	512228	89536	512228	1		
R 5		RES,MF,732,+-1%,0.125W,100PPM	294884	89536	294884	1		
TP 1		TERM,UNINSUL,WIRE FORM,TEST POINT	781237	89536	781237	1		
U 1, 2	*	IC,ECL,QUAD TTL-ECL TRANSLATOR	801266	89536	801266	2	1	
U 3	*	IC,LSTTL,DUAL 4 INPUT NAND GATE	393280	01295	SN74LS20N	1	1	
U 4	*	IC,VOLT REG,ADJ,1.2 TO 32 V,5 AMP OUT	585497	12040	LM338K	1	1	
Z 1, 3		RES,NET,SIP,10PIN,9RES,330,+-2%	769364	89536	769364	2		
Z 2		RES,NET,SIP,10PIN,9RES,4.7K,+-2%	484063	80031	95081002CL	1		

An * in 'S' column indicates a static-sensitive part.

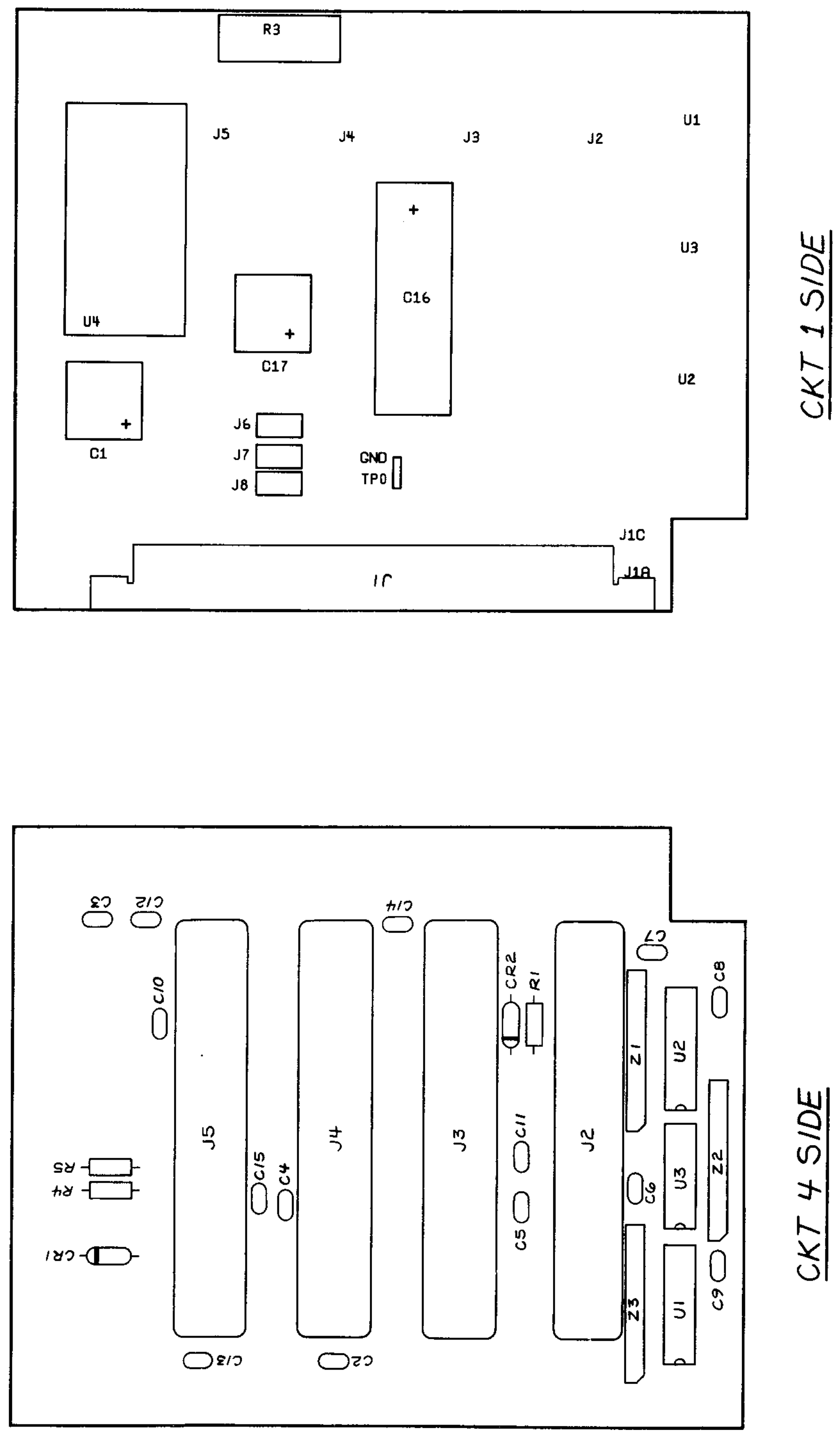


Figure 5-11. A11 I/O Connector PCA

Table 5-13. A12 Half-Width Clip Modules

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	---------------DESCRIPTION---------------	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C 1		CAP,CER,0.1UF,+-20%,50V,Z5U	597575	89536	597575	1		
C 2		CAP,CER,0.01UF,+-20%,100V,X7R	407361	72982	8121-A100-W5R-103M	1		
H 1		SCREW, MACH, PHP, STL, 4-40 X 5/8	800656	89536	800656	4		
J 1		CONN,RECT,PWB,PLUG,33 POS	800680	89536	800680	1	1	
J 2, 3		CONNECTOR ASSY		89536		2		1
MP 1		CLIP,TEST,IC		89536		1	2	1
MP 2		CLIP,HOOK,W/0.025 PIN INTERFACE,BLACK	757500	89536	757500	1	2	
MP 3		BUTTON, SWITCH	773895	89536	773895	1		
MP 4		MODULE BOTTOM, SINGLE	768697	89536	768697	1		
MP 5		MODULE TOP, SINGLE	774034	89536	774034	1		
MP 6		KEY		89536		2		1
MP 7		MODULE DECAL		89536		1		1
P 1, 2		BANANA PLUG,PWB,SOLDER OR SWAGE TYPE	800698	89536	800698	2		
S 1		SWITCH,PUSHBUTTON,SPST,MOMENTARY	782433	89536	782433	1	1	
S 2		SWITCH,DIP,SPST,4 POS	408559	00779	435166-2	1		
W 1		CABLE SET ASSY		89536		1		1
W 2		WIRE ASSY, GROUND CLIP	801704	89536	801704	1	1	

An * in 'S' column indicates a static-sensitive part.

NOTES:

1 = Refer to the table below for appropriate part numbers for each type of Clip Module:

	MODULE -14D	-14S	-16D	-16S	-18D	-20D	-20S	-24D	-24S
MP1	800052	817429	800060	817437	800078	800086	817445	800094	817478
W1	801639	801639	801647	801647	801654	801662	801662	801670	801670
J2,3	801878	801878	801886	801886	801894	801902	801902	801910	801910
MP6	-	-	-	-	773952	773952	773952	767954	767954
MP7	802140	819631	802157	819649	802165	802173	819656	802181	819664

Table 5-14. A13 Full-Width Clip Modules

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C 1, 4		CAP,CER,0.01UF,+-20%,100V,X7R	407361	72982	8121-A100-W5R-103M	2		
C 2, 3		CAP,CER,0.1UF,+-20%,50V,Z5U	597575	89536	597575	2		
H 1		SCREW, MACH, PHP, STL, 4-40 X 5/8	800656	89536	800656	4		
J 1, 2		CONN,RECT,PWB,PLUG,33 POS	800680	89536	800680	2	1	
J 3, 4		CONNECTOR ASSY, 20 PIN		89536		2		1
MP 1		CLIP,TEST,IC		89536		1	2	1
MP 2		CLIP,HOOK,W/0.025 PIN INTERFACE,BLACK	757500	89536	757500	1	2	
MP 3		BUTTON, SWITCH	773895	89536	773895	1		
MP 4		MODULE BOTTOM, DOUBLE	802132	89536	802132	1		
MP 5		MODULE TOP, DOUBLE	802124	89536	802124	1		
MP 6		KEY, EXTENDED	767954	89536	767954	2		
MP 7		MODULE DECAL		89536		1		1
P 1- 4		BANANA PLUG,PWB,SOLDER OR SWAGE TYPE	800698	89536	800698	2		
S 1		SWITCH,PUSHBUTTON,SPST,MOMENTARY	782433	89536	782433	1	1	
S 2		SWITCH,DIP,SPST,8 POS	414490	00779	435166-5	1		
W 1		CABLE SET ASSY		89536		1		1
W 2		WIRE ASSY, GROUND CLIP	801704	89536	801704	1	1	

An * in 'S' column indicates a static-sensitive part.

NOTES:

1 = Refer to the table below for appropriate part numbers for each type of Clip Module:

	MODULE -28D	-28S	-40D
MP1	800102	821975	800110
W1	801688	801688	801696
J3,4	801928	801928	801936
MP7	802199	819672	802207

Table 5-15. A14 Calibration Module

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
H 1		SCREW, MACH, PHP, STL, 4-40 X 5/8	800656	89536	800656	7		
J 1, 2		CONN,RECT,PWB,PLUG,33 POS	800680	89536	800680	2	1	
MP 2		TEST LEAD,CLIP-TO-CLIP,BLK,20AWG	801050	89536	801050	1	1	
MP 3		CABLE TIE,4"L,0.100"W,0.75 DIA	172080	89536	172080	2		
MP 4		BUTTON, SWITCH	773895	89536	773895	1		
MP 5		MODULE BOTTOM, DOUBLE	802132	89536	802132	1		
MP 6		MODULE TOP, DOUBLE	802124	89536	802124	1		
MP 7		KEY, EXTENDED	767954	89536	767954	2		
MP 8		MODULE DECAL, CALIBRATION	802223	89536	802223	1		
P 1- 4		BANANA PLUG,PWB,SOLDER OR SWAGE TYPE	800698	89536	800698	2		
S 1		SWITCH,PUSHBUTTON,SPST,MOMENTARY	782433	89536	782433	1	1	

An * in 'S' column indicates a static-sensitive part.

Table 5-16. A15 Flying Lead Module

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C 1		CAP,CER,0.1UF,+-20%,50V,Z5U	597575	89536	597575	1		
C 2		CAP,CER,0.01UF,+-20%,100V,X7R	407361	72982	8121-A100-W5R-103M	1		
H 1		SCREW, MACH, PHP, STL, 4-40 X 5/8	800656	89536	800656	4		
J 1		CONN,RECT,PWB,PLUG,33 POS	800680	89536	800680	1	1	
MP 1		BUTTON, SWITCH	773895	89536	773895	1		
MP 2		MODULE BOTTOM, SINGLE	768697	89536	768697	1		
MP 3		MODULE TOP, SINGLE	774034	89536	774034	1		
MP 4		KEY	773952	89536	773952	2		
MP 5		MODULE DECAL	802215	89536	802215	1		
MP 6		CLIP, HOOK	757500	89536	757500	25	10	
P 1, 2		BANANA PLUG,PWB,SOLDER OR SWAGE TYPE	800698	89536	800698	2		
S 1		SWITCH,PUSHBUTTON,SPST,MOMENTARY	782433	89536	782433	1	1	
S 2		SWITCH,DIP,SPST,4 POS	408559	00779	435166-2	1		
W 1		CABLE ASSY, 10 PAIR, POS 1-10	801712	89536	801712	1		
W 2		CABLE ASSY, 10 PAIR, POS 1-10	801720	89536	801720	1		

An * in 'S' column indicates a static-sensitive part.

Table 5-17. A16 512K RAM Module
(See Figure 5-12.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
C 1- 22		CAP,CER,0.1UF,+/-10%,25V,X7R,1206	747287	89536	747287	22		
C 23		CAP,CER,47PF,+-10%,50V,COG,1206	747352	89536	747352	1		
U 1- 9, 11-	*	IC, NMOS, 256K X 1 DRAM, 120NSEC, PLC	808212	89536	808212	18	1	
U 19	*		808212					
U 10	*	IC,ALSTTL,OCTAL BUS TRANSCEIVER,SOIC	799593	89536	799593	1	1	
U 20	*	IC,ALSTTL,QUAD 2 INPUT NAND GATE,SOIC	782268	89536	782268	1	1	
U 21	*	IC,ALSTTL,QUAD 2 INPUT OR GATE,SOIC	742460	89536	742460	1	1	
U 22	*	IC,ALSTTL,DUAL JK F/F,-EDG TRG,SOIC	807578	89536	807578	1	1	

An * in 'S' column indicates a static-sensitive part.

NOTE

The 9105A-007 uses two A16 512K RAM Modules.

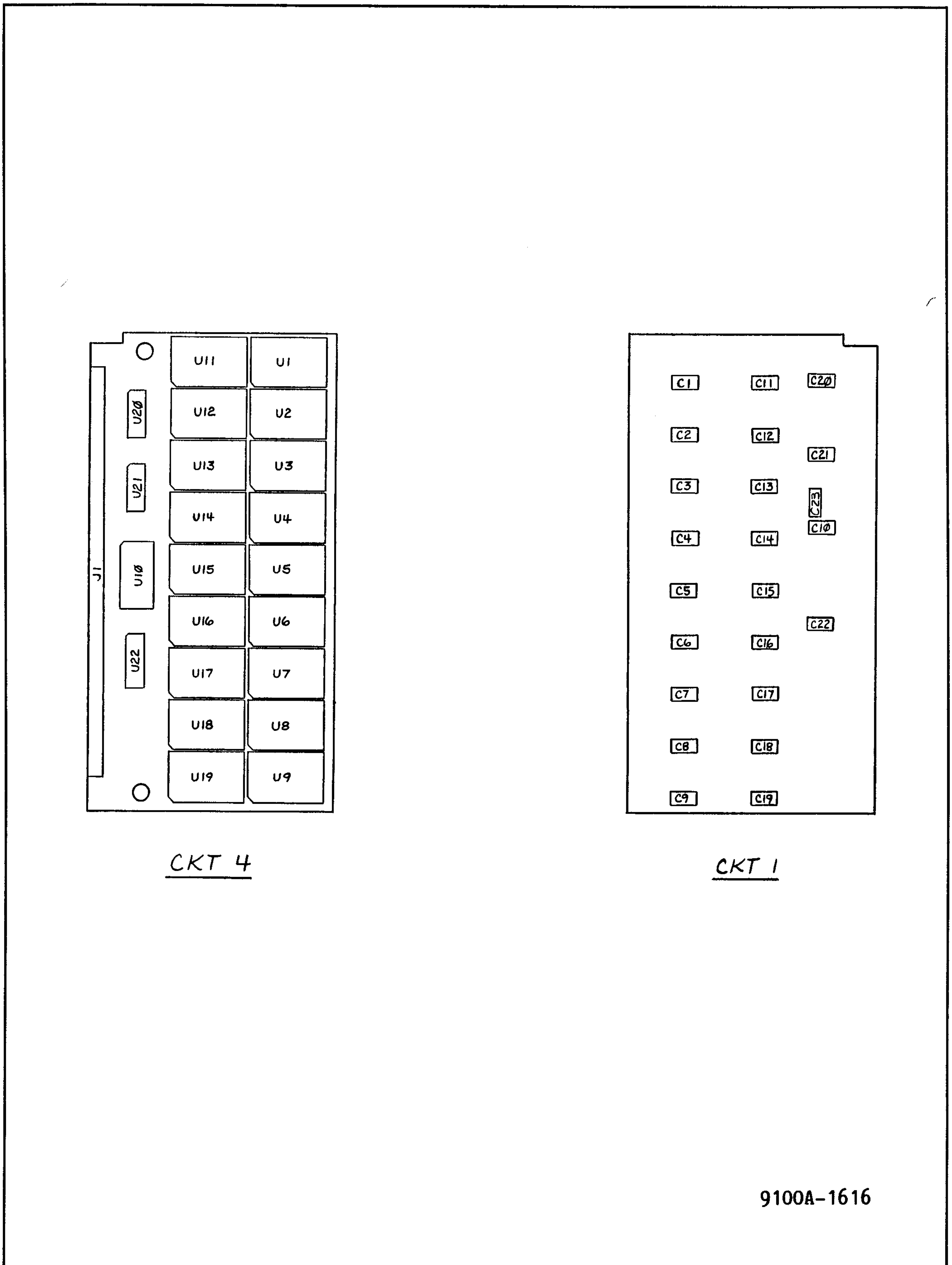


Figure 5-12. A16 512K RAM Module

Table 5-18. A19 Monochrome Monitor

REFERENCE DESIGNATOR -A>-NUMERICS---->		S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
BT	1		POWER SUP,40W,+5@3.5A,+12@2A,-12@1A	769406	89536	769406	1		
H	1		SCREW,MACH,PH,P,STL,10-32X0.375	114314	73734	19084	4		
H	2		WASHER,FLAT,STEEL,0.203X0.434X0.031	110262	89536	110262	3		
H	3		WASHER,FLAT,STL,.149,.375,.031	110270	89536	110270	8		
H	4		SCREW,MACH,PH,P,STL,6-32X0.375	152165	89536	152165	8		
H	5		SCREW,MACH,SEMS,PH,P,STL,6-32X0.375	177022	89536	177022	3		
H	6		SCREW,MACH,SEMS,PH,P,STL,6-32X0.375	177022	89536	177022	5		
H	7		SCREW,MACH,PHP SEMS,STL,4-40X1/4	185918	89536	185918	6		
H	8		CONN ACC,D-SUB,LATCH BLOCK,SHORT,4-40	783480	89536	783480	2		
H	9		SCREW,MACH,PH,P,STL,6-32X1.000	114215	89536	114215	3		
H	10		WASHER,FLAT,STL,.149,.375,.031	110270	89536	110270	3		
H	11		SCREW,MACH,SEMS,PH,P,STL,6-32X0.375	177022	89536	177022	4		
MP	1		BRACKET,CRT,FINISHED	794149	89536	794149	4	1	
MP	2		LABEL,BAR-CODE,9.4 CPI,0.245X1.25	807099	89536	807099	2		
MP	3		CHASSIS,FINISHED	794156	89536	794156	1		
MP	4		SPACER,PWB,NYL,.312	780619	89536	780619	3		
MP	5		BEZEL ASSY,9100	792903	89536	792903	1		
MP	6		GASKET,TOUCH PANEL,DUST	843250	89536	843250	1		
MP	7		NAMEPLATE	787275	89536	787275	1		
MP	8		COVER,CHASSIS,9100,FINISHED	794198	89536	794198	1		
MP	9		DAMPER, VIBRATION	805085	89536	805085	4		
MP	10		CABLE TIE ANCHOR,ADHSV,0.160"TIE	407908	89536	407908	5		
MP	11		CABLE TIE,4"L,0.100"W,0.75 DIA	172080	89536	172080	8		
MP	12		DECAL,COVER,9100	792911	89536	792911	1		
MP	13		DECAL, FAN PANEL	785493	89536	785493	1		
MP	14		BRACKET,POT MOUNTING,FINISHED	794131	89536	794131	1		
MP	15		THUMBWHEEL, POTENTIOMETER	787358	89536	787358	1		
MP	16		SHIPPING BOX	776435	89536	776435	1		
MP	17		SHIPPING INSERT	777045	89536	777045	1		
MP	18		OPTION TRAY	801613	89536	801613	1		
MP	19		SHIPPING CARRIER/INSERT	777052	89536	777052	1		
MP	20		INSERT,OPTION TRAY	809616	89536	809616	1		
MP	21		ENCLOSURE W/GRILLS	802454	89536	802454	1		
MP	22		COVER, FAN	787366	89536	787366	1		
MP	23		DECAL,CAUTION	787242	89536	787242	1		
MP	24		BASE	747972	89536	747972	1		
MP	25		RETAINER, NUT	749655	89536	749655	1		
MP	26		BUSHING COVER RF OUTPUT	802553	89536	802553	1		
MP	27		SHOULDER WASHER	792861	89536	792861	2		
MP	28		RETAINER PIN	802520	89536	802520	1		
MP	29		BASE, MOUNTING PLATE	747998	89536	747998	1		
MP	30		FOOT,RUBBER,SELF-ADHESIVE,BLACK	513820	89536	513820	4		
MP	31		PIN,MECHANICAL,CLEVIS,5/16 X 1-3/4	800524	89536	800524	1		
MP	32		SPRING,COIL,COMP,SQUARED END,M WIRE	800532	89536	800532	1		
MP	33		BUMPER,STEM,BUNA-S,0.500X0.125	800839	89536	800839	4		
MP	34		ASSY, AC POWER PANEL	776377	89536	776377	1		
MP	35		DISPLAY, MONITOR GREEN	785444	89536	785444	1		
MP	36		CONTRAST OVERLAY	819987	89536	819987	0	1	1
W	1		CORD,LINE,5-15/IEC,3-18AWG,SVT	284174	89536	284174	1		
W	2		CABLE ASSY,9100	778613	89536	778613	1		

An * in 'S' column indicates a static-sensitive part.

NOTE 1 = Contrast overlay is part of the bezel assembly.

Table 5-19. Option -003 Parallel I/O Module
(See Figure 5-13.)

REFERENCE DESIGNATOR -A>-NUMERICS---->		S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
A	7	*	I/O MODULE (MAIN) PCA	768838	89536	768838	1		
A	8	*	I/O MODULE (TOP) PCA	755611	89536	755611	1		
A	14		CALIBRATION MODULE	813980	89536	813980	1		
A	15		FLYING LEAD MODULE, 20 LEAD SET, TSTD	819763	89536	819763	1		
F	1		FUSE,1/4 X 1-1/4,SLOW,1.0A,250V	109272	71400	MDL1A	1	5	
F	1		FUSE,5X20MM,SLOW,1A,250V	808055	89536	808055	1	5	
H	1		SCREW,MACH,PHP,STL,6-32 X 7/8	801241	89536	801241	4		
H	2		SCREW,MACH,PHP SEMS,STL,6-32X1/4	178533	89536	178533	9		
MP	1		HLDR PART,FUSE,CAP,1/4X1-1/4	460238	61935	031.1666	1		
MP	2		HLDR PART,FUSE,CAP,5X20MM	461020	89536	461020	1		
MP	3		CASE TOP, I/O MODULE	773291	89536	773291	1		
MP	4		CASE BOTTOM, I/O MODULE	773283	89536	773283	1		
MP	5		DECAL, CASE TOP, I/O MODULE	805630	89536	805630	1		
MP	6		DECAL, CASE BOTTOM, I/O MODULE	773382	89536	773382	1		
MP	7		SHIELD, I/O MODULE	775866	89536	775866	1		
MP	8		FOOT, NON-SKID	774000	89536	774000	4		
MP	9		NAMEPLATE, SERIAL -REAR PANEL-	472795	89536	472795	1		
MP	10		CARTON KEYBOARD, I/O	805804	89536	805804	1		
MP	11		FOAM INSERT, KEYBOARD-I/O	805812	89536	805812	1		
MP	12		CONVOLUTED FOAM, KEYBOARD-I/O	805820	89536	805820	1		
W	1		CABLE ASSEMBLY, EXTERNAL EVENT	773945	89536	773945	1	1	
W	2		CABLE ASSY, I/O MODULE	783977	89536	783977	1		
W	3		WIRE,SHIELD CONTACT	803122	89536	803122	1		

An * in 'S' column indicates a static-sensitive part.

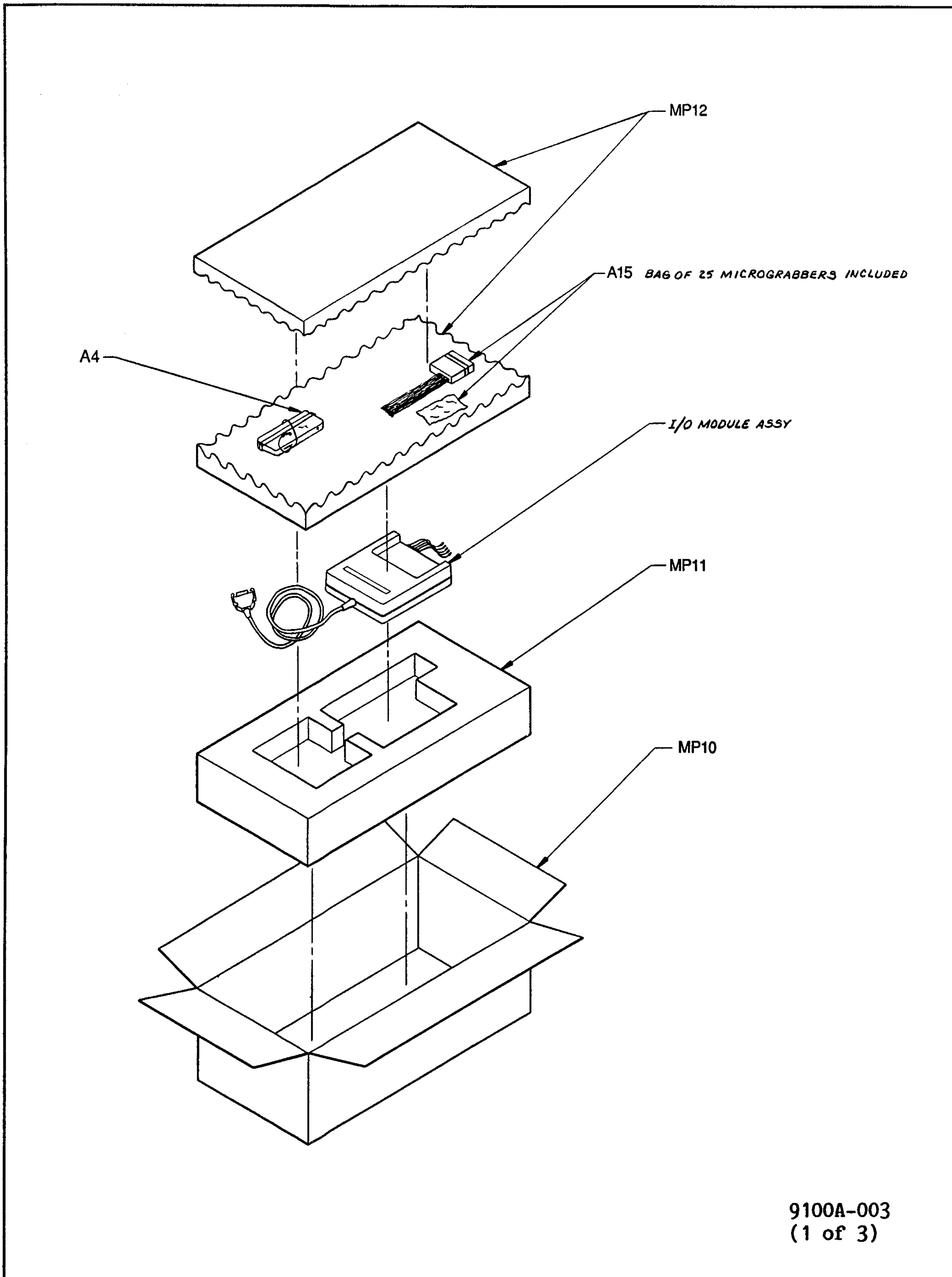


Figure 5-13. Option -003 Parallel I/O Module

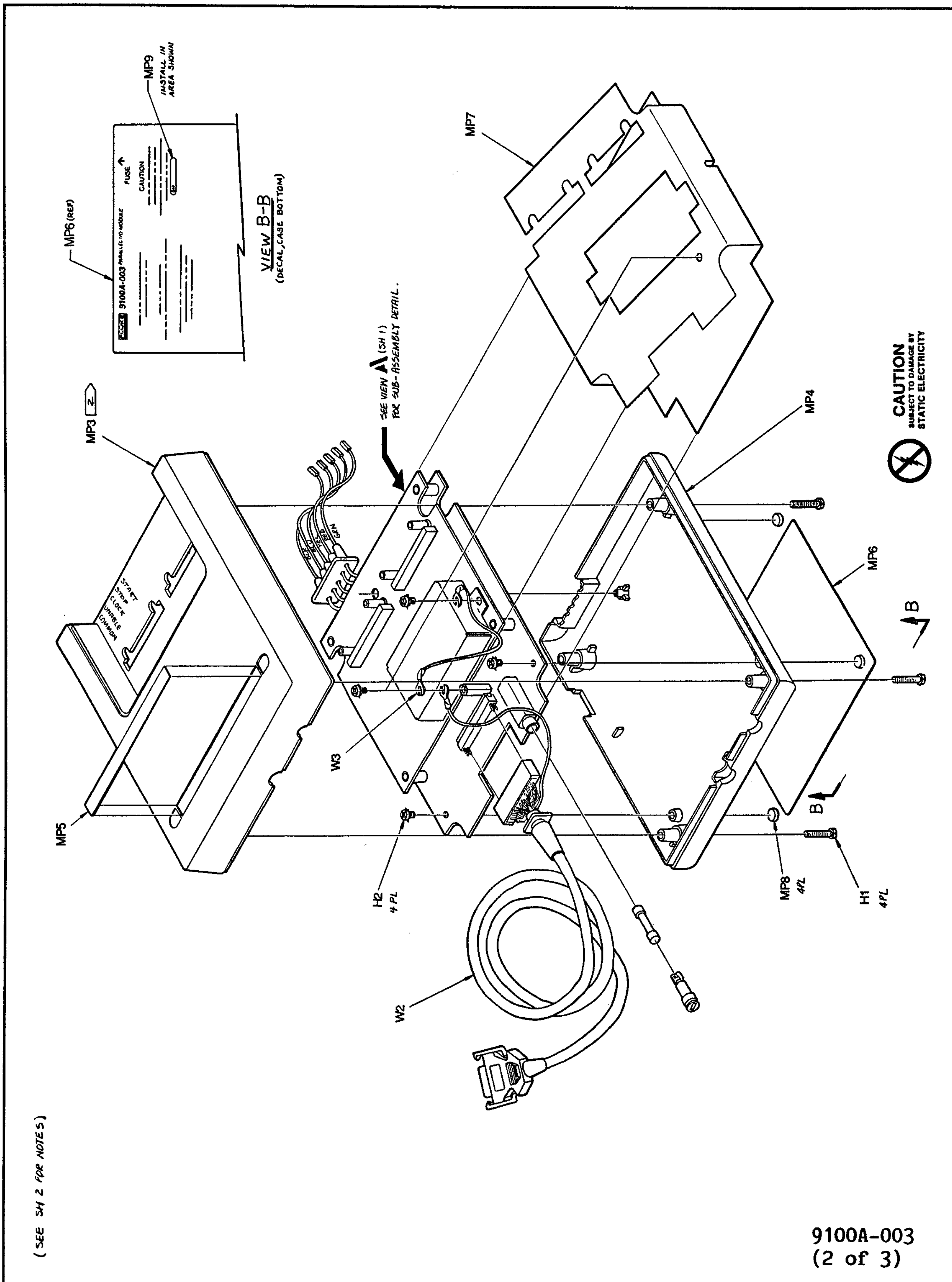
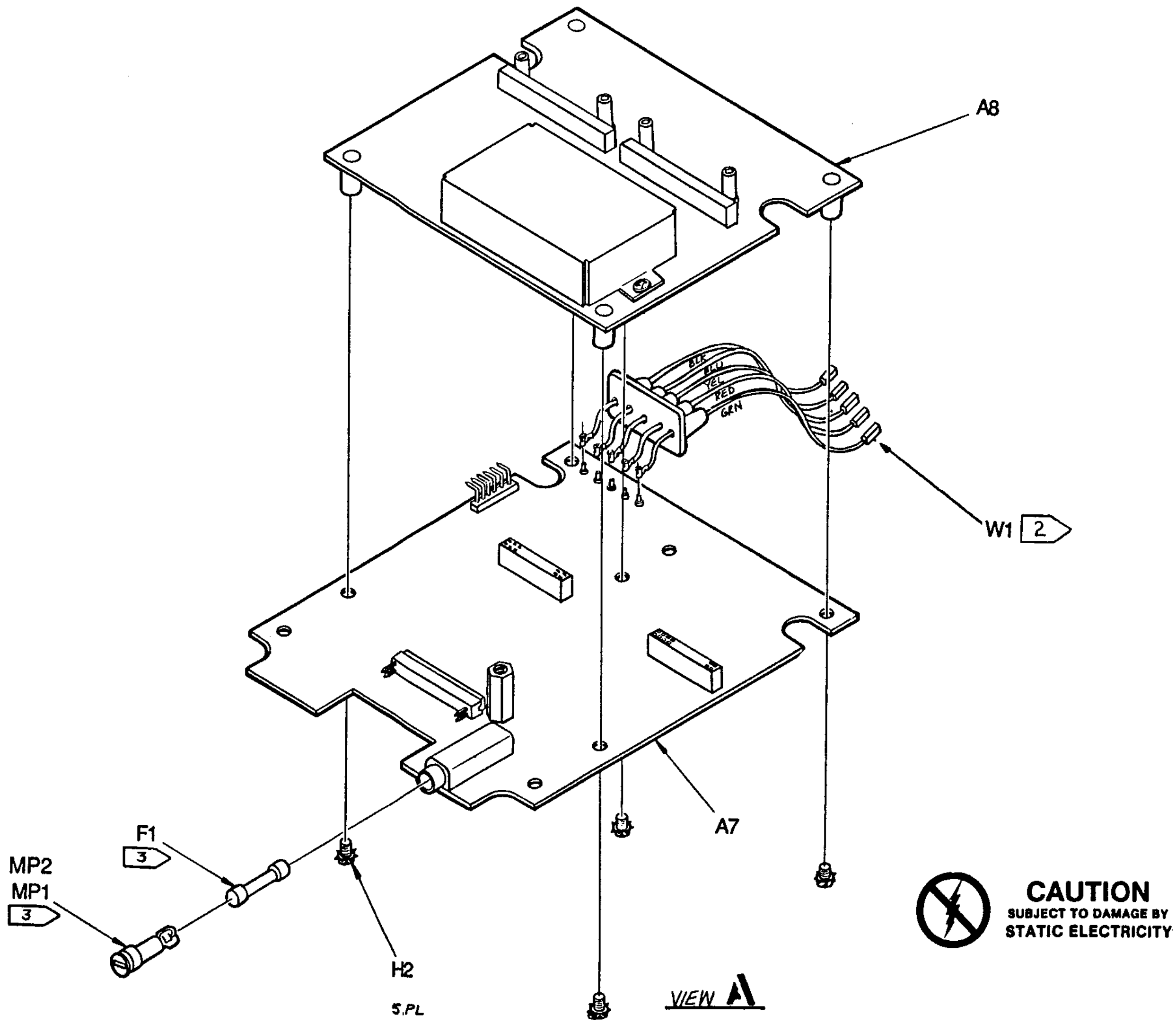


Figure 5-13. Option -003 Parallel I/O Module (cont.)



NOTES: UNLESS OTHERWISE SPECIFIED.

1. **WARNING:** Ⓢ INDICATES USAGE OF MOS DEVICE(S) WHICH MAY BE DAMAGED BY STATIC DISCHARGE. USE SPECIAL HANDLING PER S.O.P. 19.1

2. CABLE NOMENCLATURE ON MP3 CASE TOP SHALL MATCH UP WITH COLORS OF W1 AS NOTED:
   COMMON - BLACK WIRE
   UNABLE - BLUE WIRE
   CLOCK - YELLOW WIRE
   STOP - RED WIRE
   START - GREEN WIRE

3. FUSE & FUSE CAP VARY FOR DIFFERENT VOLTAGE CONFIGURATIONS: SEE FUSE CHART FOR FUSE & CAP PART NO.S.

FUSE CHART 3			CONFIGURATION	
VOLTAGE	FUSE	CAP		
100/120V	109272	460238	115V	763649
220/240V	808055	461020	230V	763656

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Figure 5-13. Option -003 Parallel I/O Module (cont.)

Table 5-20. Option -004 Programmer's Station, Monochrome
(See Figure 5-14.)

REFERENCE DESIGNATOR -A>-NUMERICS---->		S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
A	4	*	VIDEO CONTROLLER PCA	768762	89536	768762	1		
A	19		MONOCHROME MONITOR	826362	89536	826362	1		
A	103		KEYBOARD,ASYNC ASCII, 1200 BAUD	757120	89536	757120	1		1
H	1		RIVET,POP,DOME,AL,0.125X0.316	423616	89536	423616	2		
MP	2		VIDEO CONNECTOR BRACKET	768648	89536	768648	1		
MP	3		NAMEPLATE, SERIAL -REAR PANEL-	472795	89536	472795	1		
MP	4		PROGRAMMER SOFTWARE SYSTEM, SLEEVED		89536		1		2
MP	5		CARTON KEYBOARD, I/O	805804	89536	805804	1		
MP	6		CONVOLUTED FOAM, KEYBOARD-I/O	805820	89536	805820	1		
MP	7		PROGRAM COPY PROTECTION SHEET	847066	89536	847066	1		
TM	1		9100A TL/1 REFERENCE MANUAL	818047	89536	818047	1		
TM	2		9100A PROGRAMMERS MANUAL	813857	89536	813857	1		
U	5	*	PROGRAMMED 27128-150	818195	89536	818195	1		
W	1		CABLE, MONITOR	787903	89536	787903	1		
Z	1		JUMPER,DIP,0.300CTR,PROGRAM,16 POS	783183	89536	783183	1		

An * in 'S' column indicates a static-sensitive part.

NOTES:

1 = See 9100A-013 option for replacement parts breakdown for A103.

2 = This software available only for 9100A's with Programmer's Station installed. Contact the factory if replacement is needed.

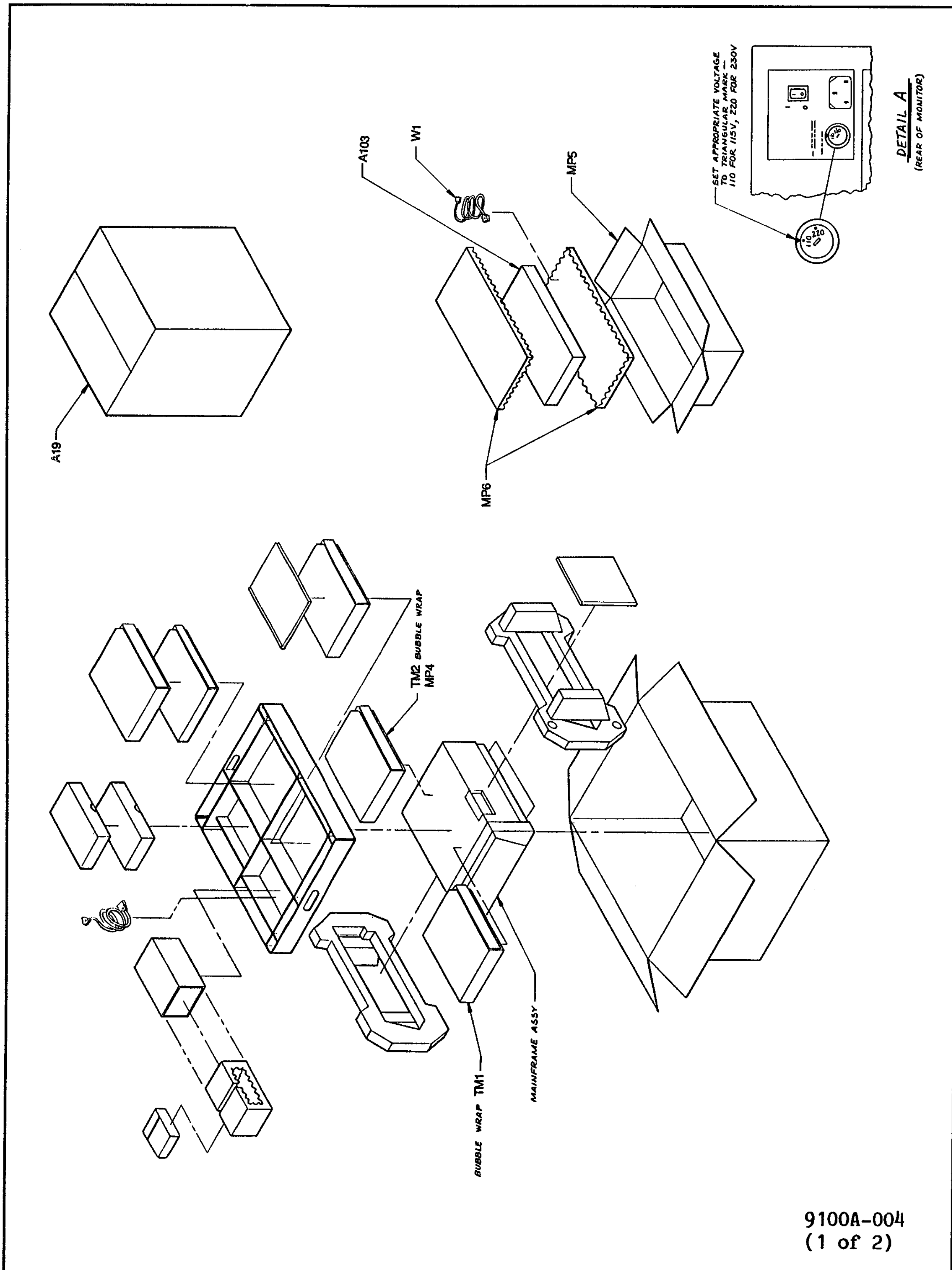
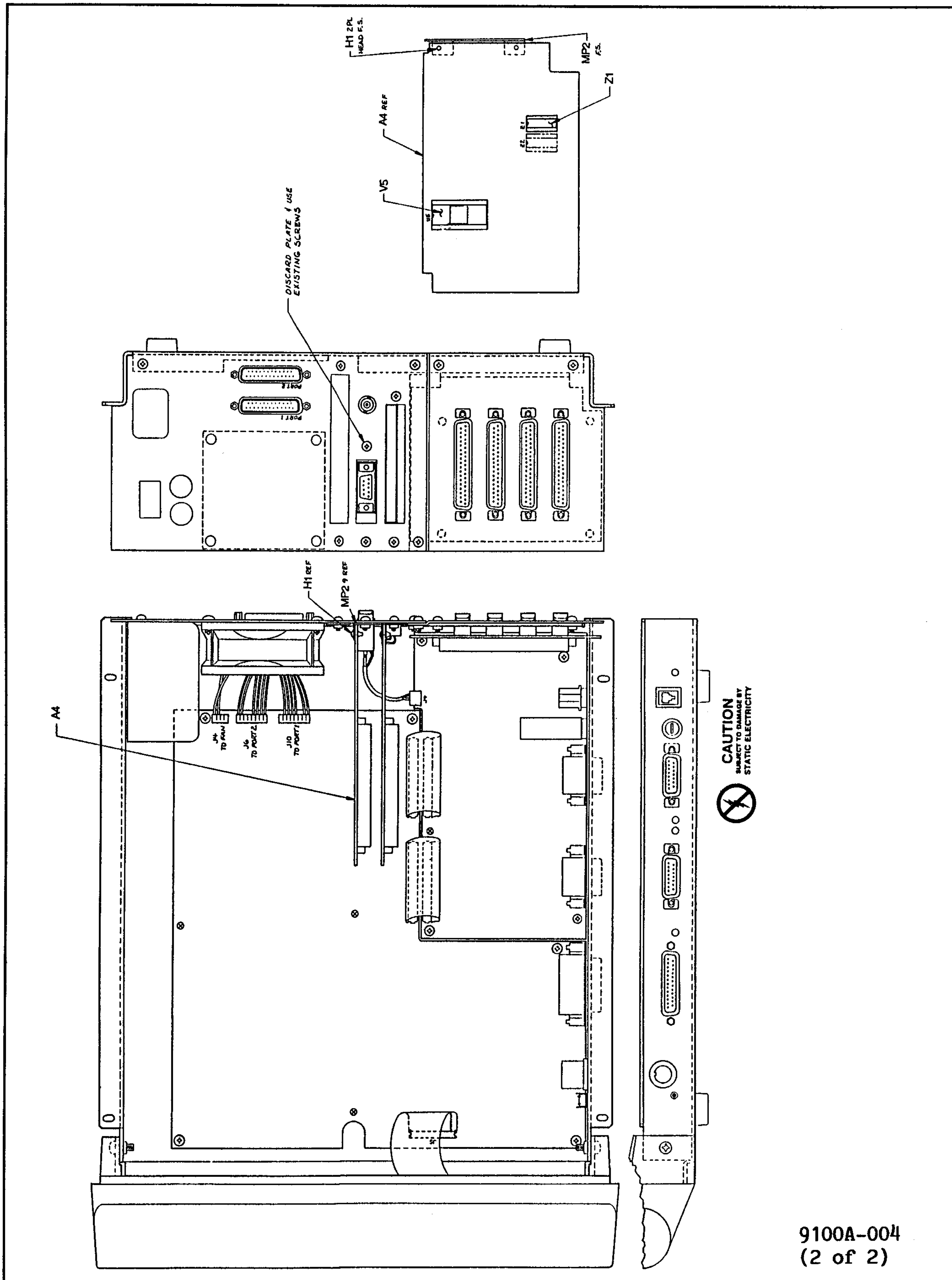


Figure 5-14. Option -004 Programmer's Station, Mono



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(2 of 2)

Figure 5-14. Option -004 Programmer's Station, Mono (cont.)

Table 5-21. Option -005 Programmer's Station, Color
(See Figure 5-15.)

REFERENCE DESIGNATOR -A>-NUMERICS---->		S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
A	4	*	VIDEO CONTROLLER PCA	768762	89536	768762	1		
A	103		KEYBOARD,ASYNC ASCII,1200 BAUD	757120	89536	757120	1		1
H	1		RIVET,POP,DOME,STL,0.250X0.720	187625	89536	187625	2		
MP	2		VIDEO CONNECTOR BRACKET	768648	89536	768648	1		
MP	3		PROGRAMMER SOFTWARE SYSTEM, SLEEVED		89536		1		2
MP	4		CARTON KEYBOARD, I/O	805804	89536	805804	1		
MP	5		CONVOLUTED FOAM, KEYBOARD-I/O	805820	89536	805820	1		
MP	6		PROGRAM COPY PROTECTION SHEET	847066	89536	847066	1		
TM	1		9100A TL/1 REFERENCE MANUAL	818047	89536	818047	1		
TM	2		9100A PROGRAMMERS MANUAL	813857	89536	813857	1		
U	5	*	PROGRAMMED 27128-150	818195	89536	818195	1		
Z	2		JUMPER,DIP,0.300CTR,PROGRAM,16 POS	783183	89536	783183	1		

An * in 'S' column indicates a static-sensitive part.

NOTES:

1 = See 9100A-013 option for replacement parts breakdown for A103.

2 = This software available only for 9100A's with Programmer's Station installed. Contact the factory if replacement is needed.

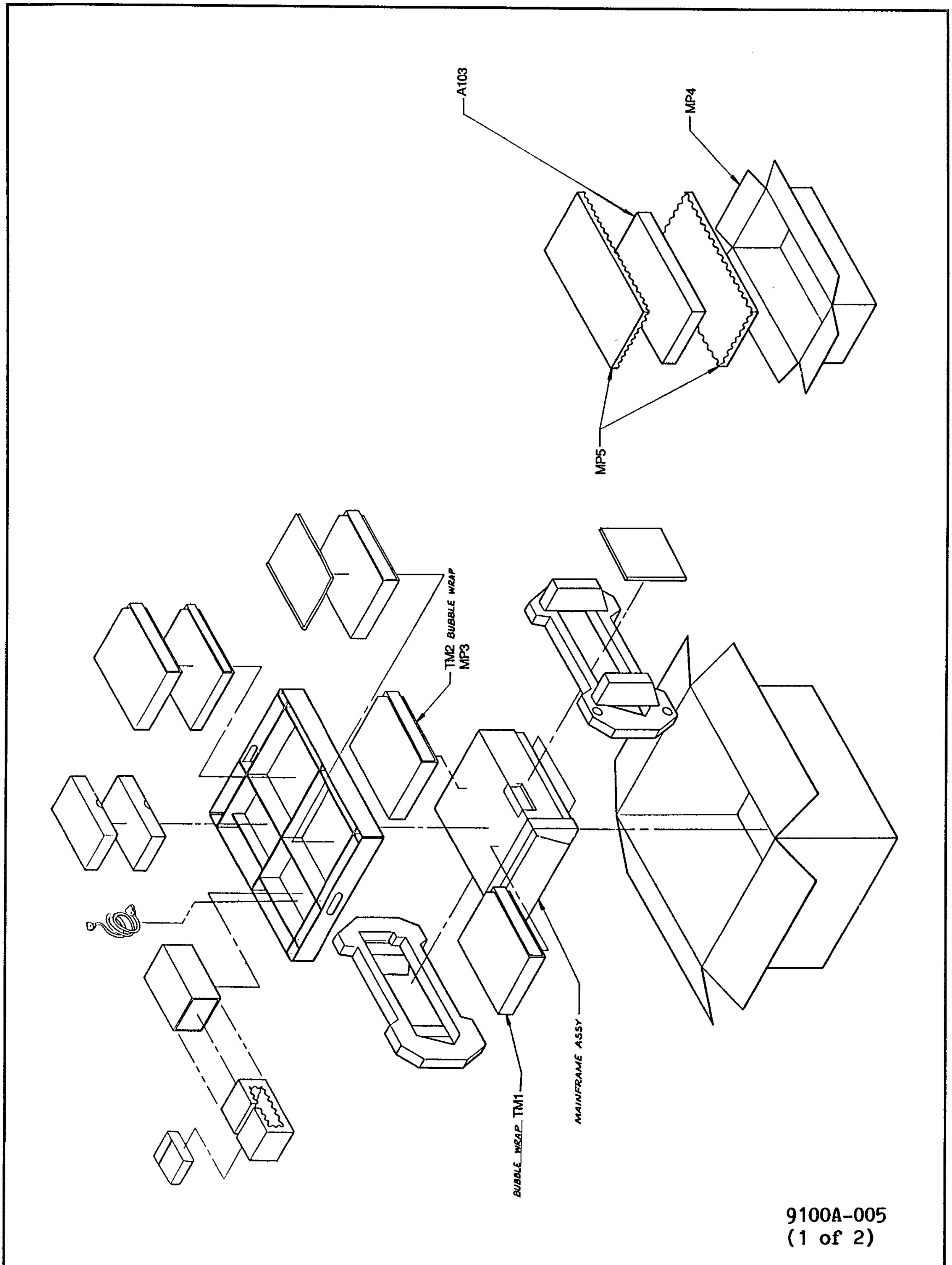

Figure 5-15. Option -005 Programmer's Station, Color

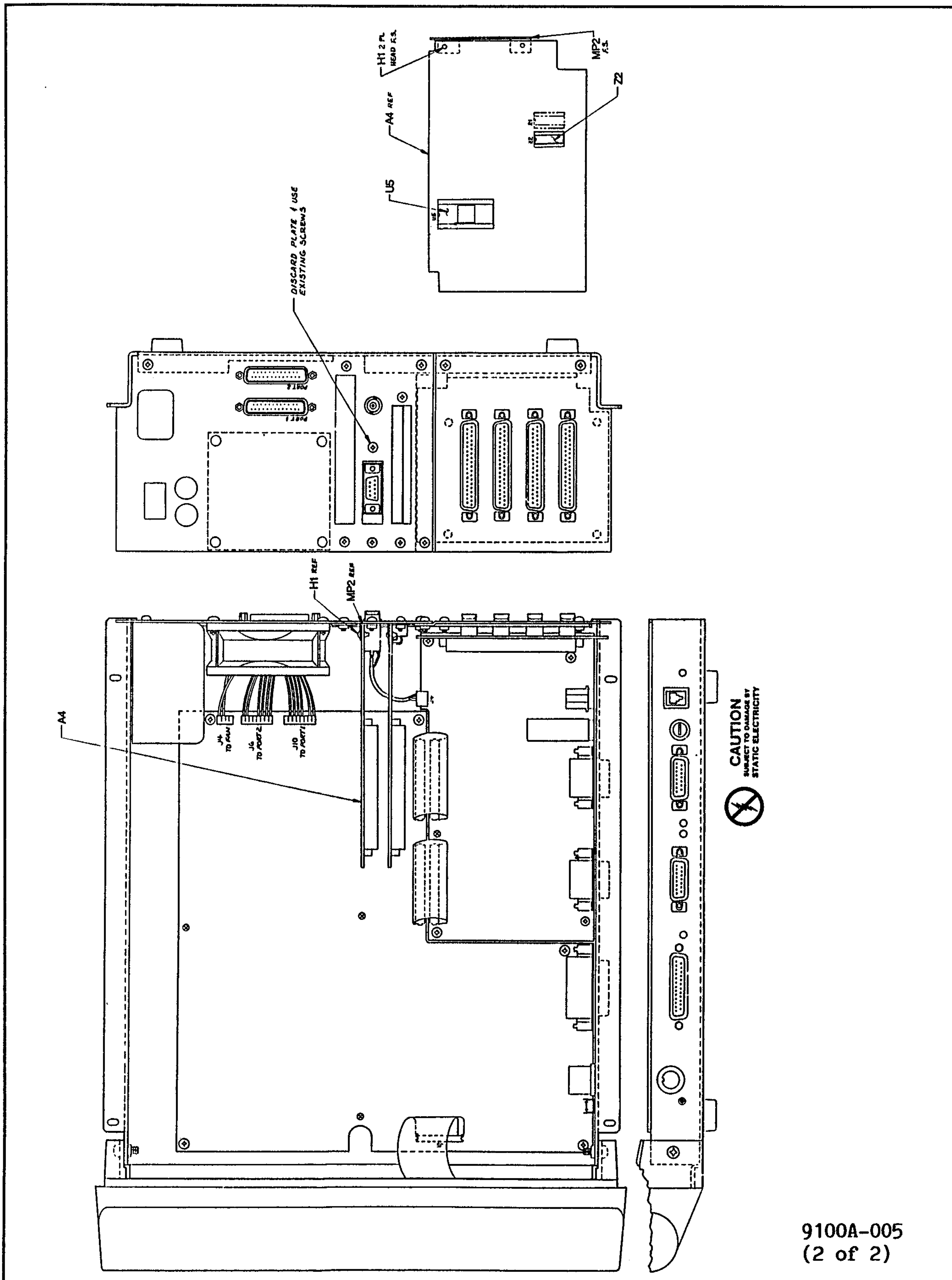

Figure 5-15. Option -005 Programmer's Station, Color (cont.)

Table 5-22. Option -008 Real Time Clock PCA
(See Figure 5-16.)

REFERENCE DESIGNATOR -A>	-NUMERICS---->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
B	1		BATTERY,LITHIUM,3.5V,0.75AH	782953	89536	782953	1	1	
C	1, 2		CAP,CER,15PF,+-2%,100V,COG	369074	89536	369074	2	1	
C	3, 10- 21		CAP,CER,0.01UF,+-20%,100V,X7R	407361	72982	8121-A100-W5R-103M	13		
CR	1	*	DIODE,SI,BV= 75.0V,IO=150MA,500 MW	203323	07910	1N4448	1	1	
H	1		SCREW,THD CUT,PHP,S.STL,4-24X3/8	183574	89536	183574	2		
H	2		RIVET,POP,DOME,AL,0.125X0.316	423616	89536	423616	2		
J	1		CONN,DIN41612,TYPE R,RT ANG,96 SCKT	747816	89536	747816	1		
MP	1		REAL TIME CLOCK/MFI BRACKET	802009	89536	802009	1		
Q	1	*	TRANSISTOR,SI,PNP,SMALL SIGNAL	195974	64713	2N3906	1	1	
Q	2	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	218396	04713	2N3904	1	1	
R	1, 2, 6,		RES,CF,10K,+-5%,0.25W	348839	80031	CR251-4-5P10K	6		
R	7, 9, 12			348839					
R	4		RES,CC,22M,+-5%,0.25W	221986	01121	CB2265	1		
R	5		RES,CF,51K,+-5%,0.25W	376434	80031	CR251-4-5P51K	1		
R	8, 10		RES,CF,200K,+-5%,0.25W	441485	80031	CR251-4-5P200K	2		
R	11		RES,CF,10,+-5%,0.25W	340075	80031	CR251-4-5P10E	1		
RN	5		RES,NET,SIP,10 PIN,9 RES,10K+-2%	414003	80031	95081002CL	1		
TP	1- 3		TERM,UNINSUL,WIRE FORM, TEST POINT	781237	89536	781237	3		
U	3	*	IC, PROGRAMMED PAL 20L8	818211	89536	818211	1	1	
U	9	*	IC,CMOS,PARALLEL I/O CALENDER & CLOCK	604181	12040	MM58167N	1	1	
U	10	*	IC,LSTTL,8BIT S-IN, P-OUT R-SHIFT RGS	408732	01295	SN74LS164N	1	1	
U	11	*	IC,CMOS,HEX INVERTERS	799924	89536	799924	1	1	
U	12	*	IC,CMOS,QUAD Z-INPUT NAND GATE	741280	89536	741280	1	1	
XU	3		SOCKET,IC,24 PIN	643999	89536	643999	1		
XU	9		SOCKET,IC,24 PIN	376236	91506	324-AG39D	1		
Y	1	*	CRYSTAL,32.768KHZ,+-0.003%	501817	89536	501817	1	1	

An * in 'S' column indicates a static-sensitive part.

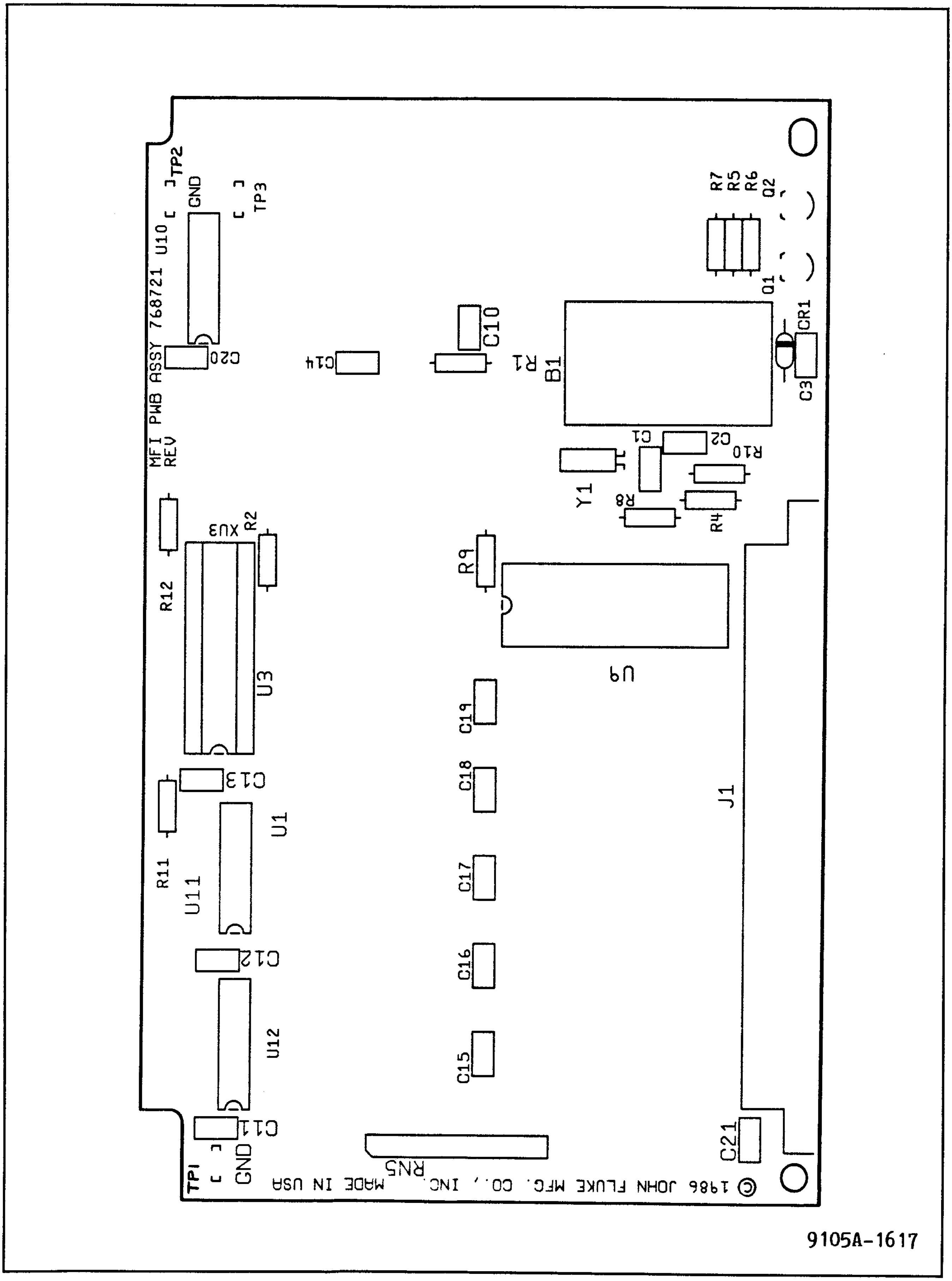

Figure 5-16. Option -008 Real-Time Clock PCA

Table 5-23. Option -009 Video, Monochrome
(See Figure 5-17.)

REFERENCE DESIGNATOR -A>-NUMERICS---->		S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
A	4	*	VIDEO CONTROLLER PCA	768762	89536	768762	1		
A	19		MONOCHROME MONITOR	826362	89536	826362	1		
H	1		RIVET,POP,DOME,AL,0.125X0.316	423616	89536	423616	2		
MP	2		VIDEO CONNECTOR BRACKET	768648	89536	768648	1		
MP	3		NAMEPLATE, SERIAL -REAR PANEL-	472795	89536	472795	1		
U	5	*	PROGRAMMED 27128-150	818195	89536	818195	1		
W	1		CABLE, MONITOR	787903	89536	787903	1		
Z	1		JUMPER,DIP,0.300CTR,PROGRAM,16 POS	783183	89536	783183	1		

An * in 'S' column indicates a static-sensitive part.

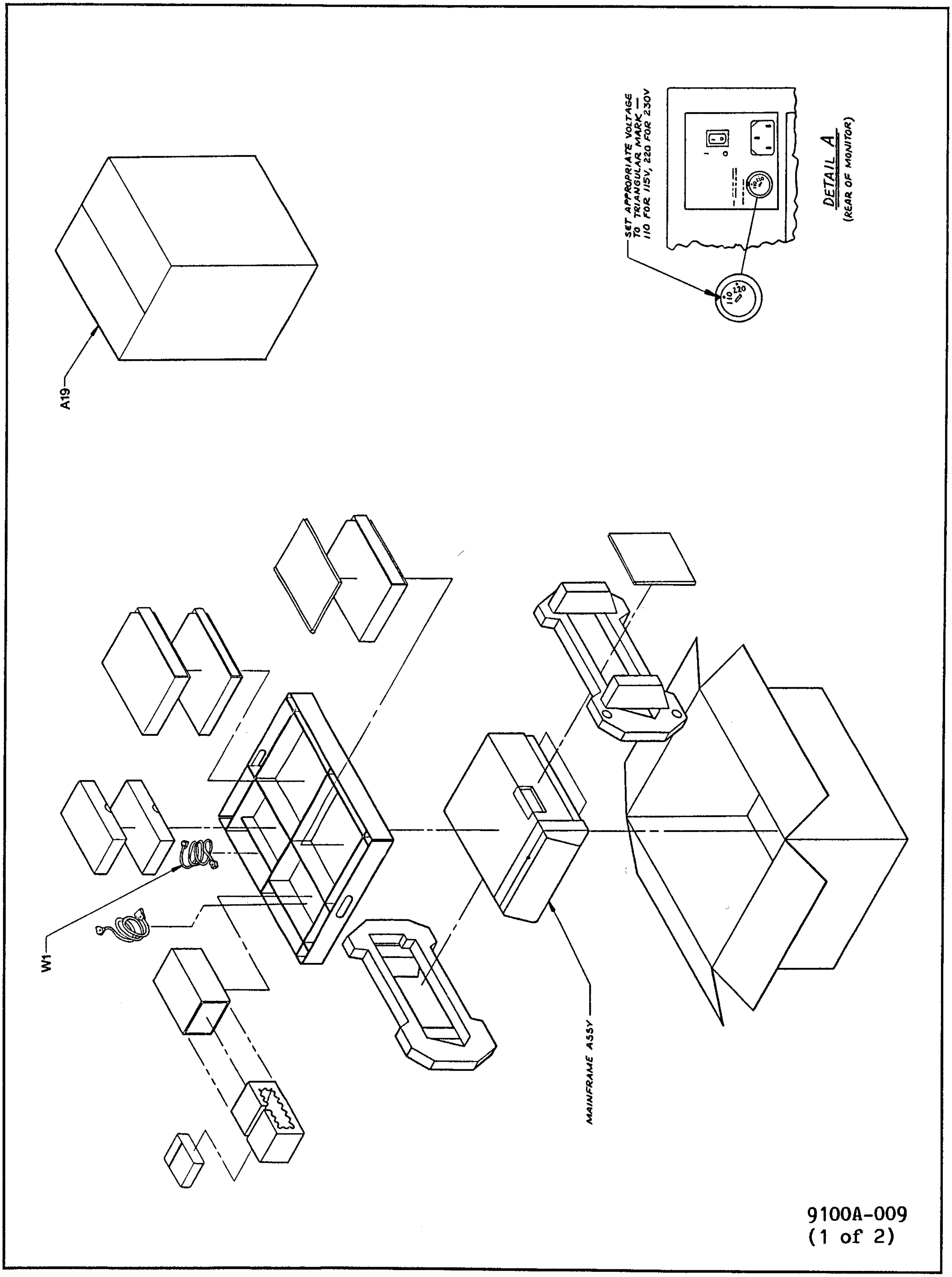

Figure 5-17. Option -009 Video, Monochrome

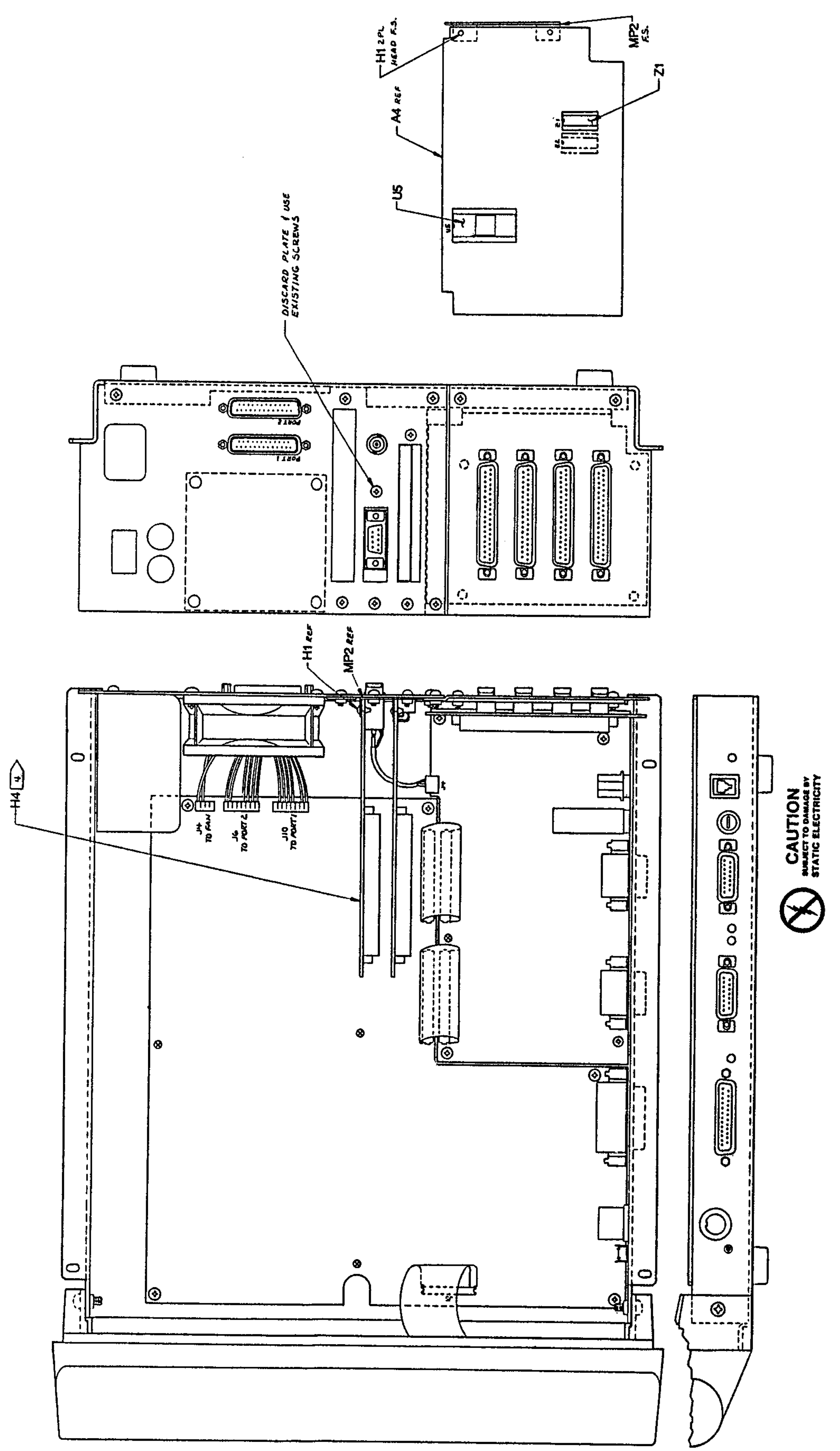

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Figure 5-17. Option -009 Video, Monochrome (cont.)

Table 5-24. Option -011 Video, Color
(See Figure 5-18.)

REFERENCE DESIGNATOR -A>-NUMERICS---->	S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-	TOT QTY-	R S -Q	N O T -E-
A 4	*	VIDEO CONTROLLER PCA	768762	89536	768762	1		
H 1		RIVET,POP,DOME,AL,0.125X0.316	423616	89536	423616	2		
MP 2		VIDEO CONNECTOR BRACKET	768648	89536	768648	1		
U 5	*	PROGRAMMED 27128-150	818195	89536	818195	1		
Z 2		JUMPER,DIP,0.300CTR,PROGRAM,16 POS	783183	89536	783183	1		

An * in 'S' column indicates a static-sensitive part.

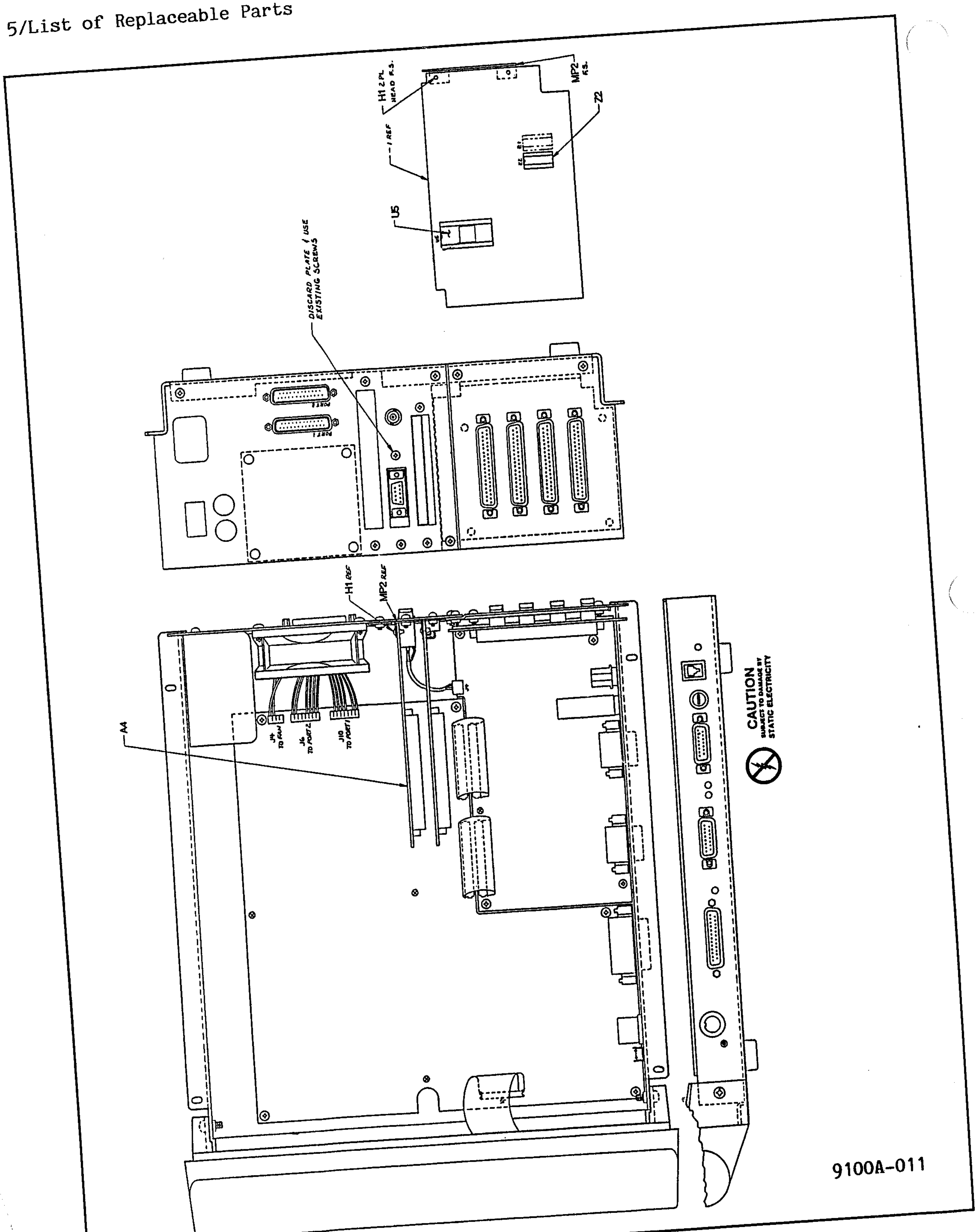

Figure 5-18. Option -011 Video, Color

Table 5-25. Option -013 Programmer's Keyboard

REFERENCE DESIGNATOR -A>-NUMERICS---->		S	---DESCRIPTION---	FLUKE STOCK --NO--	MFRS SPLY -CODE-	MANUFACTURERS PART NUMBER -OR GENERIC TYPE-----	TOT QTY-	R S -Q	N O T -E-
MP	1	*	ENCODER ASSEMBLY	783092	89536	783092	1		
MP	2	*	MEMBRANE SWITCH ASSEMBLY	783076	89536	783076	1		
MP	3		KEYCAP SET	783118	89536	783118	1		
MP	4		TOP CASE	783035	89536	783035	1		
MP	5		BASE	783084	89536	783084	1		
W	1		CABLE	783043	89536	783043	1		

An * in 'S' column indicates a static-sensitive part.

CONTENTS

Appendix 6A
Federal Supply Codes

Federal Supply Codes for Manufacturers (cont)

08261
Spectra Strip Corp.
Garden Grove, California

08530
Reliance Mica Corp.
Brooklyn, New York

08806
General Electric Co.
Miniature Lamp Products Dept
Cleveland, Ohio

08863
Nylomatic Corp.
Norrisville, Pennsylvania

08988
Use 53085
Skottie Electronics Inc.
Archbald, Pennsylvania

09214
G.E. Co. Semi-Conductor
Products Dept.
Power Semi-Conductor
Products OPN Sec.
Auburn, New York

09353
C and K Components
Watertown, Massachusetts

09423
Scientific Components, Inc.
Santa Barbara, California

09922
Burndy Corp.
Norwalk, Connecticut

09969
Dale Electronics Inc.
Yankton, S. Dakota

10059
Barker Engineering Corp.
Formerly Amerace, Amerace
ESNA Corp.
Kenilworth, New Jersey

11236
CTS of Berne
Berne, Indiana

11237
CTS Keene Inc.
Paso Robles, California

11358
CBS Electronic Div.
Columbia Broadcasting System
Newburyport, Minnesota

11403
Best Products Co.
Chicago, Illinois

11503
Keystone Columbia Inc.
Warren, Michigan

11532
Teledyne Relays
Hawthorne, California

11711
General Instrument Corp.
Rectifier Division
Hicksville, New York

11726
Qualidyne Corp.
Santa Clara, California

12014
Chicago Rivet & Machine Co.
Bellwood, Illinois

12040
National Semiconductor Corp.
Danburry, Connecticut

12060
Diodes, Inc.
Chatsworth, California

12136
Philadelphia Handle Co.
Camden, New Jersey

12300
Potter-Brumfield Div.
AMF Canada LTD.
Guelph, Ontario, Canada

12323
Presin Co., Inc.
Shelton, Connecticut

12327
Freeway Corp. formerly
Freeway Washer & Stamping Co.
Cleveland, Ohio

12443
The Budd Co. Polychem Products
Plastic Products Div.
Bridgeport, Pennsylvania

12615
U.S. Terminals Inc.
Cincinnati, Ohio

12617
Hamlin Inc.
Lake Mills, Wisconsin

12697
Clarostat Mfg. Co.
Dover, New Hampshire

12749
James Electronics
Chicago, Illinois

12856
Micrometals
Sierra Madre, California

12954
Dickson Electronics Corp.
Scottsdale, Arizona

12969
Unitrode Corp.
Watertown, Massachusetts

13103
Thermalloy Co., Inc.
Dallas, Texas

13327
Solitron Devices Inc.
Tappan, New York

13511
Amphenol Cadre Div.
Bunker-Ramo Corp.
Los Gatos, California

13606
Use 56289
Sprague Electric Co.
Transistor Div.
Concord, New Hampshire

13839
Replaced by 23732

14099
Semtech Corp.
Newbury Park, California

14140
Edison Electronic Div.
Mc Gray-Edison Co.
Manchester, New Hampshire

14193
Cal-R-Inc. formerly
California Resistor, Corp.
Santa Monica, California

14298
American Components, Inc.
an Insilco Co.
Conshohocken, Pennsylvania

14655
Cornell-Dubilier Electronics
Division of Federal Pacific
Electric Co. Govt. Control Dept.
Newark, New Jersey

14752
Electro Cube Inc.
San Gabriel, California

14869
Replaced by 96853

14936
General Instrument Corp.
Semi Conductor Products Group
Hicksville, New York

15636
Elec-Trol Inc.
Saugus, California

15801
Fenwal Electronics Inc.
Div. of Kidde Walter and Co., Inc.
Framingham, Massachusetts

15818
Teledyne Semiconductors,
formerly Amelco Semiconductor
Mountain View, California

15849
Litton Systems Inc. Useco Div.
formerly Useco Inc.
Van Nuys, California

15898
International Business
Machines Corp.
Essex Junction, Vermont

15909
Replaced by 14140

16258
Space-Lok Inc.
Burbank, California

16299
Corning Glass
Electronic Components Div.
Raleigh, North Carolina

16332
Replaced by 28478

16473
Cambridge Scientific Ind.
Div. of Chemed Corporation
Cambridge, Maryland

16742
Paramount Plastics
Fabricators, Inc.
Downey, California

16758
Delco Electronics
Div. of General Motors Corp.
Kokomo, Indiana

17001
Replaced by 71468

17069
Circuit Structures Lab.
Burbank, California

17338
High Pressure Eng. Co., Inc.
Oklahoma City, Oklahoma

17545
Atlantic Semiconductors, Inc.
Asbury Park, New Jersey

17856
Siliconix, Inc.
Santa Clara, California

17870
Replaced by 14140

18178
Vactec Inc.
Maryland Heights, Missouri

18324
Signetics Corp.
Sunnyvale, California

18612
Vishay Resistor Products Div.
Vishay Intertechnology Inc.
Malvern, Pennsylvania

18736
Voltronics Corp.
Hanover, New Jersey

18927
GTE Sylvania Inc.
Precision Material Group
Parts Division
Titusville, Pennsylvania

19451
Perine Machinery & Supply Co.
Seattle, Washington

19701
Electro-Midland Corp.
Mepco-Electra Inc.
Mineral Wells, Texas

20584
Enochs Mfg. Inc.
Indianapolis, Indiana

Federal Supply Codes for Manufacturers (cont)

20891
Self-Organizing Systems, Inc.
Dallas, Texas

21604
Bucheye Stamping Co.
Columbus, Ohio

21845
Solitron Devices Inc.
Transistor Division
Riveria Beach, Florida

22767
ITT Semiconductors
Palo Alto, California

23050
Product Comp. Corp.
Mount Vernon, New York

23732
Tracor Inc.
Rockville, Maryland

23880
Stanford Applied Engrng.
Santa Clara, California

23936
Pamotor Div., Wm. J. Purdy Co.
Burlingame, California

24248
Replaced by 94222

24355
Analog Devices Inc.
Norwood, Massachusetts

24655
General Radio
Concord, Massachusetts

24759
Lenox Fugle Electronics Inc.
South Plainfield, New Jersey

25088
Siemen Corp.
Isilen, New Jersey

25403
Amperex Electronic Corp.
Semiconductor &
Micro-Circuits Div.
Slatersville, Rhode Island

27014
National Semiconductor Corp.
Santa Clara, California

27264
Molex Products
Downers Grove, Illinois

28213
Minnesota Mining & Mfg. Co.
Consumer Products Div.
St. Paul, Minnesota

28425
Serv-/-Link formerly
Bohannan Industries
Fort Worth, Texas

28478
Deltrol Controls Div.
Deltrol Corporation
Milwaukee, Wisconsin

28480
Hewlett Packard Co.
Corporate HQ
Palo Alto, California

28520
Heyman Mfg. Co.
Kenilworth, New Jersey

29083
Monsanto, Co., Inc.
Santa Clara, California

29604
Stackpole Components Co.
Raleigh, North Carolina

30148
AB Enterprise Inc.
Ahoskie, North Carolina

30323
Illinois Tool Works, Inc.
Chicago, Illinois

31091
Optimax Inc.
Colmar, Pennsylvania

32539
Mura Corp.
Great Neck, New York

32767
Griffith Plastic Corp.
Burlingame, California

32879
Advanced Mechanical
Components
Northridge, California

32897
Erie Technological Products, Inc.
Frequency Control Div.
Carlisle, Pennsylvania

32997
Bourns Inc.
Trimpot Products Division
Riverside, California

33173
General Electric Co.
Products Dept.
Owensboro, Kentucky

34333
Silicon General
Westminister, California

34335
Advanced Micro Devices
Sunnyvale, California

34802
Electromotive Inc.
Kenilworth, New Jersey

37942
P.R. Mallory & Co., Inc.
Indianapolis, Indiana

42498
National Radio
Melrose, Massachusetts

43543
Nytronics Inc.
Transformer Co. Div.
Geneva, New York

44655
Ohmite Mfg. Co.
Skokie, Illinois

49671
RCA Corp.
New York, New York

49956
Raytheon Company
Lexington, Massachusetts

50088
Mostek Corp.
Carrollton, Texas

50579
Litronix Inc.
Cupertino, California

51605
Scientific Components Inc.
Linden, New Jersey

53021
Sangamo Electric Co.
Springfield, Illinois

54294
Cutler-Hammer Inc. formerly
Shallcross, A Cutter-Hammer Co.
Selma, North Carolina

55026
Simpson Electric Co.
Div. of Am. Gage and Mach. Co.
Elgin, Illinois

56289
Sprague Electric Co.
North Adams, Massachusetts

58474
Superior Electric Co.
Bristol, Connecticut

60399
Torin Corp. formerly
Torrington Mfg. Co.
Torrington, Connecticut

63743
Ward Leonard Electric Co., Inc.
Mount Vernon, New York

64834
West Mfg. Co.
San Francisco, California

65092
Weston Instruments Inc.
Newark, New Jersey

66150
Winslow Tele-Tronics Inc.
Eaton Town, New Jersey

70485
Atlantic India Rubber Works
Chicago, Illinois

70563
Amperite Company
Union City, New Jersey

70903
Belden Corp.
Geneva, Illinois

71002
Birnback Radio Co., Inc.
Freeport, New York

71400
Bussmann Mfg.
Div. of McGraw-Edison Co.
Saint Louis, Missouri

71450
CTS Corp.
Elkhart, Indiana

71468
ITT Cannon Electric Inc.
Santa Ana, California

71482
Clare, C.P. & Co.
Chicago, Illinois

71590
Centrelab Electronics
Div. of Globe Union Inc.
Milwaukee, Wisconsin

71707
Coto Coil Co., Inc.
Providence, Rhode Island

71744
Chicago Miniature Lamp Works
Chicago, Illinois

71785
TRW Electronics Components
Cinch Connector Operations Div.
Elk Grove Village
Chicago, Illinois

72005
Wilber B. Driver Co.
Newark, New Jersey

72092
Replaced by 06980

72136
Electro Motive Mfg. Co.
Williamantic, Connecticut

72259
Nytronics Inc.
Pelham Manor, New Jersey

72619
Dialight Div.
Amperex Electronic Corp.
Brooklyn, New York

72653
G.C. Electronics
Div. of Hydrometals, Inc.
Brooklyn, New York

72665
Replaced by 90303

72794
Dzus Fastener Co., Inc.
West Islip, New York

72928
Gulton Ind. Inc.
Gudeman Div.
Chicago, Illinois

Federal Supply Codes for Manufacturers (cont)

72982
Erie Tech. Products Inc.
Erie, Pennsylvania

73138
Bechman Instrument Inc.
Helipot Division
Fullerton, California

73293
Hughes Aircraft Co.
Electron Dynamics Div.
Torrance, California

73445
Amperex Electronic Corp.
Hicksville, New York

73559
Carling Electric Inc.
West Hartford, Connecticut

73586
Circle F Industries
Trenton, New Jersey

73734
Federal Screw Products, Inc.
Chicago, Illinois

73743
Fischer Special Mfg. Co.
Cincinnati, Ohio

73899
JFD Electronics Co.
Components Corp.
Brooklyn, New York

73949
Guardian Electric Mfg. Co.
Chicago, Illinois

74199
Quan Nichols Co.
Chicago, Illinois

74217
Radio Switch Corp.
Marlboro, New Jersey

74276
Signalite Div.
General Instrument Corp.
Neptune, New Jersey

74306
Piezo Crystal Co.
Carlisle, Pennsylvania

74542
Hoyt Elect. Instr. Works
Penacook, New Hampshire

74970
Johnson E.F., Co.
Waseca, Minnesota

75042
TRW Electronics Components
IRC Fixed Resistors
Philadelphia, Pennsylvania

75376
Kurz-Kasch Inc.
Dayton, Ohio

75378
CTS Knights Inc.
Sandwich, Illinois

75382
Kulka Electric Corp.
Mount Vernon, New York

75915
Littlefuse Inc.
Des Plaines, Illinois

76854
Oak Industries Inc.
Switch Div.
Crystal Lake, Illinois

77342
AMF Inc.
Potter & Brumfield Div.
Princeton, Indiana

77638
General Instrument Corp.
Rectifier Division
Brooklyn, New York

77969
Rubbercraft Corp. of CA. LTD.
Torrance, California

78189
Shakeproof
Div. of Illinois Tool Works Inc.
Elgin, Illinois

78277
Sigma Instruments, Inc.
South Braintree, Massachusetts

78488
Stackpole Carbon Co.
Saint Marys, Pennsylvania

78553
Eaton Corp. Engineered
Fastener Div.
Tinnerman Plant
Cleveland, Ohio

79136
Waldes Kohinoor Inc.
Long Island City, New York

79497
Western Rubber Company
Goshen, Indiana

79963
Zierick Mfg. Corp.
Mt. Kisko, New York

80031
Electro-Midland Corp.
Mepco Div.
A North American Phillips Co.
Norristown, New Jersey

80145
LFE Corp., Process Control Div.
formerly API Instrument Co.
Chesterland, Ohio

80183
Use 56289
Sprague Products
North Adams, Massachusetts

80294
Bourns Inc., Instrument Div.
Riverside, California

80583
Hammarlund Mfg. Co., Inc.
Red Bank, New Jersey

80640
Arnold Stevens, Inc.
South Boston, Massachusetts

81073
Grayhill, Inc.
La Grange, Illinois

81312
Winchester Electronics
Div. of Litton Industries Inc.
Oakville, Connecticut

81483
Therm-O-Disc Inc.
Mansfield, Ohio

81483
International Rectifier Corp.
Los Angeles, California

81590
Korry Mfg. Co.
Seattle, Washington

81741
Chicago Lock Co.
Chicago, Illinois

82305
Palmer Electronics Corp.
South Gate, California

82389
Switchcraft Inc.
Chicago, Illinois

82415
North American Phillips
Controls Corp.
Frederick, Maryland

82872
Roanwell Corp.
New York, New York

82877
Rotron Inc.
Woodstock, New York

82879
ITT Royal Electric Div.
Pawtucket, Rhode Island

83003
Varo Inc.
Garland, Texas

83058
The Carr Co., United Can Div.
of TRW
Cambridge, Massachusetts

83298
Bendix Corp.
Electric Power Div.
Eatontown, New Jersey

83330
Herman H. Smith, Inc.
Brooklyn, New York

83478
Rubbercraft Corp.
of America, Inc.
West Haven, Connecticut

83594
Burroughs Corp.
Electronic Components Div.
Plainfield, New Jersey

83740
Union Carbide Corp.
Battery Products Div.
formerly Consumer Products Div.
New York, New York

84171
Arco Electronics
Great Neck, New York

84411
TRW Electronic Components
TRW Capacitors
Ogallala, Nebraska

84613
Fuse Indicator Corp.
Rockville, Maryland

84682
Essex International Inc.
Industrial Wire Div.
Peabody, Massachusetts

86577
Precision Metal Products
of Malden Inc.
Stoneham, Massachusetts

86684
Radio Corp. of America
Electronic Components Div.
Harrison, New Jersey

86928
Seastrom Mfg. Co., Inc.
Glendale, California

87034
Illuminated Products Inc.
Subsidiary of Oak Industries Inc.
Anahiem, California

88219
Gould Inc.
Industrial Div.
Trenton, New Jersey

88245
Litton Systems Inc.
Useco Div.
Van Nuys, California

88419
Cornell-Dubilier Electronic Div.
Federal Pacific Co.
Fuquay-Varian, North Carolina

88486
Plastic Wire & Cable
Jewitt City, Connecticut

88690
Replaced by 04217

89536
John Fluke Mfg. Co., Inc.
Seattle, Washington

89730
G.E. Co., Newark Lamp Works
Newark, New Jersey

Federal Supply Codes for Manufacturers (cont)

90201
Mallory Capacitor Co.
Div. of P.R. Mallory Co., Inc.
Indianapolis, Indiana

90211
Use 56365
Square D Co.
Chicago, Illinois

90215
Best Stamp & Mfg. Co.
Kansas City, Missouri

90303
Mallory Battery Co.
Div. of Mallory Co., Inc.
Tarrytown, New York

91094
Essex International Inc.
Suglex/IWP Div.
Newmarket, New Hampshire

91293
Johanson Mfg. Co.
Boonton, New Jersey

91407
Replaced by 58474

91502
Associated Machine
Santa Clara, California

91506
Augat Inc.
Attleboro, Massachusetts

91637
Dale Electronics Inc.
Columbus, Nebraska

91662
Elco Corp.
Willow Grove, Pennsylvania

91737
Use 71468
Gremar Mfg. Co., Inc.
ITT Cannon/Gremar
Santa Ana, California

91802
Industrial Devices, Inc.
Edgewater, New Jersey

91833
Keystone Electronics Corp.
New York, New York

91836
King's Electronics Co., Inc.
Tuckahoe, New York

91929
Honeywell Inc.
Micro Switch Div.
Freeport, Illinois

91934
Miller Electric Co., Inc.
Div. of Aunet
Woonsocket, Rhode Island

92194
Alpha Wire Corp.
Elizabeth, New Jersey

93332
Sylvania Electric Products
Semiconductor Products Div.
Woburn, Massachusetts

94145
Replaced by 49956

94154
Use 94988
Wagner Electric Corp.
Tung-Sol Div.
Newark, New Jersey

94222
Southco Inc. formerly
South Chester Corp.
Lester, Pennsylvania

95146
Alco Electronic Products Inc.
Lawrence, Massachusetts

95263
Leecraft Mfg. Co.
Long Island City, New York

95264
Replaced by 98278

95275
Vitramon Inc.
Bridgeport, Connecticut

95303
RCA Corp.
Receiving Tube Div.
Cincinnati, Ohio

95348
Gordo's Corp.
Bloomfield, New Jersey

95354
Methode Mfg. Corp.
Rolling Meadows, Illinois

95712
Bendix Corp.
Electrical Components Div.
Microwave Devices Plant
Franklin, Indiana

95987
Weckesser Co. Inc.
Chicago, Illinois

96733
San Fernando Electric Mfg. Co.
San Fernando, California

96853
Gulton Industries Inc.
Measurement and Controls Div.
formerly Rustrak Instruments Co.
Manchester, New Hampshire

96881
Thomson Industries, Inc.
Manhasset, New York

97540
Master Mobile Mounts, Div. of
Whitehall Electronics Corp.
Ft. Meyers, Florida

97913
Industrial Electronic
Hardware Corp.
New York, New York

97945
Penwalt Corp.
SS White Industrial Products Div.
Piscataway, New Jersey

97966
Replaced by 11358

98094
Replaced by 49956

98159
Rubber-Teck, Inc.
Gardena, California

98278
Malco A Microdot Co., Inc.
Connector & Cable Div.
Pasadena, California

98291
Sealectro Corp.
Mamaroneck, New York

98388
Royal Industries
Products Div.
San Diego, California

98743
Replaced by 12749

98925
Replaced by 14433

99120
Plastic Capacitors, Inc.
Chicago, Illinois

99217
Bell Industries Elect.
Comp. Div.
formerly Southern Elect. Div.
Burbank, California

99392
STM
Oakland, California

99515
ITT Jennings Monrovia Plant
Div. of ITT Jennings formerly
Marshall Industries Capacitor Div.
Monrovia, California

99779
Use 29587
Bunker-Ramo Corp.
Barnes Div.
Landsdowne, Pennsylvania

99800
American Precision Industries Inc.
Delevan Division
East Aurora, New York

99942
Centrelab Semiconductor
Centrelab Electronics Div. of
Globe-Union Inc.
El Monte, California

Toyo Electronics
(R-Ohm Corp.)
Irvine, California

National Connector
Minneapolis, Minnesota

Appendix 6B
Fluke Sales and Service Centers

U.S. SALES AREAS for all Fluke products

Alabama

Huntsville
4920 Corporate Drive
Suite J
Huntsville, AL 35805-6202
(205) 837-0581

Arizona

Tempe
2211 S. 48th Street
Suite B
Tempe, AZ 85282
(602) 438-8314

Tucson
(602) 790-9881

California

Burbank
2020 N. Lincoln Street
Burbank, CA 91504
(213) 849-7181

Northern
2300 Walsh Ave., Bldg. K
Santa Clara, CA 95051
(408) 727-0513

San Diego
(619) 292-7657

Southern
P.O. Box 19676
Irvine, CA 92713-9676
16969 Von Karman
Suite 100
Irvine, CA 92714
(714) 863-9031

Colorado

Denver
14180 E. Evans Ave.
Aurora, CO 80014
(303) 695-1000

Connecticut

Hartford
Glen Lochen East
41-C New London Turnpike
Glastonbury, CT 06033
(203) 659-3541

Florida

Clearwater
(813) 799-0087

Miami
(305) 462-1380

Orlando
940 N. Fern Creek Ave.
Orlando, FL 32803
(305) 896-4881

Tampa
(813) 251-9211

Georgia

Atlanta
2700 Delk Road
Suite 150
Marietta, GA 30067
(404) 953-4747

Illinois

Chicago
1150 W. Euclid Avenue
Palatine, IL 60067
(312) 705-0500

Indiana

Indianapolis
8777 Purdue Road
Suite 101
Indianapolis, IN 46268
(317) 875-7870

Louisiana

New Orleans
(504) 455-0814

Massachusetts

Boston
Middlesex Technology Center
900 Middlesex Turnpike
Building 8
Billerica, MA 01821
(617) 663-2400

Maryland

Baltimore
(301) 792-7060

Rockville
5640 Fishers Lane
Rockville, MD 20852
(301) 770-1570

Michigan

Detroit
33031 Schoolcraft
Livonia, MI 48150
(313) 522-9140

Minnesota

Bloomington
1801 E. 79th St.
Suite 9
Bloomington, MN 55420
(612) 854-5526

Missouri

St. Louis
11756 Borman Drive
Suite 160
St. Louis, MO 63146
(314) 993-3805

North Carolina

Greensboro
1310 Beaman Place
Greensboro, NC 27408
(919) 273-1918

New Jersey

Paramus
P.O. Box 930
Paramus, NJ 07653-0930
West 75 Century Road
Paramus, NJ 07652
(201) 262-9550

New Mexico

Albuquerque
(505) 881-3550

New York

Rochester
4515 Culver Road
Rochester, NY 14622
(716) 323-1400

Ohio

Cleveland
Plaza South Three
Suite 402
7271 Engle Road
Middleburg Heights, OH 44130
(216) 234-4540

Oklahoma

Northeast
(405) 236-2977

Oregon

Portland
(503) 227-2042

Pennsylvania

Malvern
200 Lindenwood Drive
Malvern, PA 19355
(215) 647-9550

Pittsburgh
(412) 261-5171

Texas

Austin
(512) 459-3344

Dallas
1801 Royal Lane
Suite 307
Dallas, TX 75229
(214) 869-0311

El Paso
(915) 533-3508

Houston
(713) 240-5995

San Antonio
10417 Gulfdale
San Antonio, TX 78216
(512) 340-0498

Utah

Salt Lake City
(801) 268-9331

Washington

Seattle
5020 148th Ave. N.E.
Suite 110
Redmond, WA 98052
(206) 881-6966

Washington, DC

Washington, DC
(301) 770-1570

INTERNATIONAL SALES OFFICES

Algeria
Bureau de Liaison Philips
(For Philips products)
24 rue Bougainville
El Mouradia, Alger
Tel: 60 14 05
TLX: 62221

Antilles
Philips Antillana N.V.
(For Philips products)
Schottegatweg Oost 146
P.O.Box 3523
Willemstad, Curacao
Tel: 599-9-615277
TLX: 1047

Argentina
Coasin S.A.
(For Fluke products)
Virrey del Pino 4071DPTO E-65
1430 CAP FED
Buenos Aires, Argentina
Tel: (54) (1) 552-5248
TLX: (390) 22284

Philips Argentina S.A.
(For Philips products)
Casilla Correo 3479
Vedia 3892
1430 Buenos Aires
Tel: 54-1-5414106/5417141
TLX: 21359/21243

Australia
Elmeasco Instruments Pty, Ltd.
(For Fluke products)
P.O. Box 30
Concord, N.S.W. 2137
Australia
Tel: (61) (2) 736-2888
TLX: (790) AA25887
FAX: (61) 2-733663

Elmeasco Instruments Pty, Ltd.
(For Fluke products)
P.O. Box 623
12 Maroondah Highway
Ringwood, Victoria 3134
Australia
Tel: (61) (3) 879-2322
TLX: (790) AA30418
FAX: (61) 3-879-4310

Elmeasco Instruments Pty, Ltd.
(For Fluke products)
P.O. Box 274
Salisbury, Qld Australia 4107
Tel: (61) (7) 875-1444
TLX: (790) AA44062

Elmeasco Instruments Pty, Ltd.
(For Fluke products)
P.O. Box 154
Prospect, South Australia 5082
Tel: (61) (8) 344-9000

Elmeasco Instruments Pty, Ltd.
(For Fluke products)
32 Teddington Rd.
Victoria Park
Western Australia 6100
Tel: (61) 9-470-1855

Philips Scientific & Industrial Equipment Division
(For Philips products)
Centrecourt 25-27 Paul Street
North Ryde
Sydney N.S.W. 2113
Tel: 88 88 222

Austria
Walter Rekirsch Elektronische Gerate GmbH & Co.
(For Fluke products)
Vertrieb KG
Obachgasse 28
1220 Vienna, Austria
Tel: (43) (222) 253626
TLX: (847) 134759
FAX: (43) (222) 257275

Osterreichische Philips Industrie GmbH
(For Philips products)
Geschaftsbereich I & E
Marktbereich Test-und Meβgerate
A-1101 WIEN, Triester Straβe 64
Tel: (0222) 60101/1772 DW

Bahrain
Basma W.L.L.
(For Fluke products)
P.O. Box 5701
Manama, Bahrain
Tel: (973) 251-364
TLX: (955) 9003
FAX: (965) 245218

Bangladesh
Motherland Corporation
(For Fluke products)
24 Hatkhola Road, Tikatuli
Dacca-3, Bangladesh
Tel: 257249, TLX: (950) 642022

Philips Bangladesh Ltd.
(For Philips products)
P.O. Box 62, Ramna
16/17 Kawran Bazar C/A
DHAKA
Tel: 411976
TLX: 65668

Belgium
N.V. Philips Professional Systems S.A. Test and Measurement
Tweestationsstraat 80
Rue des Deux Gares
Brussel 1070 Bruxelles
Tel: 2-5256111

Bolivia
Coasin Bolivia S.R.L.
(For Fluke products)
Casilla 7295
La Paz, Bolivia
Tel: (591) (2) 40962
TLX: (336) 3233 COALAP BV

Brazil
ATP Hi-Tek Eletronica Ltda.
(For Fluke products)
Al. Amazonas 422, Alphaville
Barueri
CEP 06400, Sao Paulo, Brazil
Tel: (55) (11) 421-5477
TLX: (391) 1171413

Philips do Brasil Ltda.
(For Philips products)
Av. Eng. Luiz Carlos Berrini 3009
Caixa Postal 8681
04571 SAO PAULO S.P.
Tel: 55-11-2411611
TLX: (011) 32750

Brunei
Rank O'Connor's, Sdn Bhd
(For Fluke products)
No. 8 Block D,
Sufri Shophouse Complex
Mile 1 Jalan Tutong
Bandar Seri Begawan
Negara Brunei Darussalam
Tel: (673) (2) 23109 or 23557
TLX: (799) BU2265 RANKOC

Canada
Fluke Electronics Canada Inc.
400 Britannia Rd. East Unit #1
Mississauga, Ontario
L4Z 1X9 Canada
Tel: (416) 890-7600
FAX: (416) 890-6866

Fluke Electronics Canada Inc.
1690 Woodward Drive
Suite 216
Ottawa, Ontario
K2C 3R8 Canada
Tel: (613) 723-9453
FAX: (613) 723-9458

Fluke Electronics Canada Inc.
1255 Trans Canada Highway
Suite 130
Dorval, Quebec
H9P 2V4 Canada
Tel: (514) 685-0022
FAX: (514) 685-0039

Fluke Electronics Canada Inc.
101, 1144 - 29th Ave. N.E.
Calgary, Alberta
T2E 7P1 Canada
Tel: (403) 291-5215
FAX: (403) 291-5219

Chile
Intronica Chile, Ltda.
(For Fluke products)
Casilla 16228
Santiago 9, Chile
Tel: (56) 2-2321886
TLX: (332) 346351

Philips Chilena S.A. de Produc. Electr.
(For Philips products)
Avenida Santa Maria 0760
Casilla 2687
Santiago De Chile
Tel: 56-2-770038
TLX: 240239

China, Peoples Republic of
Fluke International Corp.
(For Fluke products)
P.O. Box C9090 M/S 206A
Everett, WA 98206 U.S.A.
Tel: (206) 356-5511
TLX: 185103 FLUKE UT
FAX: (206) 356-5116

Colombia
Sistemas E Instrumentacion, Ltda.
(For Fluke products)
Carrera 13, No. 37-43, Of. 401
Ap. Aereo 29583
Bogota DE, Colombia
Tel: (57) 232-4532
TLX: (396) 45787

Industrias Philips de Colombia S.A.
(For Philips products)
Apartado Aereo 4282
Calle 13 No. 51-39
Bogota
Tel: 57-1-2600600
TLX: Philcolon 44776

Cyprus
Chris Radiovision, Ltd.
(For Fluke products)
P.O. Box 1989
Nicosia, Cyprus
Tel: (357) (21) 66121
TLX: (826) 2395

Cyprus, Northern
Ucok Buroteknik
(For Fluke products)
2C & 2D Muftu Ziyai Street
Lefkosa, Northern Cyprus
Mersin 10, Turkey
Tel: (90) (741) 357-20-71777
TLX: (821) 57267

Denmark
Tage Olsen A/S
(For Fluke products)
Ballerup Byvej 222
2750 Ballerup
Denmark
Tel: (45) (2) 658111
TLX: (855) 35293
FAX: (45) 2-680 300

Philips A/S Test & Measurement
(For Philips products)
Prags Boulevard 80
DK-2300-Kobenhavn S
Tel: (01) 572222
TLX: 31201

Ecuador
Proteco Coasin Cia., Ltda.
(For Fluke products)
P.O. Box 228-A
Ave. 12 de Octubre 2285
y Orellana
Quito, Ecuador
Tel: (593) (2) 529684
TLX: (393) 22085

Philips Ecuador S.A.
(For Philips products)
Casilla 343
Paez 118 y Avenida Patria
Quito
Tel: 593-2-546100/546125
TLX: 2227 PHLPSQ ED

Proteco Coasin Cia., Ltda.
(For Fluke products)
P.O. Box 9733
Ave. Principal No. 204 y Calle Segunda
Urbanizacion Miraflores
Guayaquil, Ecuador
Tel: (593) (4) 387519

Egypt and Sudan
Electronic Engineering Liaison Office
(For Fluke products)
P.O. Box 2891 Horreya
11361 Heliopolis, Cairo
Egypt
Tel: (20) 2-695705
TLX: (927) 22782

Philips Egypt Liaison Office of Philips
(For Philips products)
Export B.V.
10, Abdel Rahman el Rafei Str.
P.O. Box 1687
Dokki, Cairo
Tel: 20-2-3490922
TLX: 22816 PHEGY UN

Ethiopia
(For Philips products)
Philips Ethiopia (Priv. Ltd. Co.)
Ras Abebe Areguay Avenue
P.O. Box 2565
Addis Ababa
Tel; 148300

Fiji
Awa New Zealand Ltd.
(For Fluke products)
37 Freestone Walu Bay Road
P.O. Box 858
Suva, Fiji
Tel: (679) 312079
TLX: (792) 2347
FAX: (679) 314379

Finland
Instrumentarium Elektroniikka
(For Fluke products)
P.O. Box 64
02631 Espoo 63
Finland
Tel: (358) (0) 5281
TLX: (857) 124426
FAX: (358) 0-502-1073

OY Philips AB
(For Philips products)
P.O. Box 11
02631 ESPOO
Tel. 0-5257225

France
M.B. Electronique S.A.
(For Fluke products)
606 Rue Fourney
P.O. Box 31
78530 BUC, France
Tel: (33) (1) 39568131
TLX: (842) 695414
FAX: (33) (1) 3956-53-44

S.A. Philips Industrielle et Commercials Division Science et Industrie
(For Philips products)
105 rue de Paris, BP 62
93002 BOBIGNY Cedex
Tel: (1) 49 42 80 80
TLX: 210290

Germany
Philips GmbH
(For Philips products)
Unternehmensbereich
Elektronik fur Wissenschaft
und Industria
Vertriebsbereich Testr and Meßtechnik
Miramstraße 87 Postfach 310320
D-3500 KASSEL
Tel: (0561) 5010, TLX: 997070

Bereich Fluke Produkts
Oskar-Messter-Strape 18
D-8045 Ismaning

Great Britain
Philips Test & Measurement
York Street
Cambridge CB1 2PX
Tel: (0223) 358866
TLX: 817331

Philips Test & Measurement
(For Fluke products)
Colonial Way
Watford WD2 4TT

Greece
Hellenic Scientific Representations Ltd.
(For Fluke products)
11 Vrassida Street
Athens 612, Greece
Tel: (30) (1) 7211140
TLX: (863) 219330

Philips S.A. Hellenique I&E Division
(For Philips products)
15, 25th March Street
GR-17778 TAVROS or
P.O. Box 3153 Athens
Tel: 30-1-4894911
TLX: 241566-241567

Hong Kong
Fluke Asia Ltd.
(For Fluke products)
Shun Tak Centre
Suite No. 1501
200 Connaught Road
Central, Hong Kong
Tel: (852) 5-482116
FAX: (852) 5-479863
TLX: (780) 87058 Fluke HX

Philips Hong Kong Ltd.
(For Philips products)
29/F Hopewell Centre
17 Kennedy Road
G.P.O. Box 2108
Hong Kong
Tel: 852-5-283298
TLX: 73660 PHILH HX

Schmidt & Co (H.K.), Ltd
(For Fluke products)
18th Floor, Great Eagle Centre
23 Harbour Road
Wanchai, Hong Kong
Tel: (852) (5) 8330-222
TLX: (780) 74766 or 76762
FAX: (852) 5-8918754

India
Hinditron Services Pvt., Ltd.
(For Fluke products)
69/A.L. Jagmohandas Marg
Bombay 400 006, India
Tel: (22) 8121316, (91) (22) 8125344
TLX: (953) 1175326

Hinditron Services Pvt., Ltd.
(For Fluke products)
8th Main Road
33/44A Raj Mahal Vilas Extension
Bangalore 560 080, India
Tel: (91) 812-363139, TLX: (953) 8452741

Hinditron Services Pvt. Ltd.
(For Fluke products)
5th Floor, "Castle House"
5/1A, Hungerford St.
Calcutta 700 017, India
Tel: (91) 33-432628, TLX (953) 21-4153

Hinditron Services Pvt. Ltd.
(For Fluke products)
204-5-6 Hemkunt Tower
98 Nehru Place
New Delhi, 110019, India
Tel: (91) 11-6410380, TLX: (953) 316458

Hinditron Services Pvt., Ltd.
(For Fluke products)
Emerald Complex 1-7-264
5th Floor
114 Sarojini Devi Rd.
Secunderabad 500 003, India
Tel: 842 821117, TLX: (953) 04256973

Pelco Electronics & Electricals Ltd.
(For Philips products)
Shivsagar Estate, Block 'A'
Dr. Annie Besant Road
P.O.B. 6598
Worli, Bombay 4000018
Tel: 4921500/4921513

Indonesia
P.T. Lamda Triguna
(For Fluke products)
Tel: (62) 21-8195365
TLX: (796) 45483 LOMAS I.A.
P.O. Box: 6/JATJG, Jakarta 13001

P.T. Daeng Brothers
(For Philips products)
Centre Point Building, 3rd Fl.
Jalan Gatot Subroto Kav. 35/36
P.O. Box 41 Tebet
Jakarta
Tel: 62-21-517900
TLX: 62798 PHDC IA

Iran
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Tel Aviv 61430
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Taipei
Tel: 752-7421

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(For Philips products)
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Necatiby Cad 92/3
Karakoy, Istanbul, Turkey
Tel: 441546

Turk Philips Ticaret A.S.
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Beykoglu Istanbul
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Philips Middle East b.v.
(For Philips products)
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Tel: 377000

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Tel: 47211

INTRODUCTION

As changes and improvements are made to the instrument, they are identified by incrementing the revision letter marked on the affected PCA.

These changes are documented on supplemental change/errata sheets which, when applicable, are inserted at the front of the manual. To identify the configuration of the PCAs used in your instrument, refer to the revision letter marked on each PCA.

Module Revision Information

Ref	Assembly Name	Fluke Part No.	Revision Level
A1	Main PCA	755520	C2
A2	Display IF PCA	767947	C1
A3	Keypad	755454	D
A4	Video Controller PCA	755553	C1
A5	Probe PCA	755561	E
A6	Clock Module PCA	755579	B
A7	I/O Module (Main) PCA	755587	C
A8	I/O Module (Top) PCA	768747	A2
A9	Probe I/O PCA	768788	G
A10	Multi-Function IF PCA	768721	A1
A11	I/O Connector PCA	767996	A
A16	512K RAM Module	809079	A
-008	Real-Time Clock PCA	768721	A1

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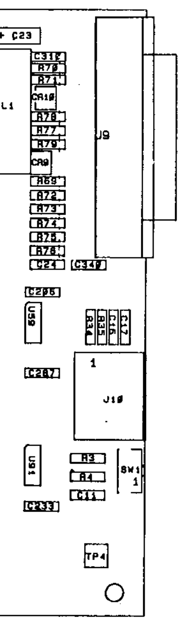
* A10 schematic also used with -008 Real-Time Clock PCA
** A12 schematic also used with A15 Flying Lead Module



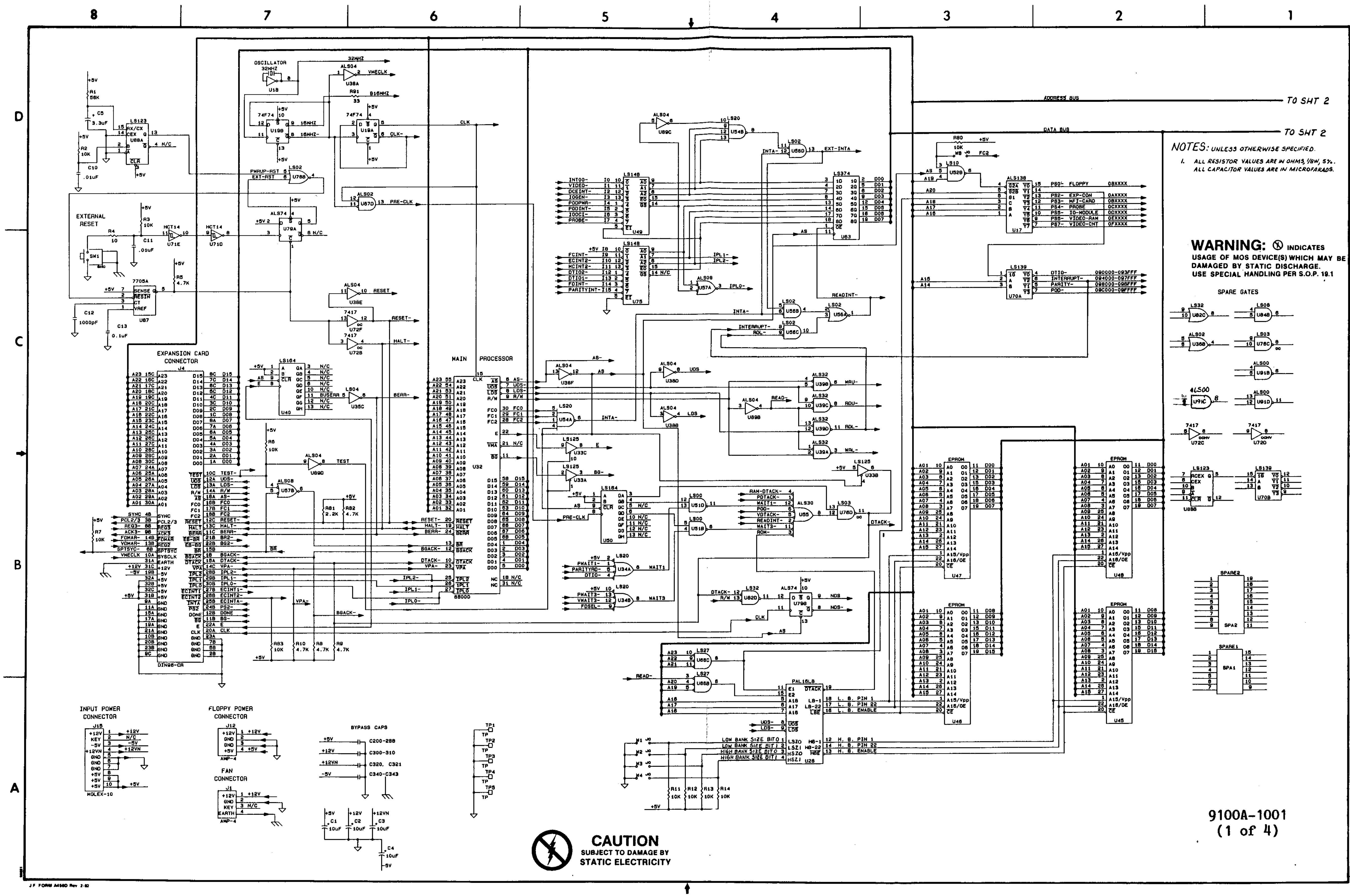
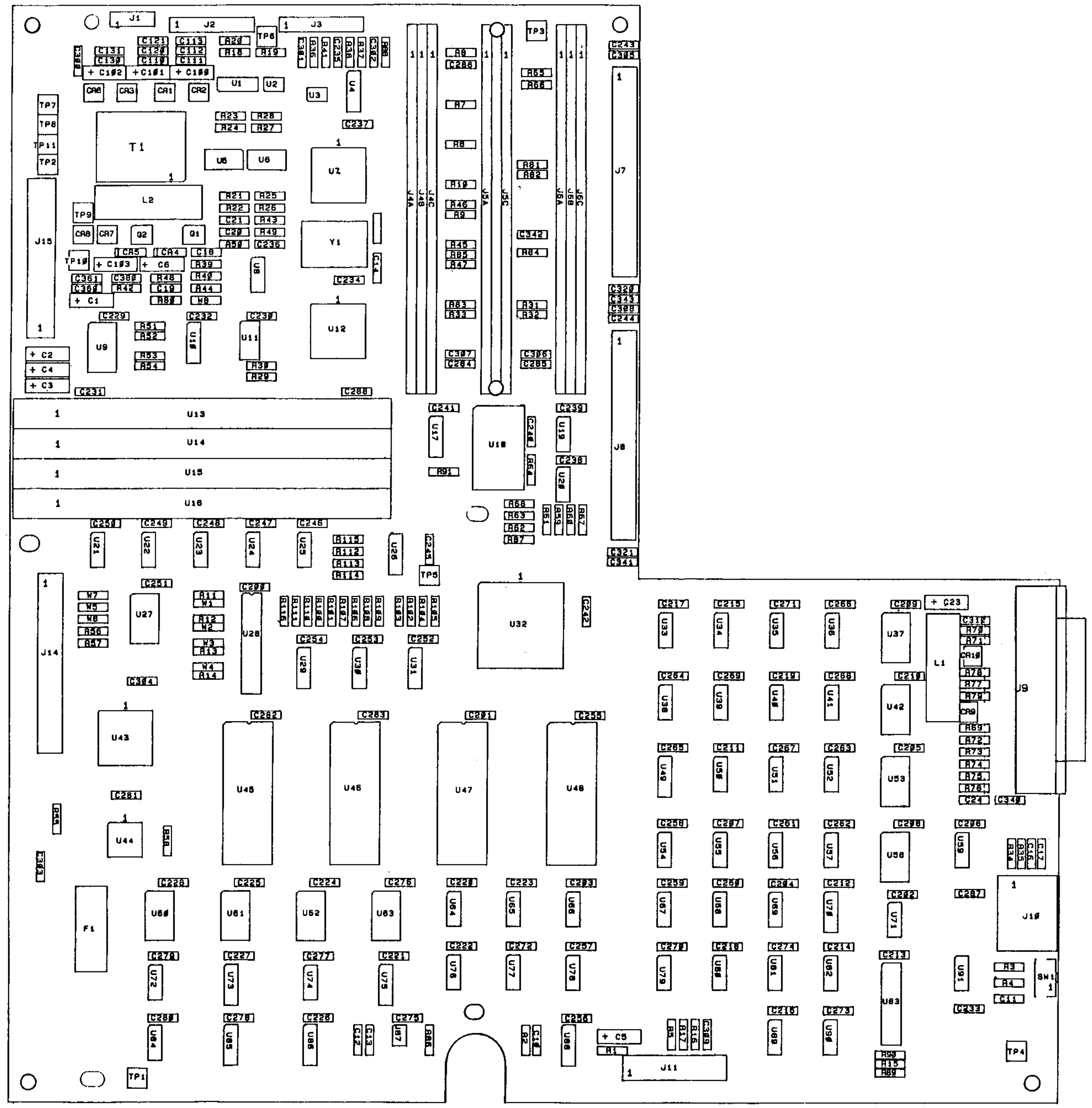


Figure 7-1. A1 Main PCA



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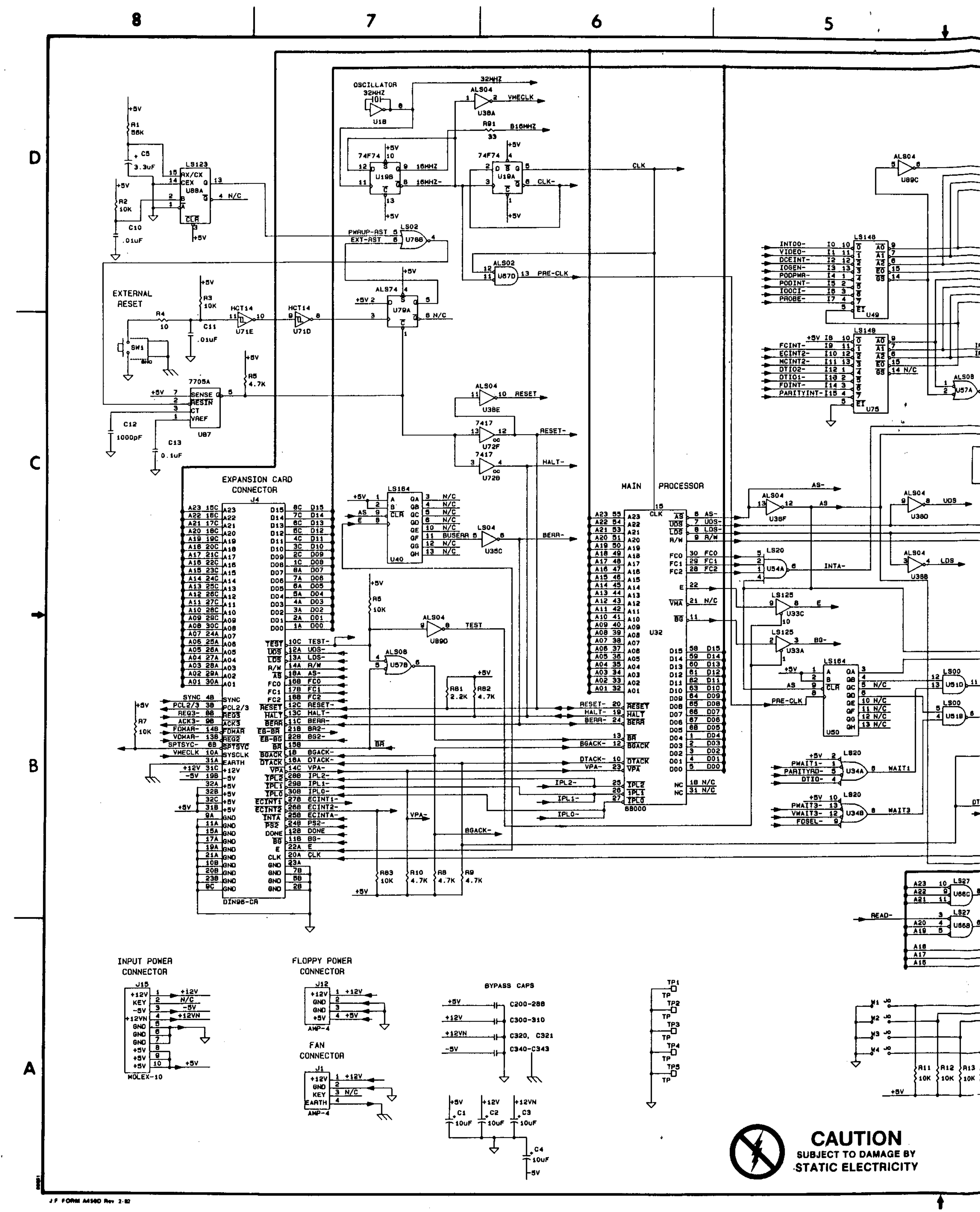

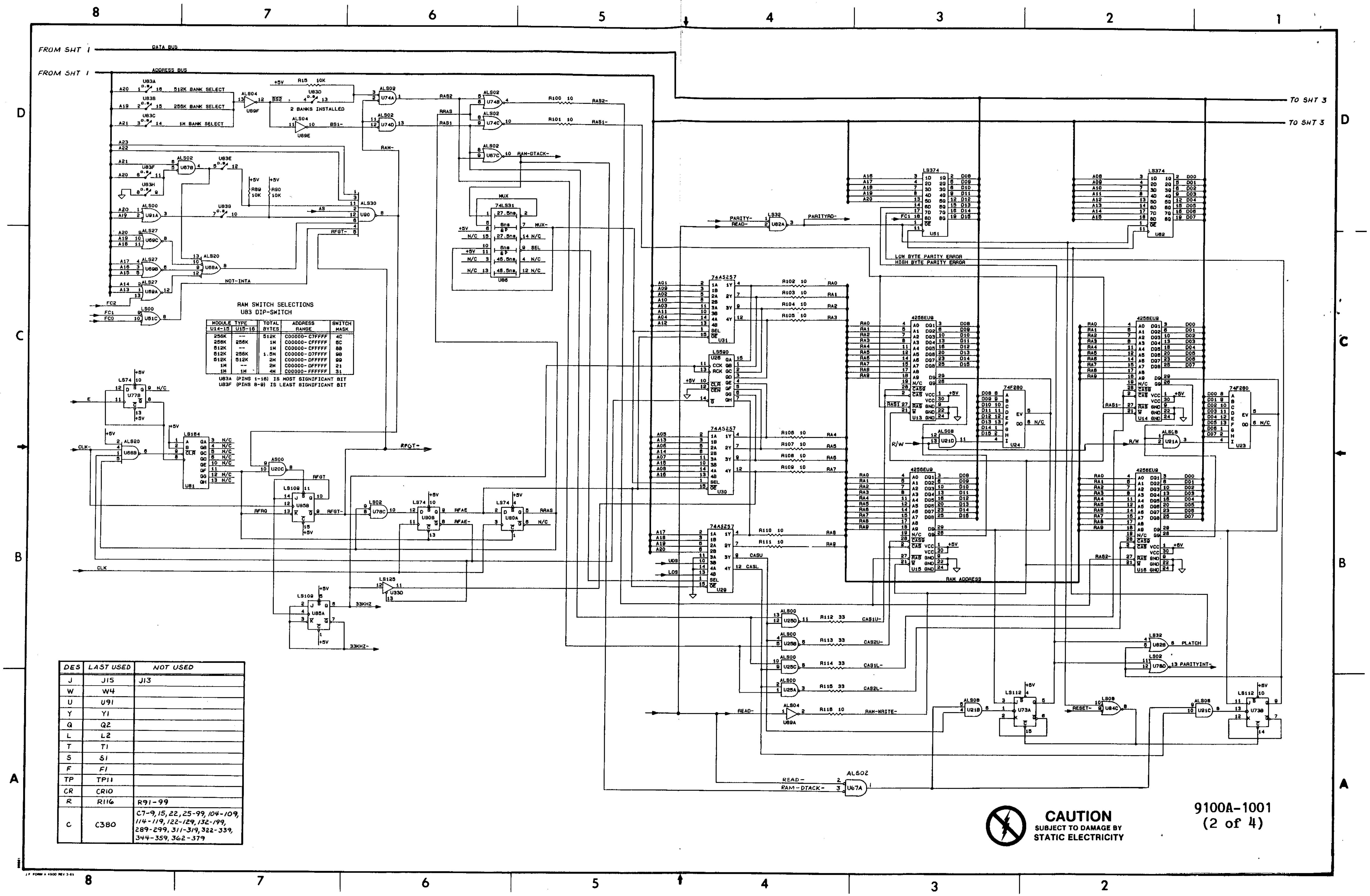

RAM SWITCH SELECTIONS
U83 DIP-SWITCH

MODULE TYPE U14-15	MODULE TYPE U15-16	TOTAL BYTES	ADDRESS RANGE	SWITCH MASK
256K	--	512K	C00000-C7FFFF	4C
256K	256K	1M	C00000-CFFFFF	5C
512K	--	1M	C00000-CFFFFF	88
512K	256K	1.5M	C00000-D7FFFF	98
512K	512K	2M	C00000-DFFFFF	99
1M	--	2M	C00000-DFFFFF	21
1M	1M	4M	C00000-FFFFFF	31

U83A (PINS 1-16) IS MOST SIGNIFICANT BIT
U83F (PINS 8-9) IS LEAST SIGNIFICANT BIT

DES	LAST USED	NOT USED
J	J15	J13
W	W4	
U	U91	
Y	Y1	
Q	Q2	
L	L2	
T	T1	
S	S1	
F	F1	
TP	TP11	
CR	CR10	
R	R116	R91-99
C	C380	C7-9, 15, 22, 25-99, 104-109, 114-119, 122-129, 132-199, 289-299, 311-319, 322-339, 344-359, 362-379

CAUTION
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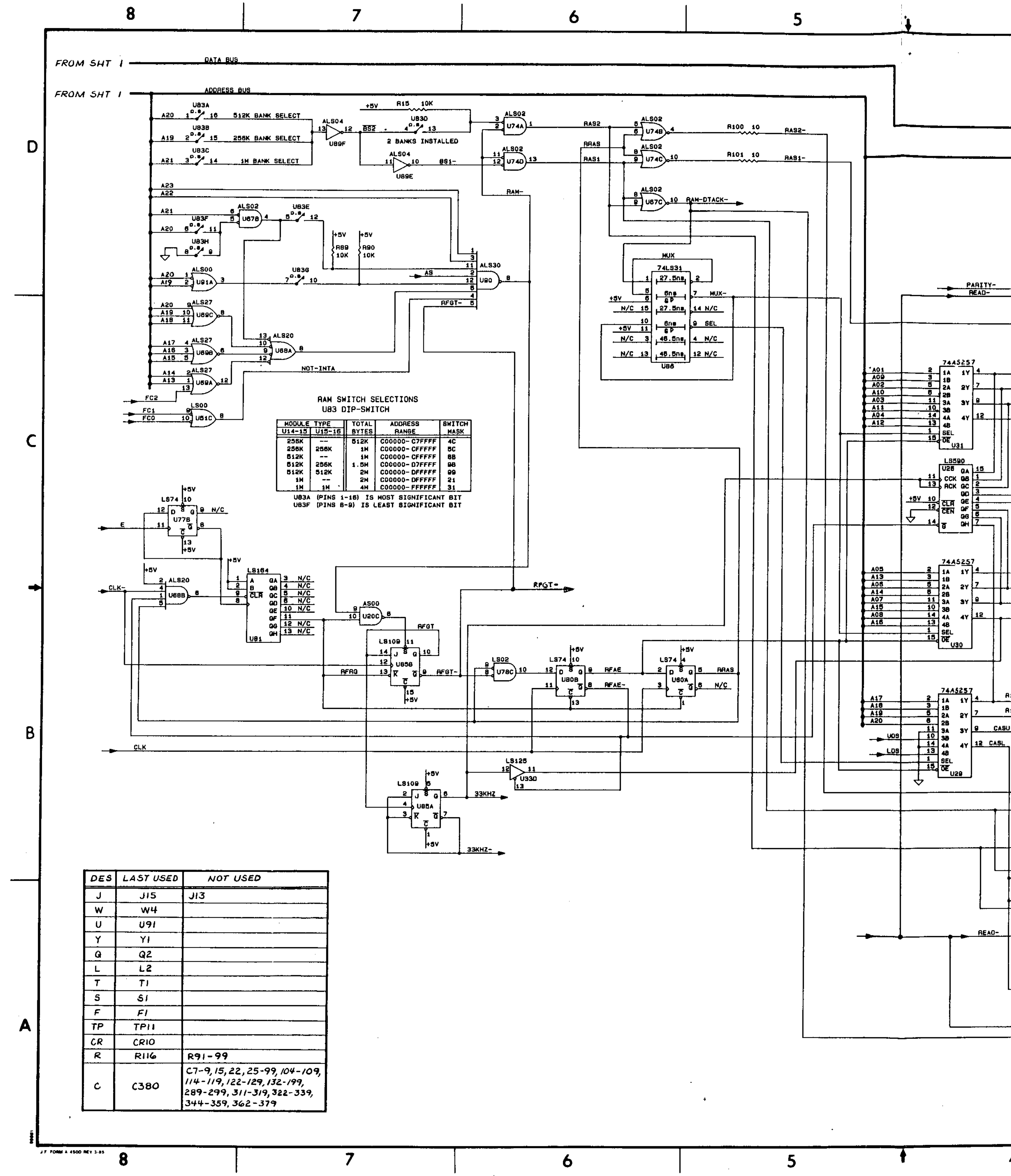
(2 of 4)

J F FORM A 4500 REV 3-85

Figure 7-1. A1 Main PCA (cont.)



RAM SWITCH SELECTIONS
U83 DIP-SWITCH

MODULE TYPE U14-15	MODULE TYPE U15-16	TOTAL BYTES	ADDRESS RANGE	SWITCH MASK
256K	--	512K	C00000- C7FFFF	4C
256K	256K	1M	C00000- CFFFFF	5C
512K	--	1M	C00000- CFFFFF	8B
512K	256K	1.5M	C00000- D7FFFF	9B
512K	512K	2M	C00000- DFFFFF	99
1M	--	2M	C00000- DFFFFF	21
1M	1M	4M	C00000- FFFFFF	31

U83A (PINS 1-16) IS MOST SIGNIFICANT BIT
U83F (PINS 8-9) IS LEAST SIGNIFICANT BIT

DES	LAST USED	NOT USED
J	J15	J13
W	W4	
U	U91	
Y	Y1	
Q	Q2	
L	L2	
T	T1	
S	S1	
F	F1	
TP	TP11	
CR	CR10	
R	R116	R91-99
C	C380	C7-9, 15, 22, 25-99, 104-109, 114-119, 122-129, 132-199, 289-299, 311-319, 322-339, 344-359, 362-379

J F FORM A 4500 REV 3-85

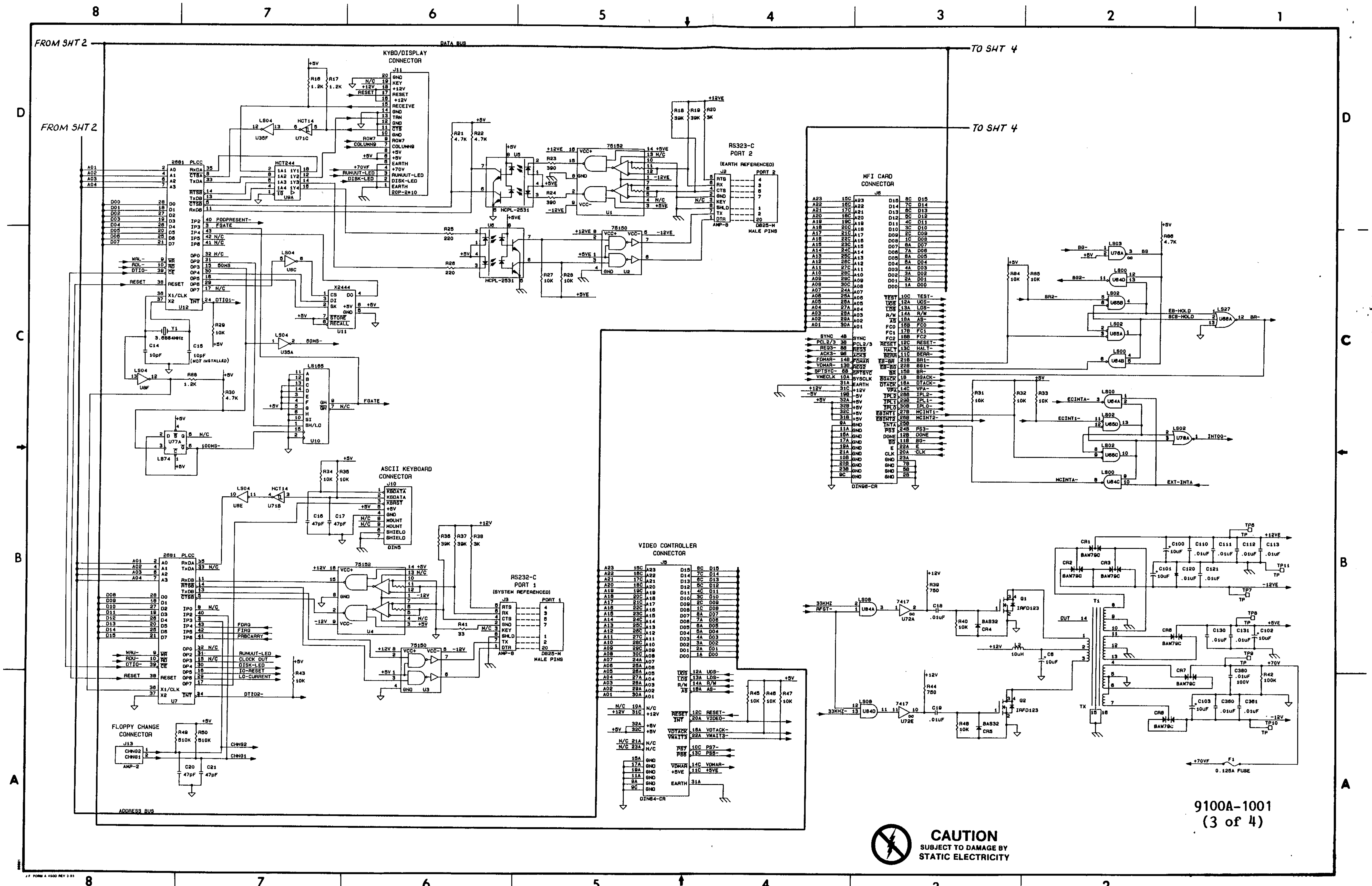
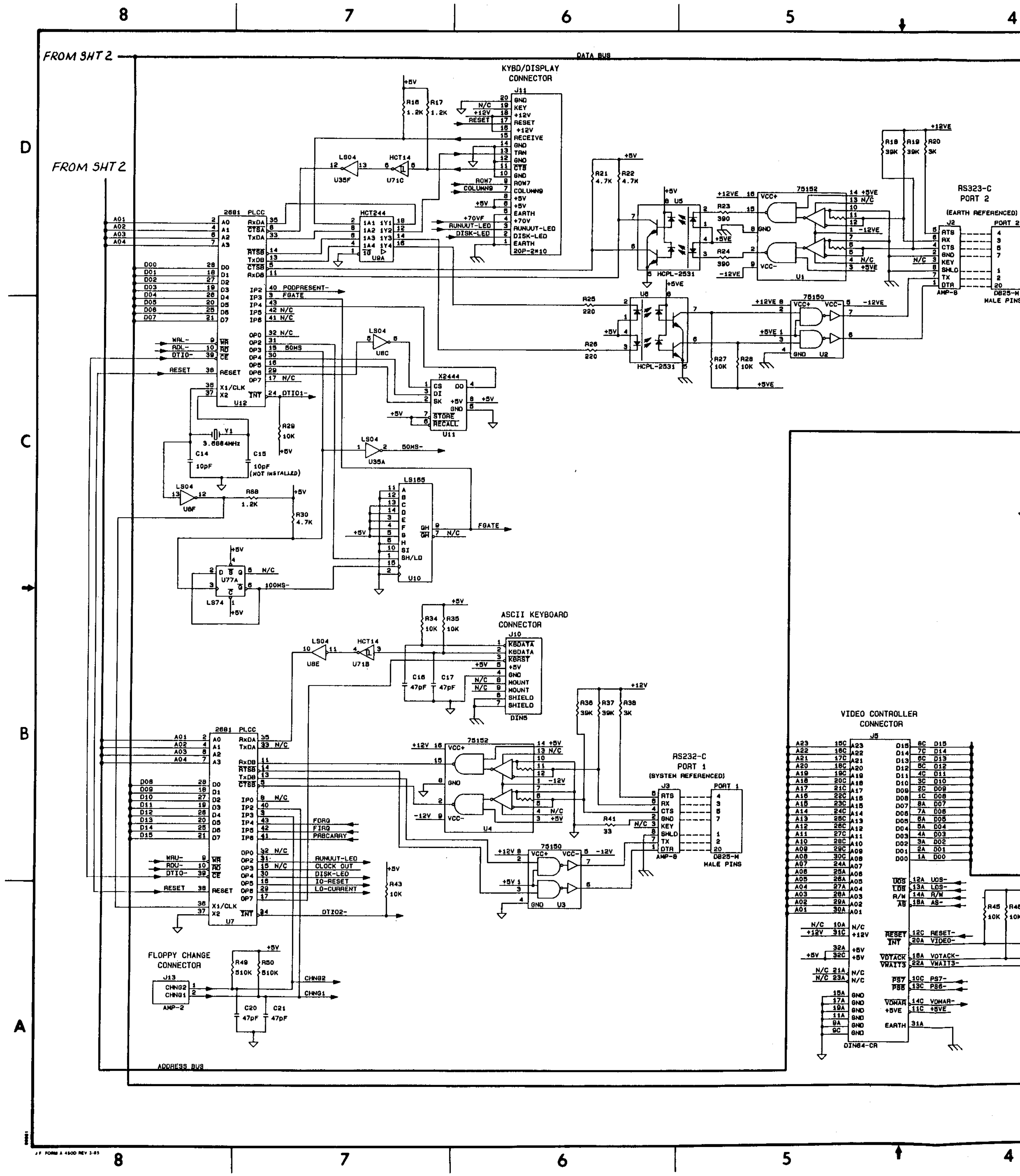
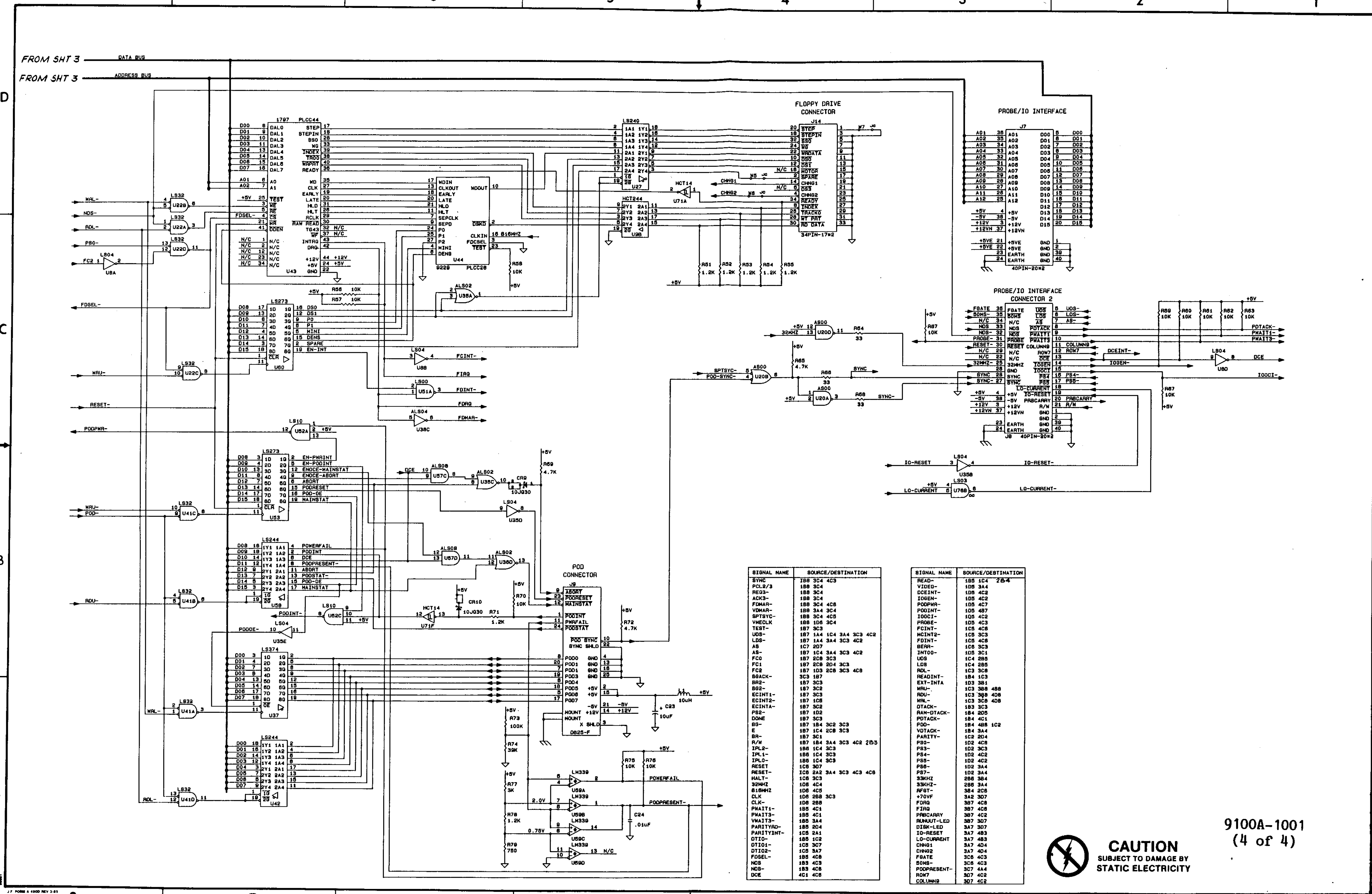


Figure 7-1. A1 Main PCA (cont.)



FROM SHT 2
FROM SHT 2
DATA BUS
KYBD/DISPLAY CONNECTOR
RS323-C PORT 2 (EARTH REFERENCED)
ASCII KEYBOARD CONNECTOR
RS232-C PORT 1 (SYSTEM REFERENCED)
VIDEO CONTROLLER CONNECTOR
FLOPPY CHANGE CONNECTOR
ADDRESS BUS



SIGNAL NAME	SOURCE/DESTINATION
SYNC	1B8 3C4 4C3
PCL2/3	1B8 3C4
REQ3-	1B8 3C4
ACK3-	1B8 3C4
FDMAR-	1B8 3C4 4C6
VDMAR-	1B8 3A4 3C4
SPTSYC-	1B8 3C4 4C5
VMECLK	1B8 1D6 3C4
TEST-	1B7 3C3
UDS-	1B7 1A4 1C4 3A4 3C3 4C2
LDS-	1B7 1A4 3A4 3C3 4C2
AS	1C7 2D7
AS-	1B7 1C4 3A4 3C3 4C2
FC0	1B7 2C8 3C3
FC1	1B7 2C8 2D4 3C3
FC2	1B7 1D3 2C8 3C3 4C8
BGACK-	3C3 1B7
BR2-	1B7 3C3
BG2-	1B7 3C2
ECINT1-	1B7 3C3
ECINT2-	1B7 1C5
ECINTA-	1B7 3C2
PS2-	1B7 1D2
DONE	1B7 3C3
BG-	1B7 1B4 3C2 3C3
E	1B7 1C4 2C8 3C3
BR-	1B7 3C1
R/W	1B7 1B4 3A4 3C3 4C2 2B3
IPL2-	1B6 1C4 3C3
IPL1-	1B6 1C4 3C3
IPL0-	1B6 1C4 3C3
RESET	1C6 3D7
RESET-	1C6 2A2 3A4 3C3 4C3 4C8
HALT-	1C6 3C3
32MHZ	1D6 4C4
B16MHZ	1D6 4C5
CLK	1D6 2B8 3C3
CLK-	1D6 2B8
PWAIT1-	1B5 4C1
PWAIT3-	1B5 4C1
VWAIT3-	1B5 3A4
PARITYRD-	1B5 2D4
PARITYINT-	1C8 2A1
DTIO-	1B5 1C2
DTIO1-	1C5 3C7
DTIO2-	1C5 3A7
FDSEL-	1B5 4C8
NDS	1B3 4C3
NDS-	1B3 4C6
DCE	4C1 4C6

SIGNAL NAME	SOURCE/DESTINATION
READ-	1B5 1C4 2B4
VIDEO-	1D5 3A4
DCEINT-	1D5 4C2
IOGEN-	1D5 4C2
PODPWR-	1D5 4C7
PODINT-	1D5 4B7
IOOCI-	1D5 4C2
PROBE-	1D5 4C3
FCINT-	1C5 4C6
MCINT2-	1C5 3C3
FDINT-	1C5 4C6
BERR-	1C6 3C3
INTOO-	1D5 3C1
UDS	1C4 2B5
LDS	1C4 2B5
RDL-	1C3 3C8
READINT-	1B4 1C3
EXT-INTA	1D3 3B1
WRU-	1C3 3B8 4B8
RDU-	1C3 3B8 4D6
WRL-	1C3 3C8 4D6
DTACK-	1B3 3C3
RAM-DTACK-	1B4 2D5
PDTACK-	1B4 4C1
POD-	1B4 4B8 1C2
VDTACK-	1B4 3A4
PARITY-	1C2 2D4
PS0-	1D2 4C8
PS3-	1D2 3C3
PS4-	1D2 4C2
PS5-	1D2 4C2
PS6-	1D2 3A4
PS7-	1D2 3A4
33KHZ	2B6 3B4
33KHZ-	2B6 3A4
RFGT-	3B4 2C6
+70VF	3A2 3D7
FDRQ	3B7 4C8
FIRQ	3B7 4C8
PRBCARRY	3B7 4C2
RUNUUT-LED	3B7 3D7
DISK-LED	3A7 3D7
IO-RESET	3A7 4B3
LO-CURRENT	3A7 4B3
CHNG1	3A7 4D4
CHNG2	3A7 4D4
FGATE	3C6 4C3
50MS-	3C6 4C3
PODPRESENT-	3C7 4A4
ROW7	3D7 4C2
COLUMN8	3D7 4C2

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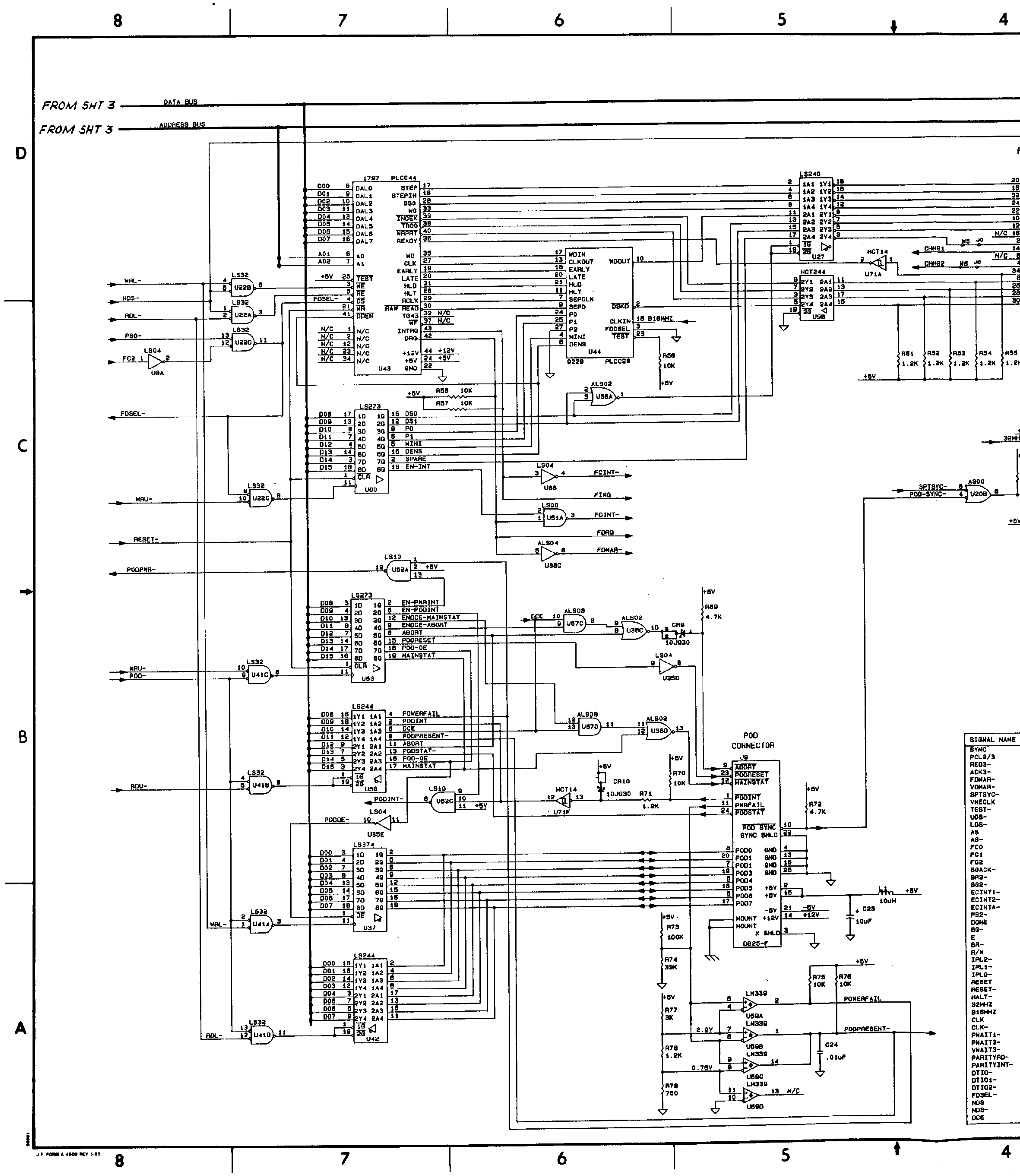
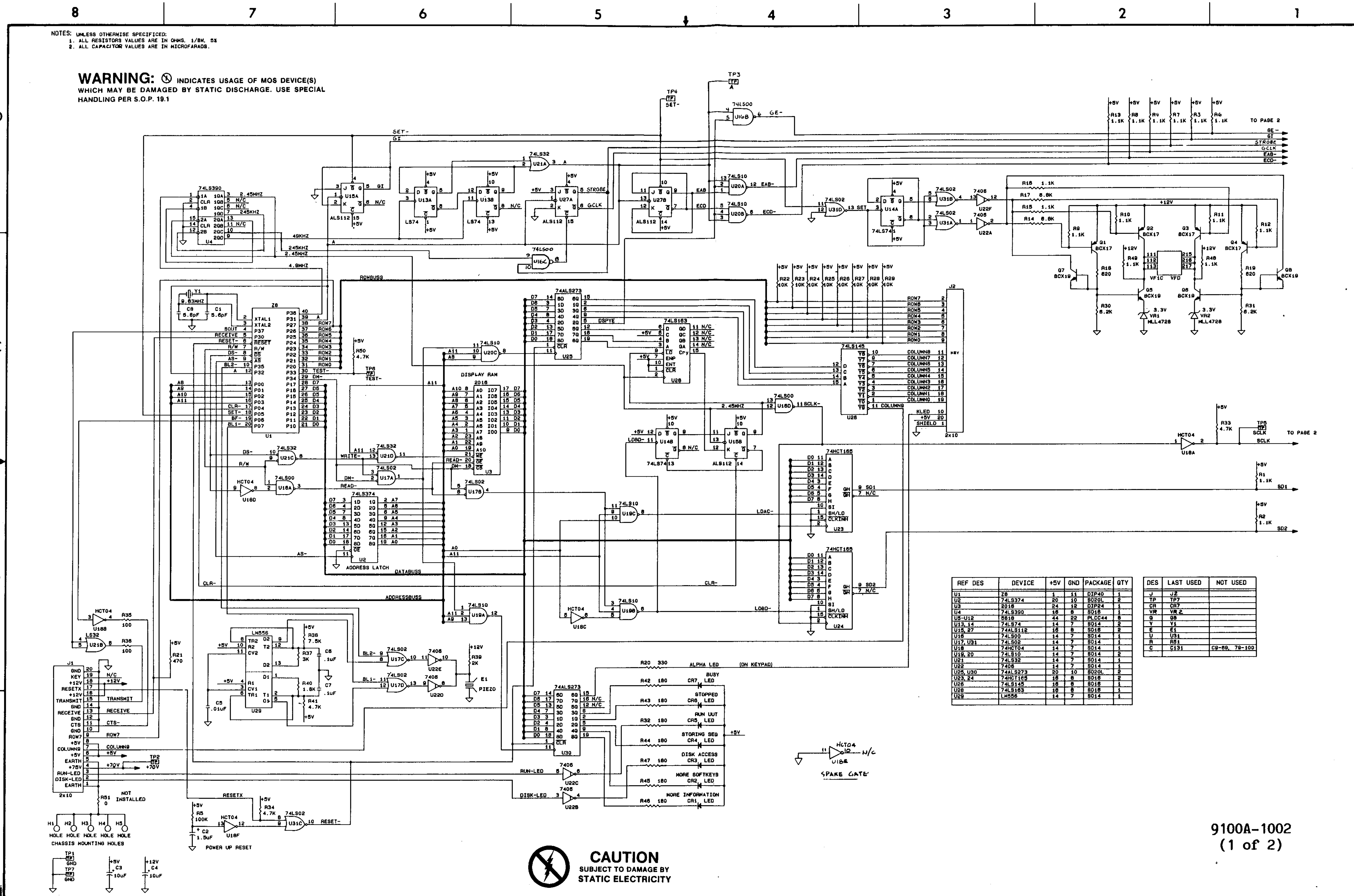
Figure 7-1. A1 Main PCA (cont.)



FROM SHT 3
DATA BUS
FROM SHT 3
ADDRESS BUS
1797 PLCC44
U43
9229 PLCC28
U44
LS273
U60
LS273
U53
LS244
U58
LS374
U37
LS244
U42
POD CONNECTOR
J9
DB25-F
POWERFAIL
PODPRESENT-
SIGNAL NAME
SYNC
PCL2/3
REQ3-
ACK3-
FDMAR-
VDMAR-
SPTSYC-
VMECLK
TEST-
UDS-
LDS-
AS
AS-
FC0
FC1
FC2
BGACK-
BR2-
BG2-
ECINT1-
ECINT2-
ECINTA-
PS2-
DONE
SG-
E
BR-
R/W
IPL2-
IPL1-
IPL0-
RESET
RESET-
HALT-
32MHZ
B16MHZ
CLK
CLK-
PWAIT1-
PWAIT3-
VWAIT3-
PARITYRD-
PARITYINT-
DTIO-
DTIO1-
DTIO2-
FDSEL-
NDS
NDS-
DCE



REF DES	DEVICE	+5V	GND	PACKAGE	QTY
U1	Z8	1	11	DIP40	1
U2	74LS374	20	10	SO20L	2
U3	2016	24	12	DIP24	1
U4	74LS390	16	8	SO16	1
U5-U12	5818	44	22	PLCC44	8
U13, 14	74LS74	14	7	SO14	2
U15, 27	74ALS112	16	8	SO16	2
U16	74LS00	14	7	SO14	1
U17, U31	74LS02	14	7	SO14	1
U18	74HCT04	14	7	SO14	1
U19, 20	74LS10	14	7	SO14	2
U21	74LS32	14	7	SO14	1
U22	7406	14	7	SO14	1
U25, U30	74ALS273	20	10	SO20L	2
U23, 24	74HCT165	16	8	SO16	2
U26	74LS145	16	8	SO16	1
U28	74LS163	16	8	SO16	1
U29	LM556	14	7	SO14	1

DES	LAST USED	NOT USED
J	J2	
TP	TP7	
CR	CR7	
VR	VR 2	
Q	Q8	
Y	Y1	
E	E1	
U	U31	
R	R51	
C	C131	C9-69, 79-100

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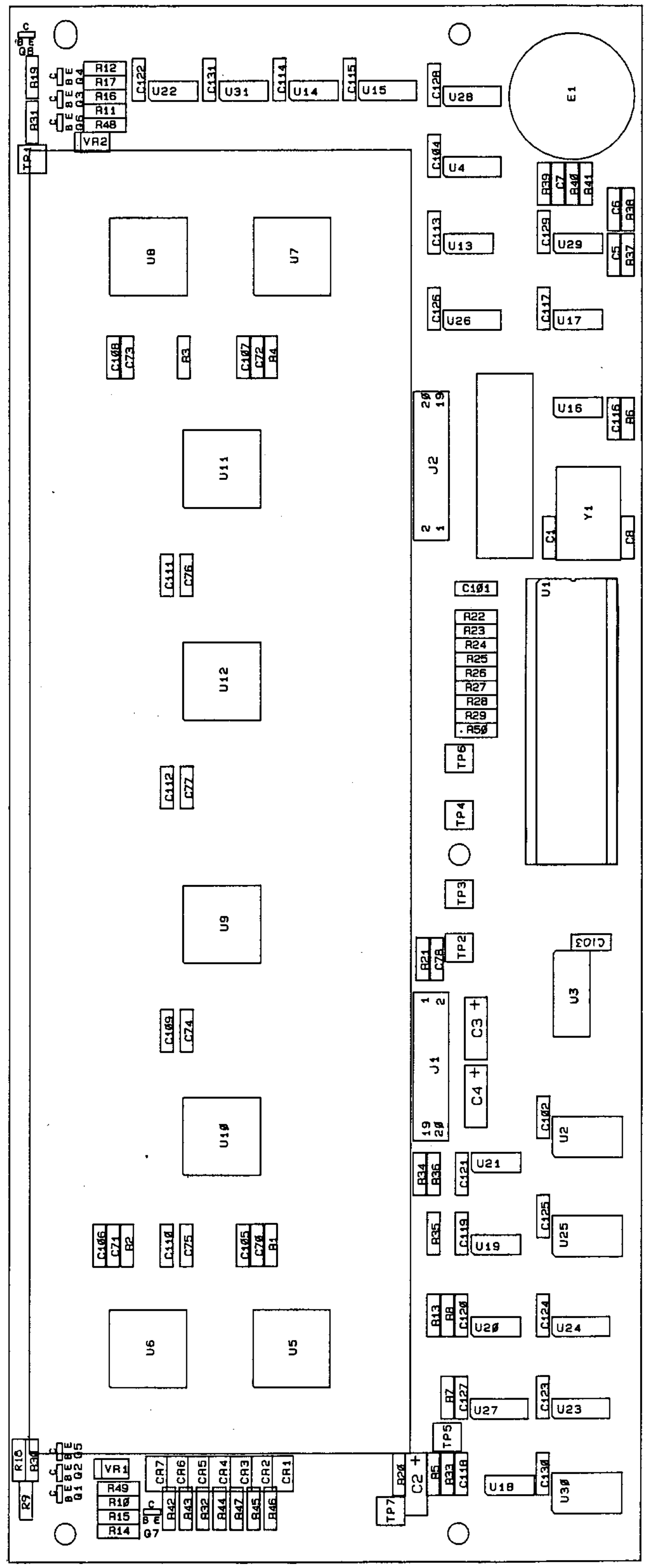
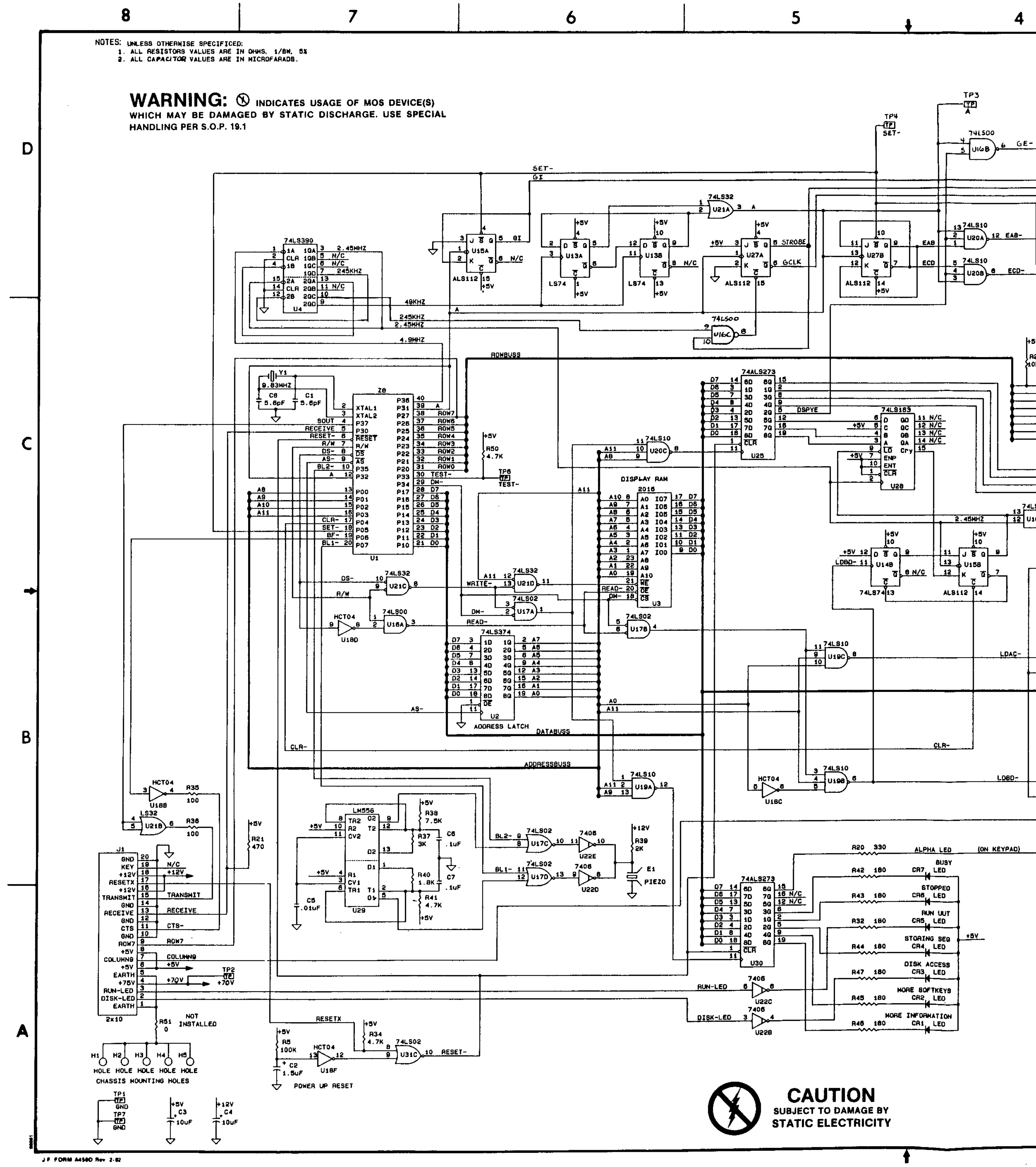
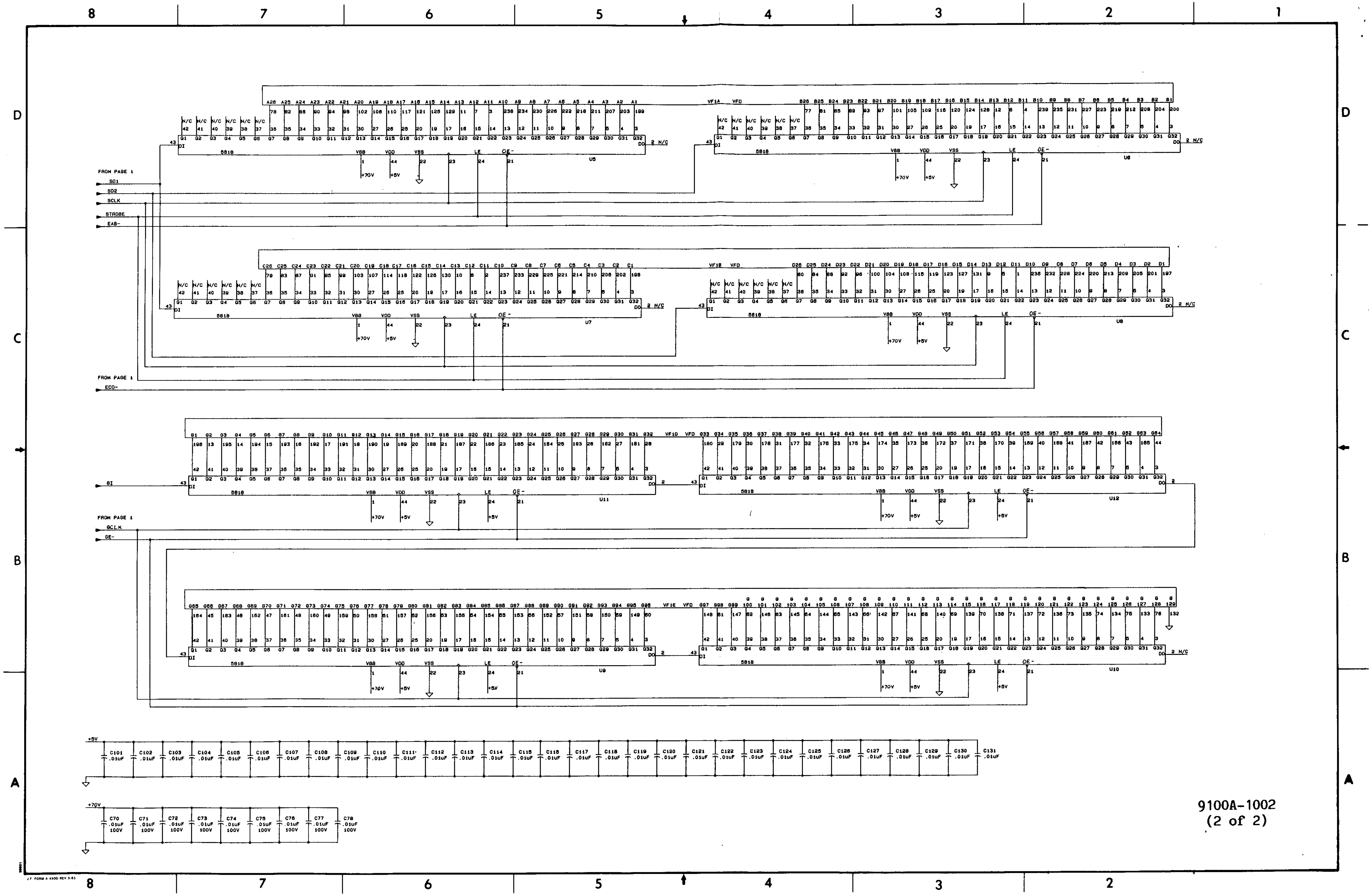
Figure 7-2. A2 Display Interface PCA



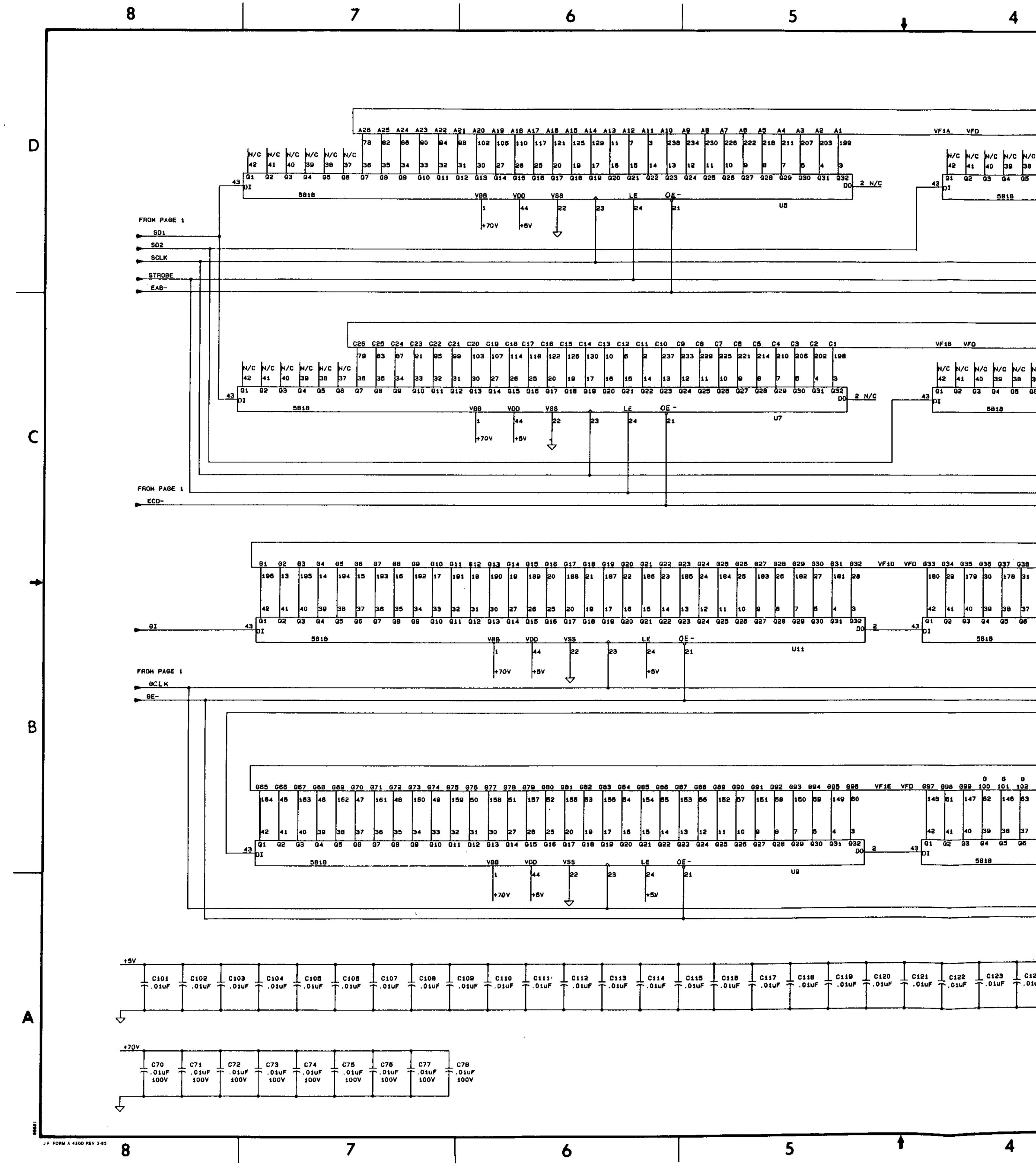
9100A-1602


NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS VALUES ARE IN OHMS, 1/8W, 5%
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
WARNING: ⓢ INDICATES USAGE OF MOS DEVICE(S) WHICH MAY BE DAMAGED BY STATIC DISCHARGE. USE SPECIAL HANDLING PER S.O.P. 19.1
CAUTION
SUBJECT TO DAMAGE BY STATIC ELECTRICITY
CHASSIS MOUNTING HOLES
POWER UP RESET
DISPLAY RAM
ADDRESS LATCH
ADDRESSBUSS
DATABUSS
ROWBUSS

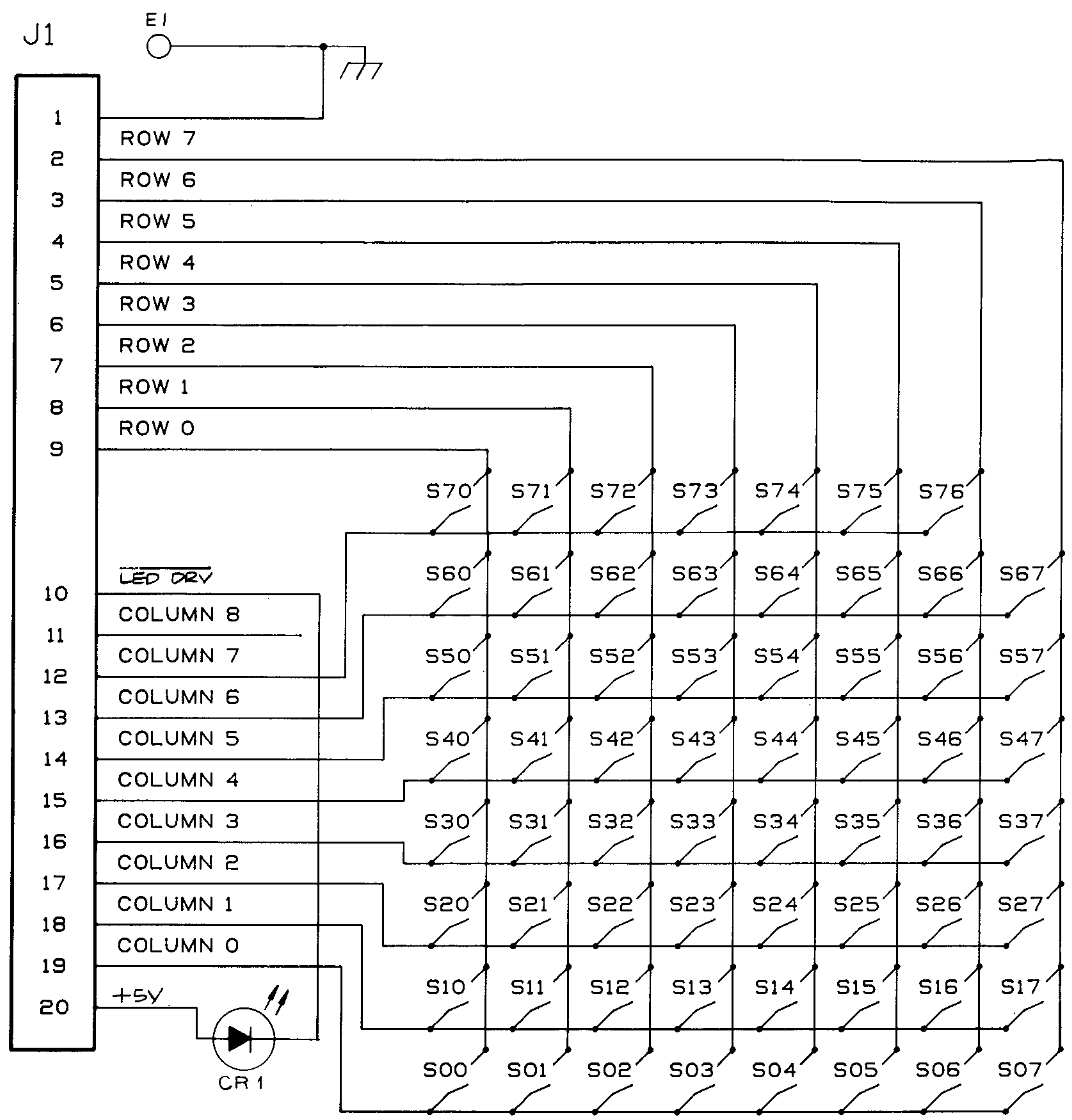


9100A-1002
(2 of 2)

Figure 7-2. A2 Display Interface PCA (cont.)



J.F. FORM A 4500 REV 3-85

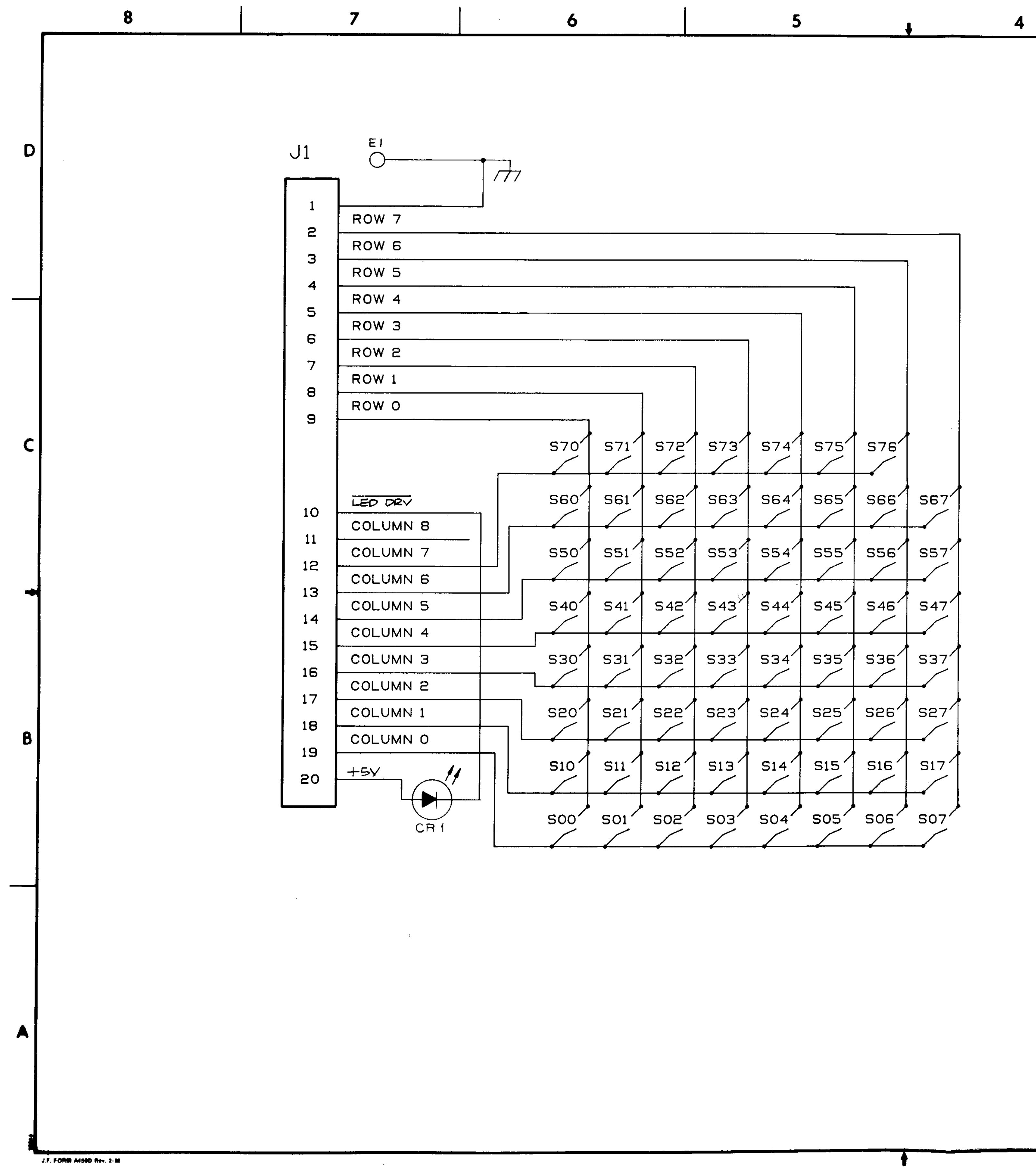


KEY CHART

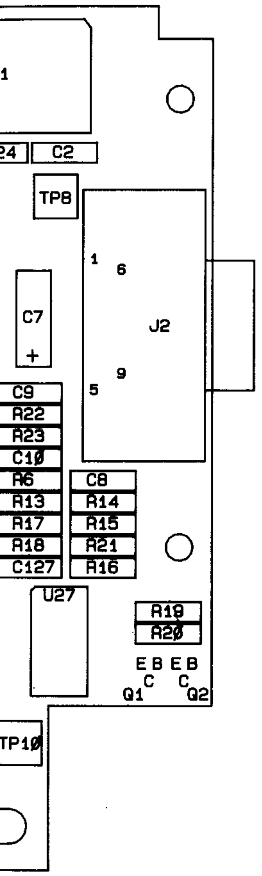
SWITCH NO.	FUNCTION	SWITCH NO.	FUNCTION
00	ALPHA	40	F
01	EXEC	41	ENTER YES
02	MAIN MENU	42	B
03	GFI	43	NOT USED
04	SETUP MENU	44	7
05	SEQ	45	NOT USED
06	OPTION	46	3
07	BLANK	47	←
10	PROBE	50	CLEAR NO
11	BUS TEST	51	NOT USED
12	I/O MOD	52	NOT USED
13	RAM TEST	53	NOT USED
14	POD	54	↑
15	ROM TEST	55	NOT USED
16	SYNC	56	↓
17	BLANK	57	→
20	READ	60	EDIT
21	C	61	HELP
22	WRITE	62	NOT USED
23	8	63	NOT USED
24	STIM	64	REPEAT
25	4	65	STOP
26	RUN UUT	66	LOOP
27	0	67	CONT
30	D	70	SOFT KEYS
31	E	71	F1
32	9	72	F2
33	A	73	F3
34	5	74	F4
35	6	75	F5
36	1	76	RESET
37	2		

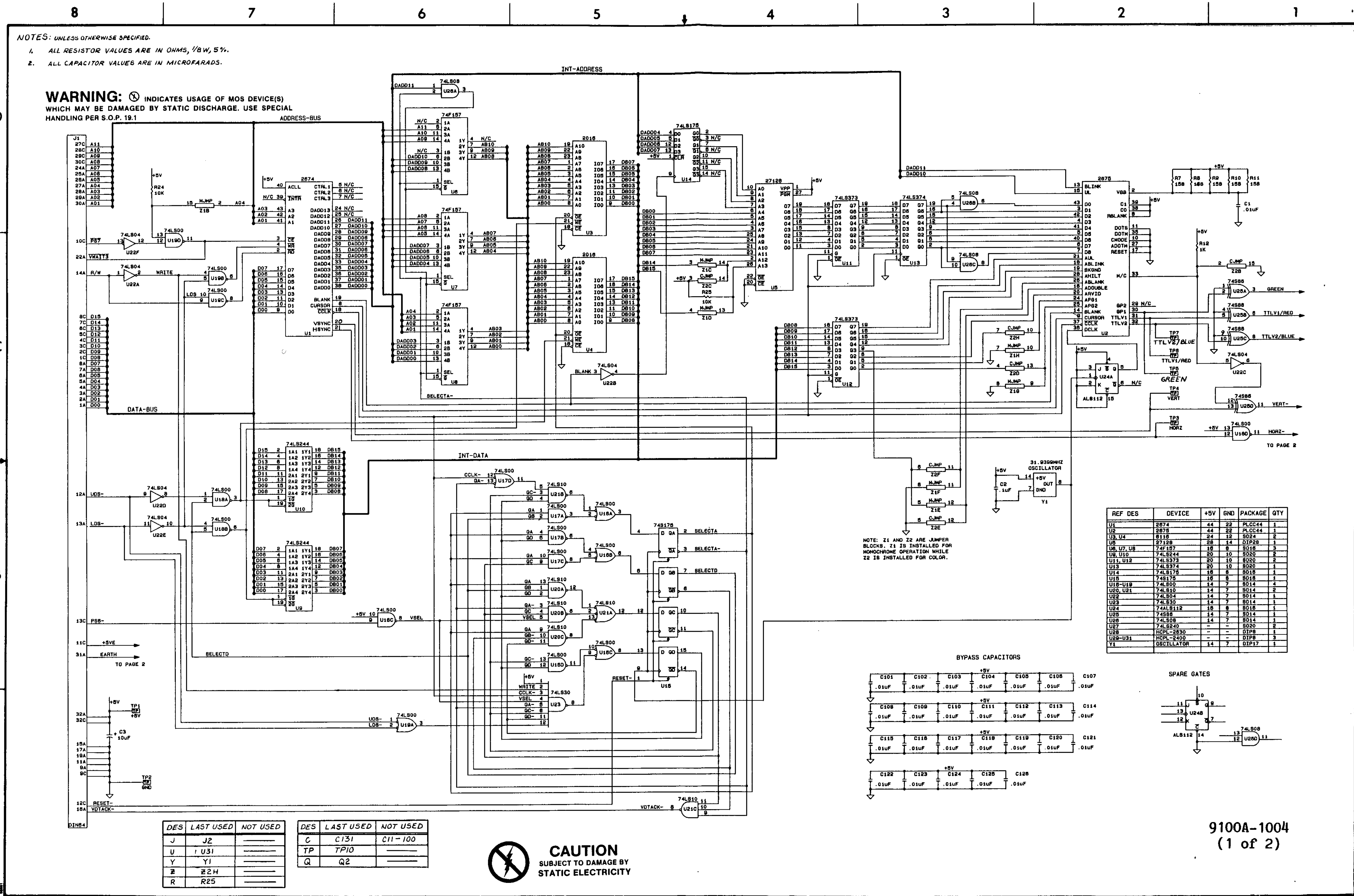
9100A-1003

Figure 7-3. A3 Keypad PCA



8
7
6
5
4
D
C
B
A
J1
E1
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
ROW 7
ROW 6
ROW 5
ROW 4
ROW 3
ROW 2
ROW 1
ROW 0
LED DRV
COLUMN 8
COLUMN 7
COLUMN 6
COLUMN 5
COLUMN 4
COLUMN 3
COLUMN 2
COLUMN 1
COLUMN 0
+5V
CR1
S70 S71 S72 S73 S74 S75 S76
S60 S61 S62 S63 S64 S65 S66 S67
S50 S51 S52 S53 S54 S55 S56 S57
S40 S41 S42 S43 S44 S45 S46 S47
S30 S31 S32 S33 S34 S35 S36 S37
S20 S21 S22 S23 S24 S25 S26 S27
S10 S11 S12 S13 S14 S15 S16 S17
S00 S01 S02 S03 S04 S05 S06 S07



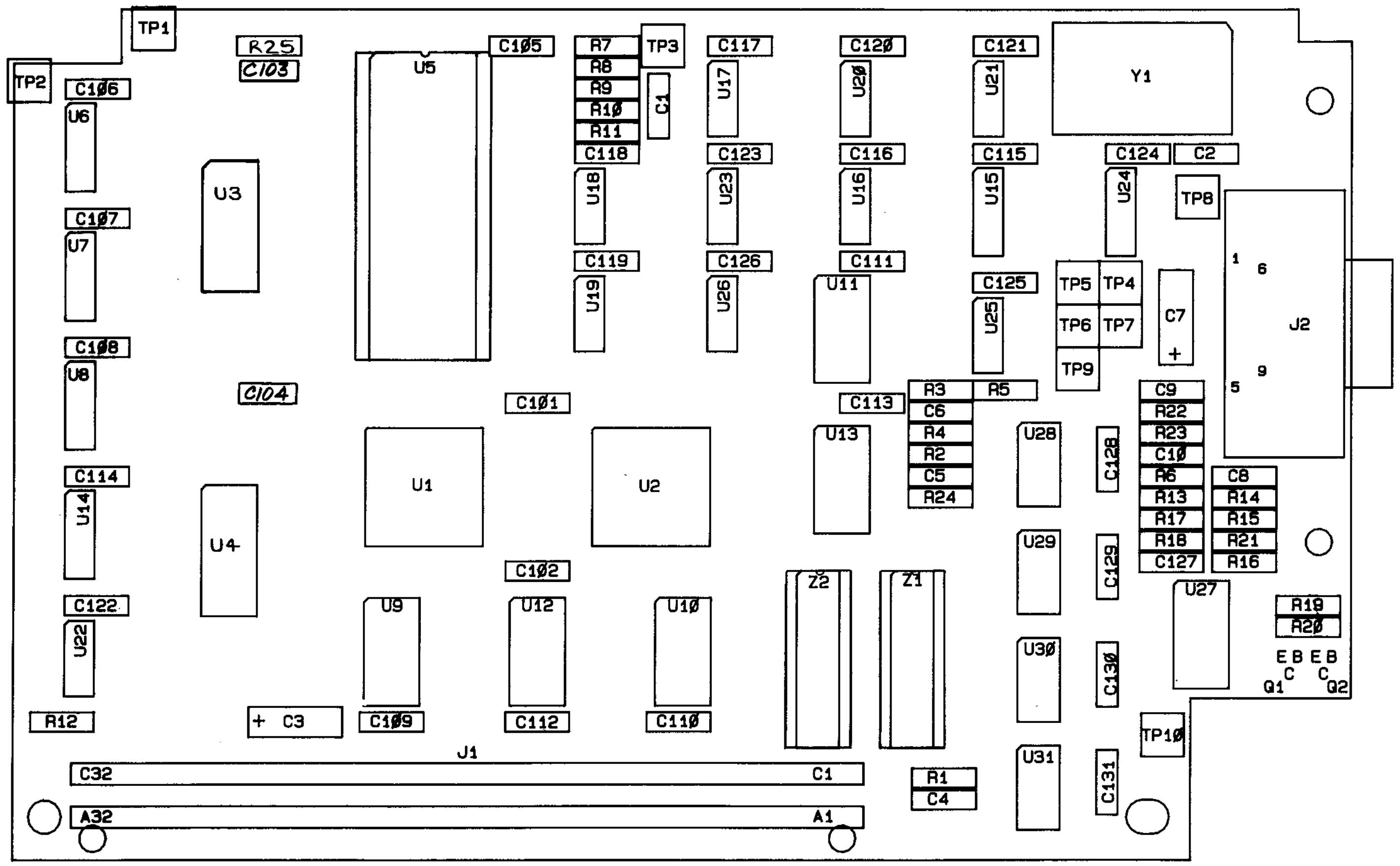


REF DES	DEVICE	+5V	GND	PACKAGE	QTY
U1	2674	44	22	PLCC44	1
U2	2675	44	22	PLCC44	1
U3, U4	6116	24	12	SO24	2
U5	27128	28	14	DIP28	1
U6, U7, U8	74F157	16	8	SO16	3
U9, U10	74LS244	20	10	SO20	2
U11, U12	74LS373	20	10	SO20	2
U13	74LS374	20	10	SO20	1
U14	74LS175	16	8	SO16	1
U15	74S175	16	8	SO16	1
U16-U19	74LS00	14	7	SO14	4
U20, U21	74LS10	14	7	SO14	2
U22	74LS04	14	7	SO14	1
U23	74LS30	14	7	SO14	1
U24	74ALS112	16	8	SO16	1
U25	74S86	14	7	SO14	1
U26	74LS08	14	7	SO14	1
U27	74LS240	-	-	SO20	2
U28	HCPL-2630	-	-	DIP8	1
U29-U31	HCPL-2400	-	-	DIP8	3
Y1	OSCILLATOR	14	7	DIP17	1

DES	LAST USED	NOT USED
J	J2	——
U	U31	——
Y	Y1	——
Z	Z2H	——
R	R25	——

DES	LAST USED	NOT USED
C	C131	C11-100
TP	TP10	——
Q	Q2	——

Figure 7-4. A4 Video Controller PCA



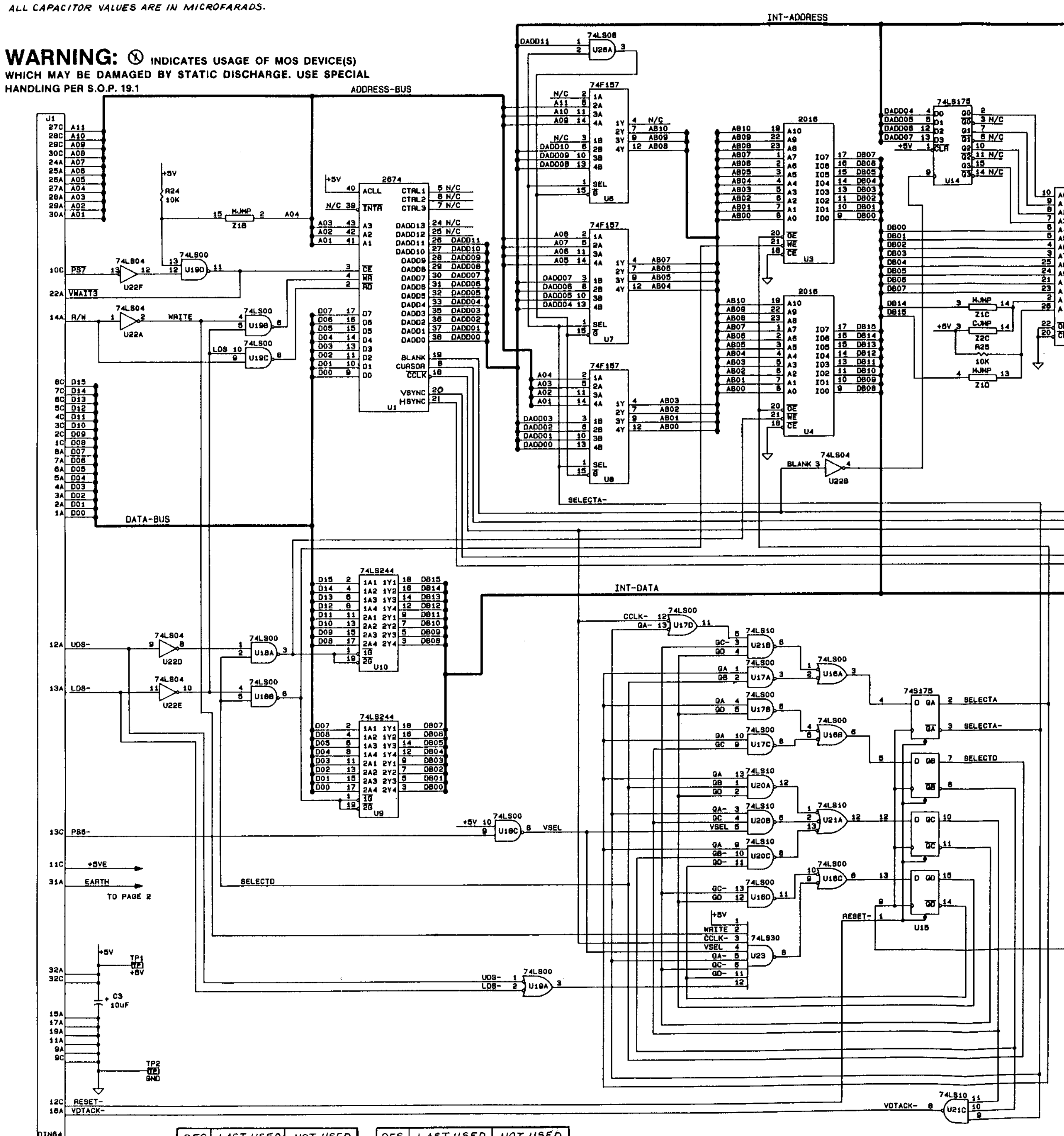
9100A-1604

8 7 6 5

NOTES: UNLESS OTHERWISE SPECIFIED.

1. *ALL RESISTOR VALUES ARE IN OHMS, 1/8W, 5%.*
2. *ALL CAPACITOR VALUES ARE IN MICROFARADS.*

WARNING: ⊗ INDICATES USAGE OF MOS DEVICE(S) WHICH MAY BE DAMAGED BY STATIC DISCHARGE. USE SPECIAL HANDLING PER S.O.P. 19.1



DES	LAST USED	NOT USED
J	J2	———
U	U31	———
Y	Y1	———
Z	Z2H	———
R	R25	———

DES	LAST USED	NOT USED
C	C131	C11-100
TP	TP10	———
Q	Q2	———

CAUTION
SUBJECT TO DAMAGE BY STATIC ELECTRICITY

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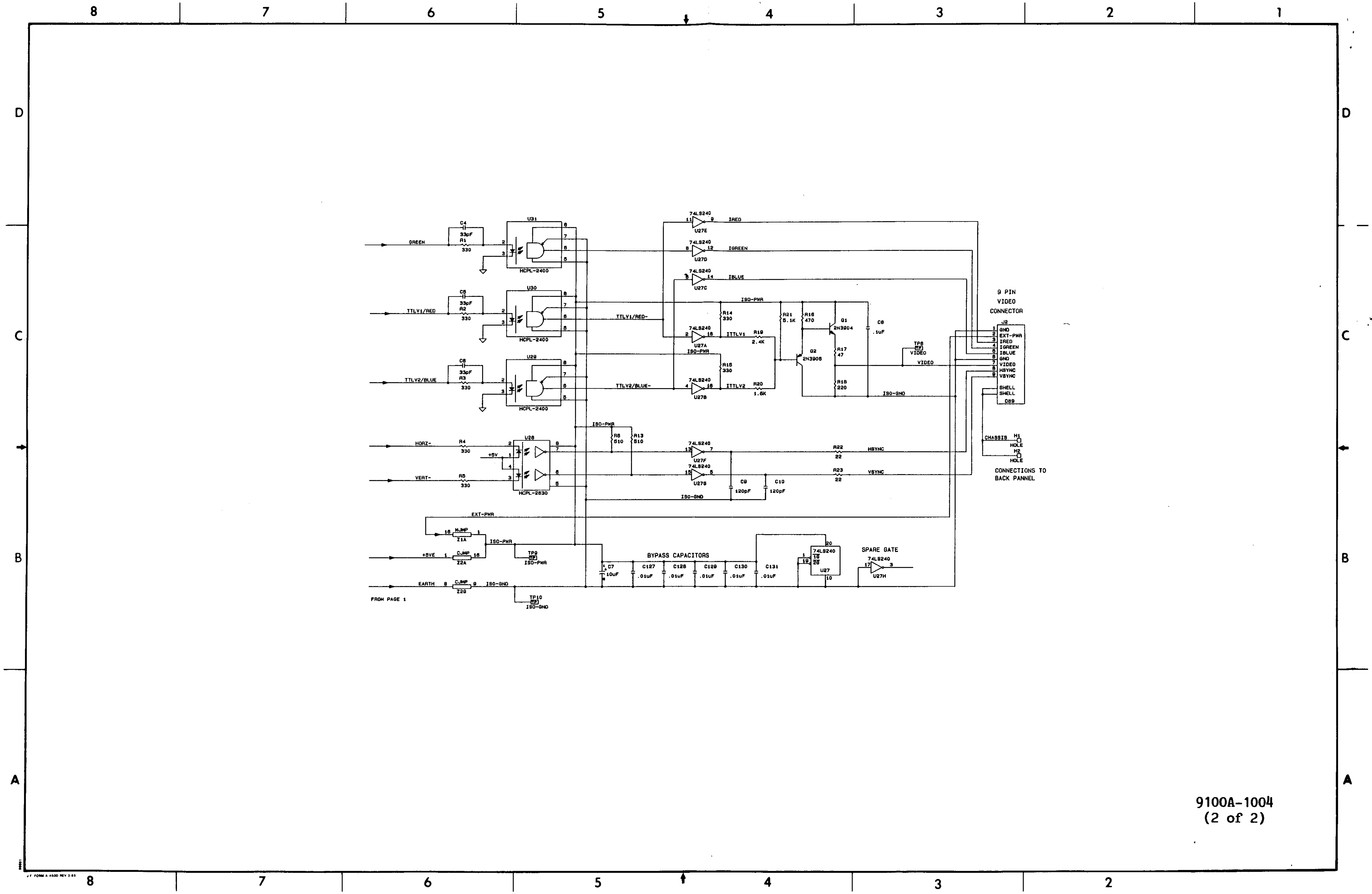
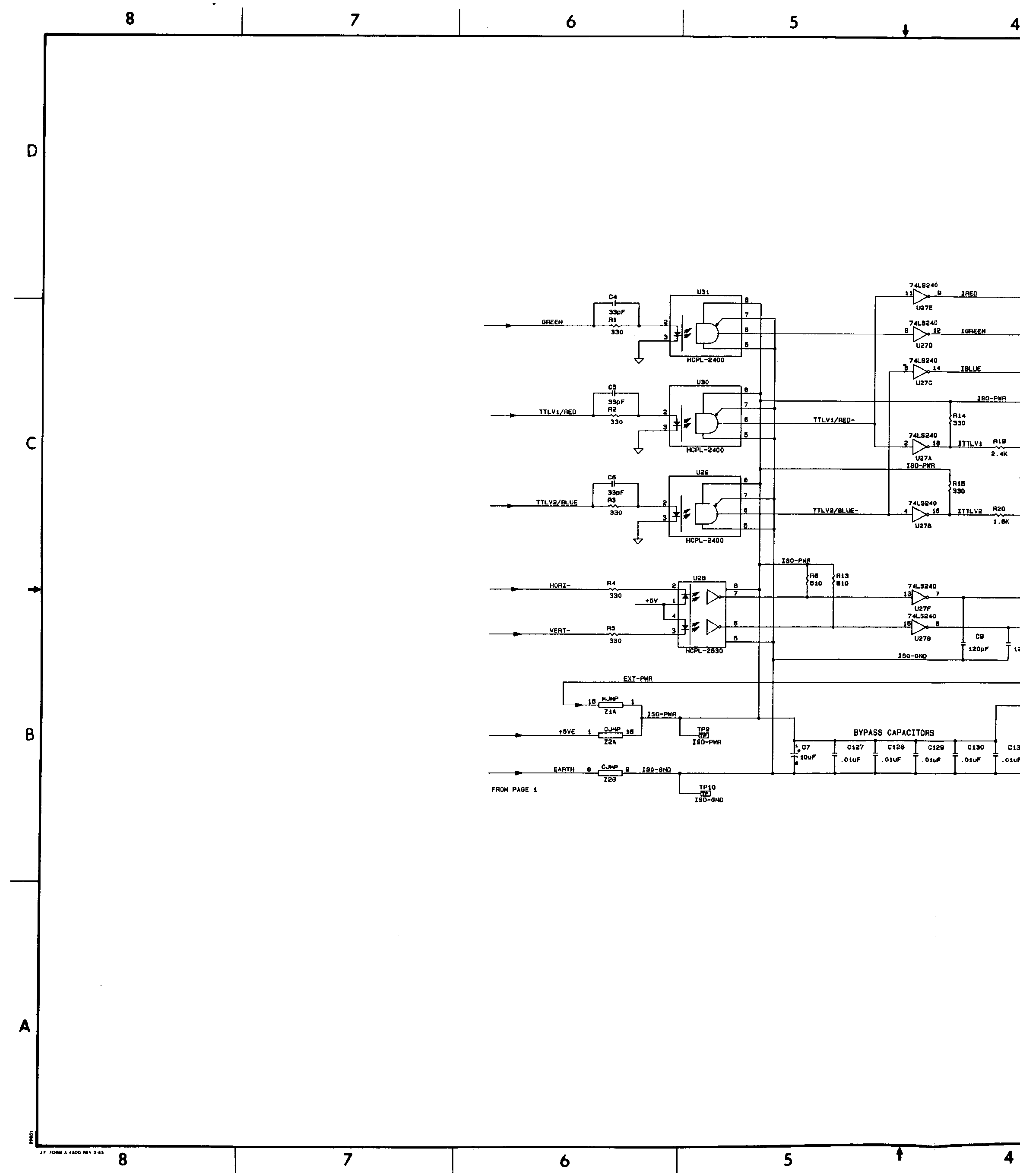
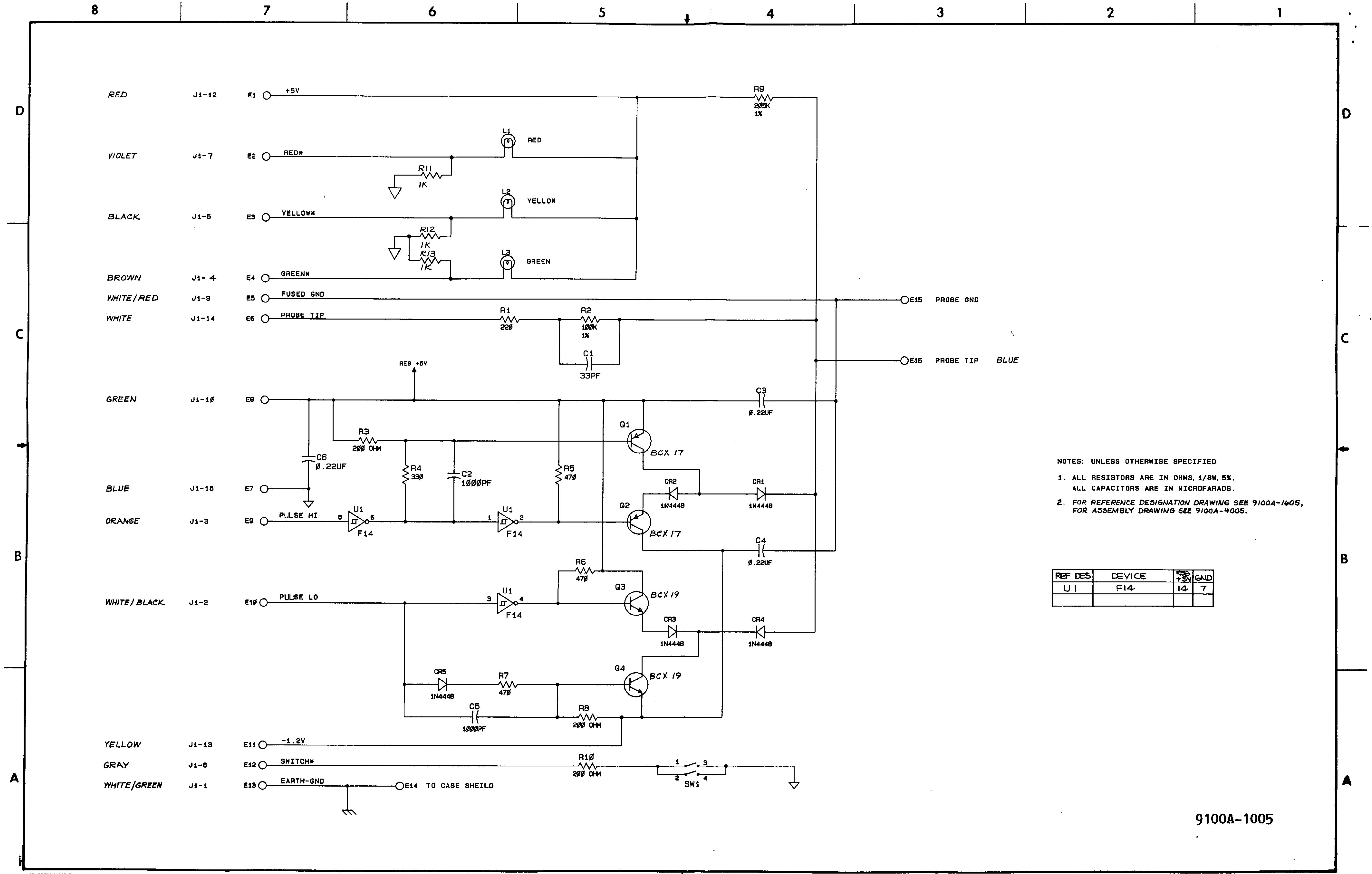


Figure 7-4. A4 Video Controller PCA (cont.)



8
7
6
5
4
D
C
B
A
GREEN
TTLV1/RED
TTLV2/BLUE
HORZ-
VERT-
C4
33pF
C5
33pF
C6
33pF
R1
330
R2
330
R3
330
R4
330
R5
330
U31
U30
U29
U28
HCPL-2400
HCPL-2630
+5V
TTLV1/RED-
TTLV2/BLUE-
74LS240
U27E
U27D
U27C
U27A
U27B
U27F
U27G
IRED
IGREEN
IBLUE
ISO-PWR
R14
330
R15
330
ITTLV1
R19
2.4K
ITTLV2
R20
1.8K
R6
510
R13
510
C9
120pF
ISO-GND
EXT-PWR
Z1A
Z2A
Z2B
+5VE
EARTH
TP9
ISO-PWR
TP10
ISO-GND
FROM PAGE 1
BYPASS CAPACITORS
C7
10uF
C127
C128
C129
C130
.01uF



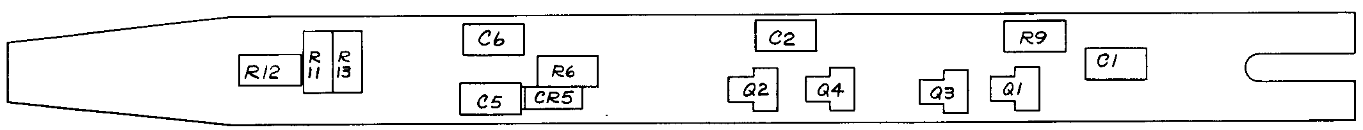
NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, 1/8W, 5%. ALL CAPACITORS ARE IN MICROFARADS.
2. FOR REFERENCE DESIGNATION DRAWING SEE 9100A-1605, FOR ASSEMBLY DRAWING SEE 9100A-4005.

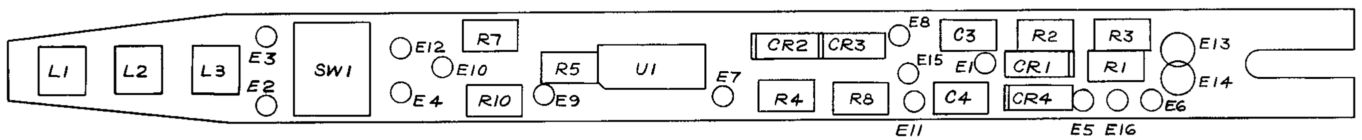
REF DES	DEVICE	REG +5V	GND
U1	F14	14	7

9100A-1005

Figure 7-5. A5 Probe PCA

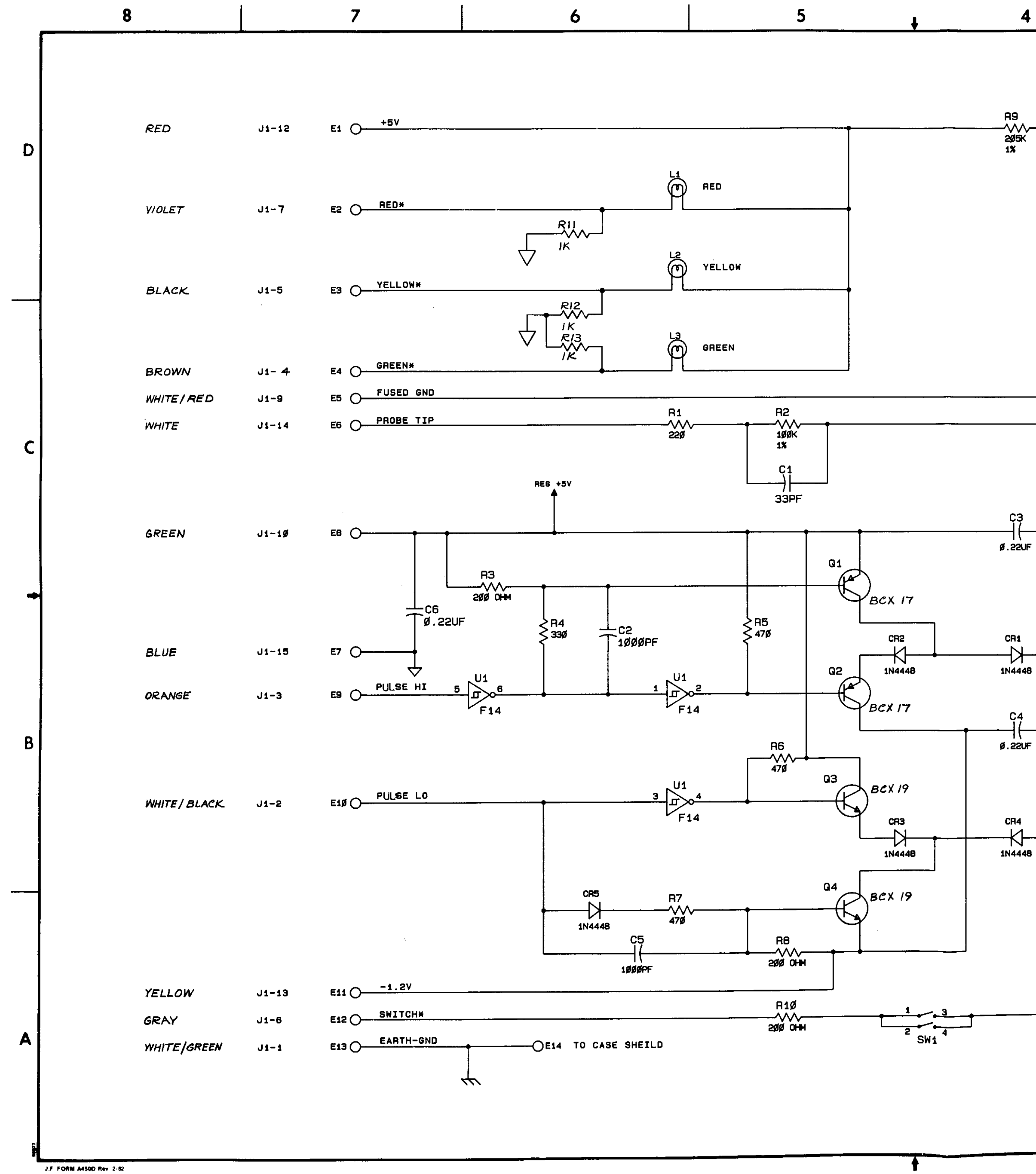


CKT 1



CKT 2

9100A-1605



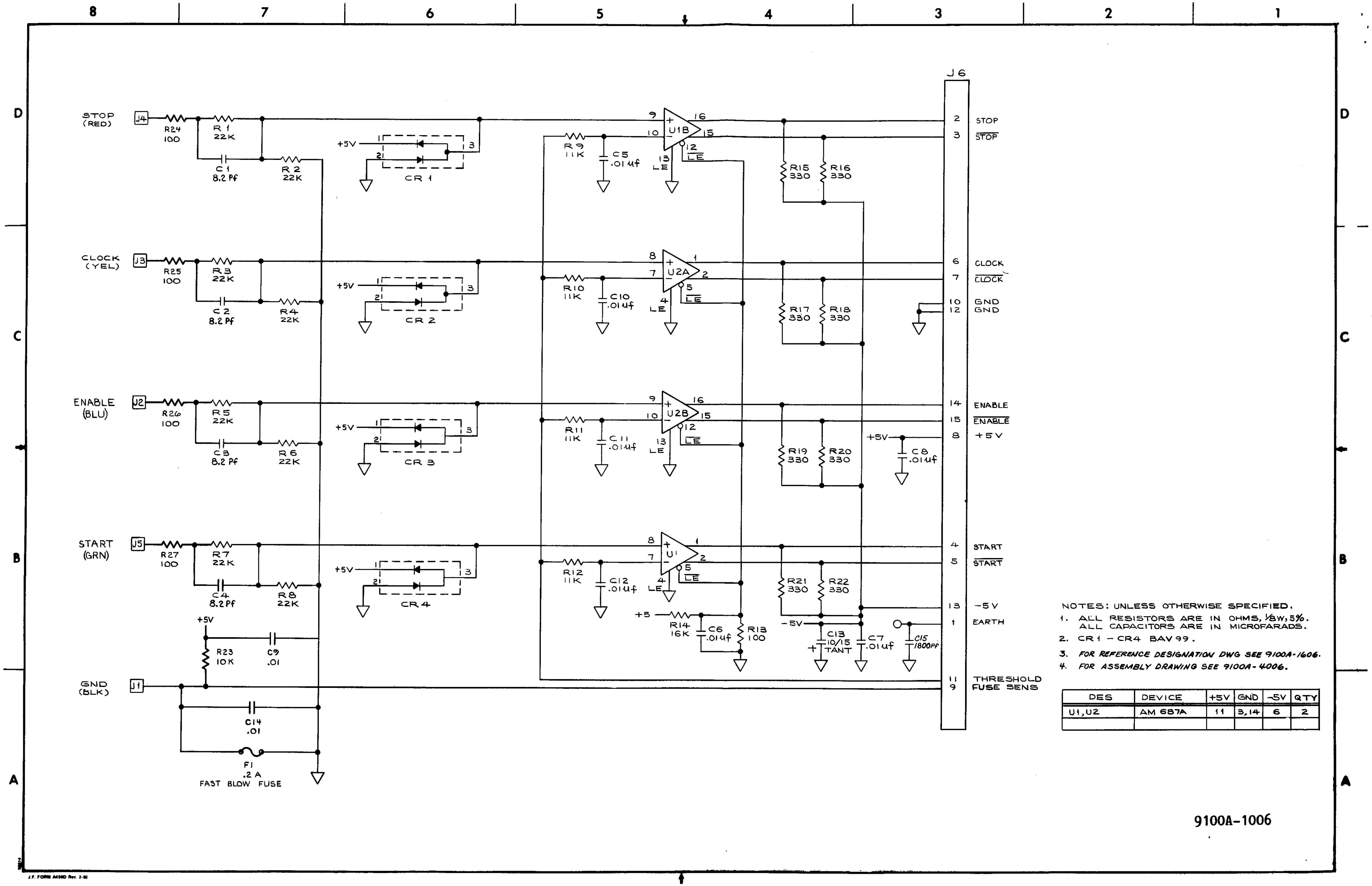
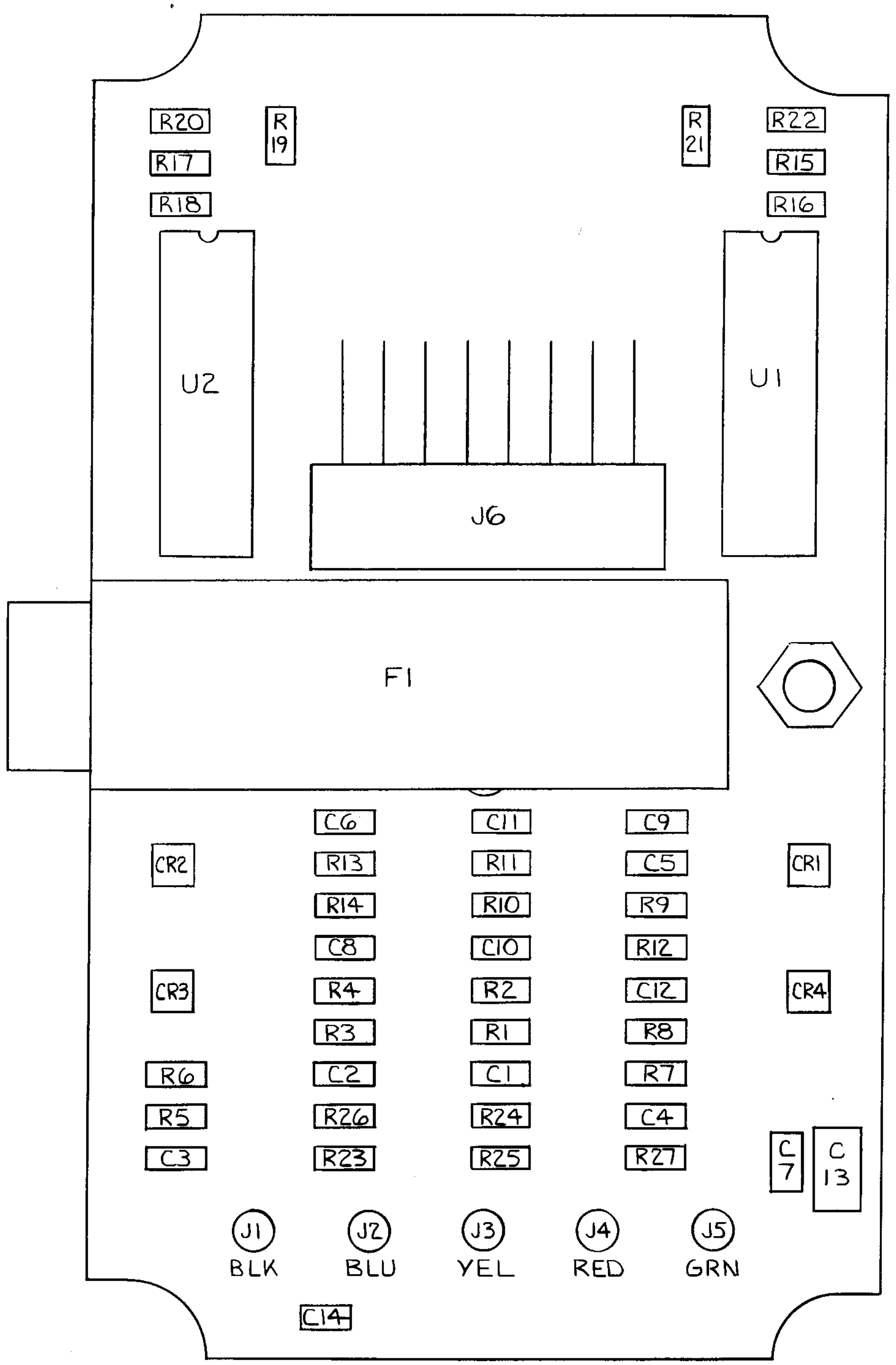
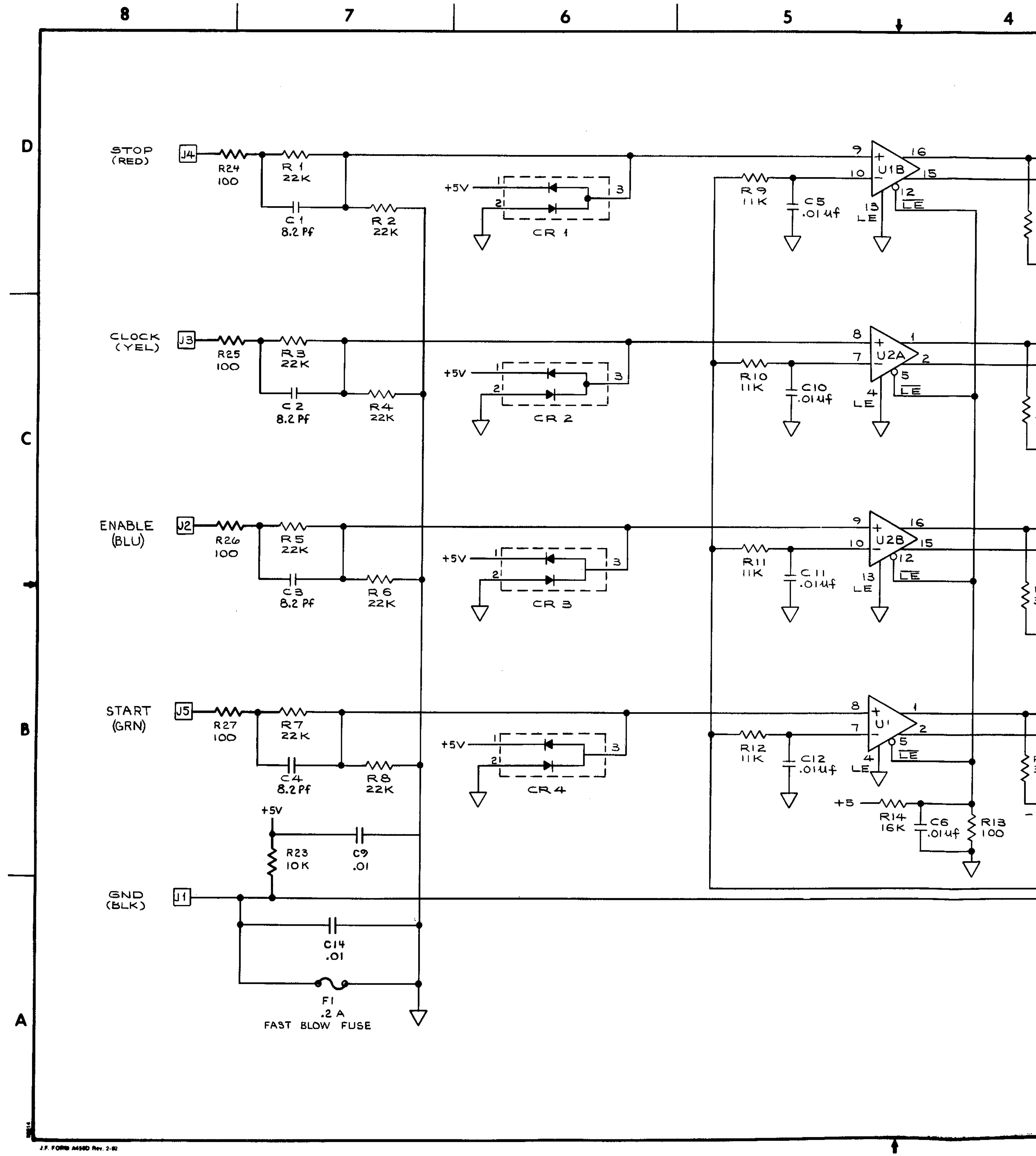


Figure 7-6. A6 Clock Module PCA


R20
R19
R21
R22
R17
R15
R18
R16
U2
U1
J6
F1
C6
C11
C9
CR2
R13
R11
C5
CR1
R14
R10
R9
C8
C10
R12
CR3
R4
R2
C12
CR4
R3
R1
R8
R6
C2
C1
R7
R5
R26
R24
C4
C3
R23
R25
R27
C7
C13
J1
J2
J3
J4
J5
BLK
BLU
YEL
RED
GRN
C14

9100A-1606


8
7
6
5
4
D
C
B
A
STOP (RED)
J4
R24 100
R1 22K
C1 8.2 Pf
R2 22K
+5V
CR1
R9 11K
C5 .01uf
U1B
LE
CLOCK (YEL)
J3
R25 100
R3 22K
C2 8.2 Pf
R4 22K
+5V
CR2
R10 11K
C10 .01uf
U2A
LE
ENABLE (BLU)
J2
R26 100
R5 22K
C3 8.2 Pf
R6 22K
+5V
CR3
R11 11K
C11 .01uf
U2B
LE
START (GRN)
J5
R27 100
R7 22K
C4 8.2 Pf
R8 22K
+5V
CR4
R12 11K
C12 .01uf
U1
LE
+5V
R23 10K
C9 .01
+5
R14 16K
C6 .01uf
R13 100
GND (BLK)
J1
C14 .01
F1 .2 A FAST BLOW FUSE

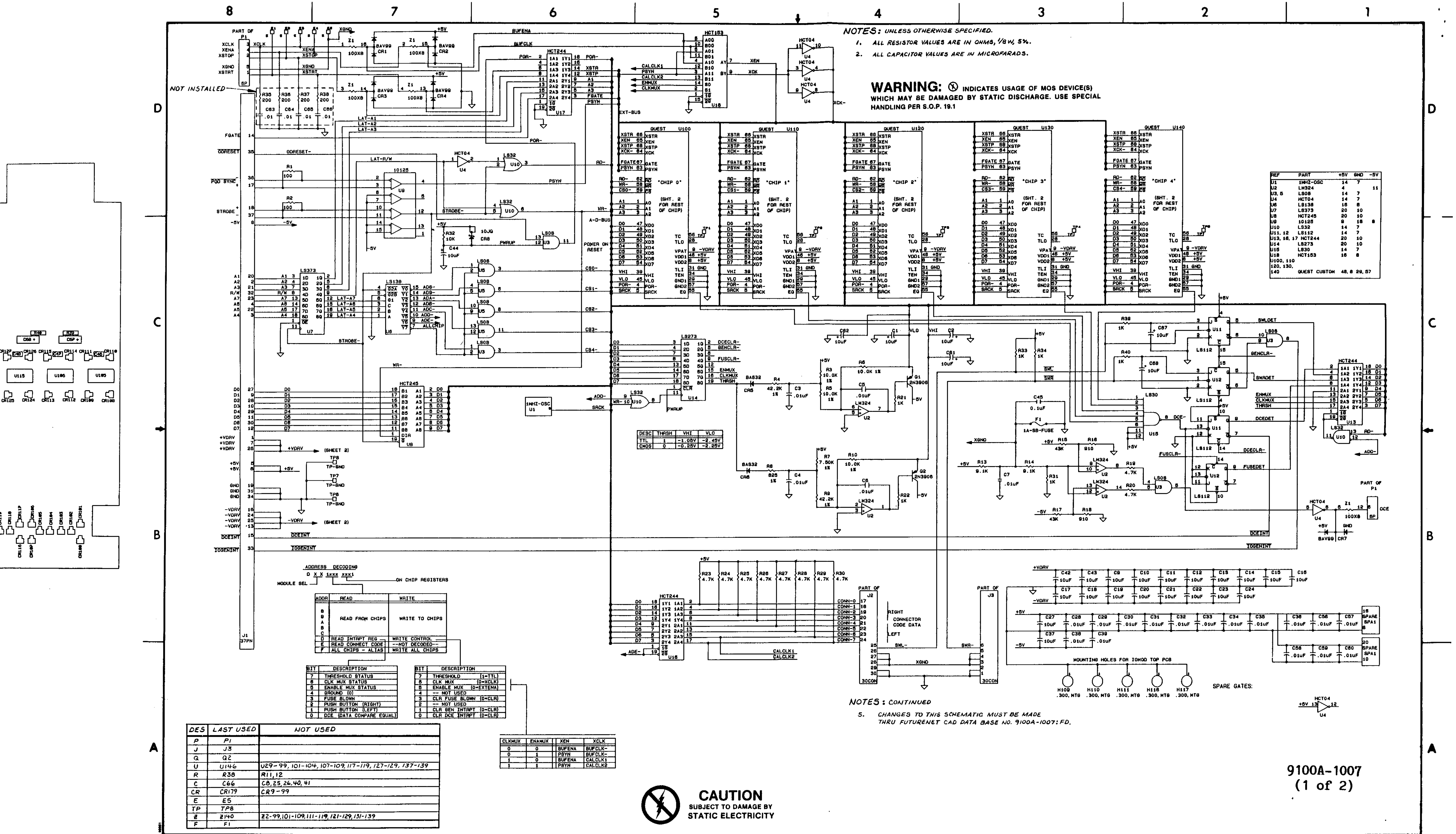
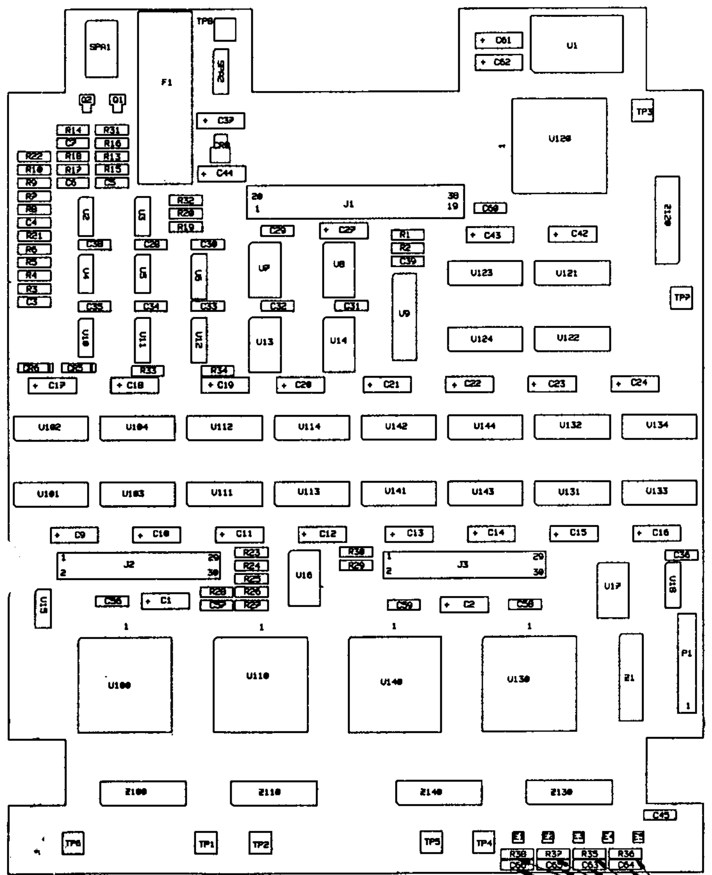
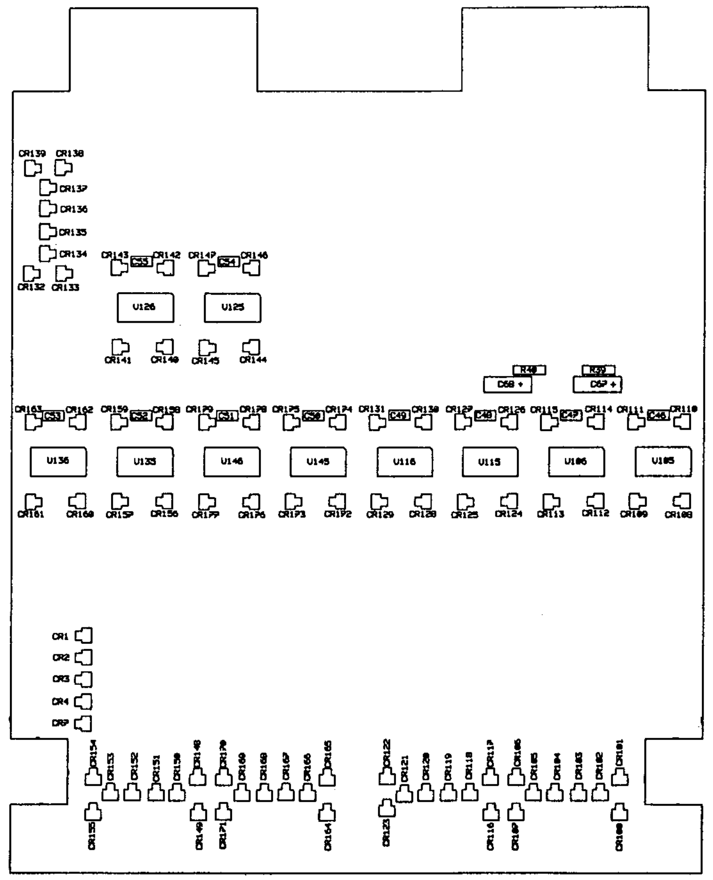


Figure 7-7. A7 I/O Module (Main) PCA



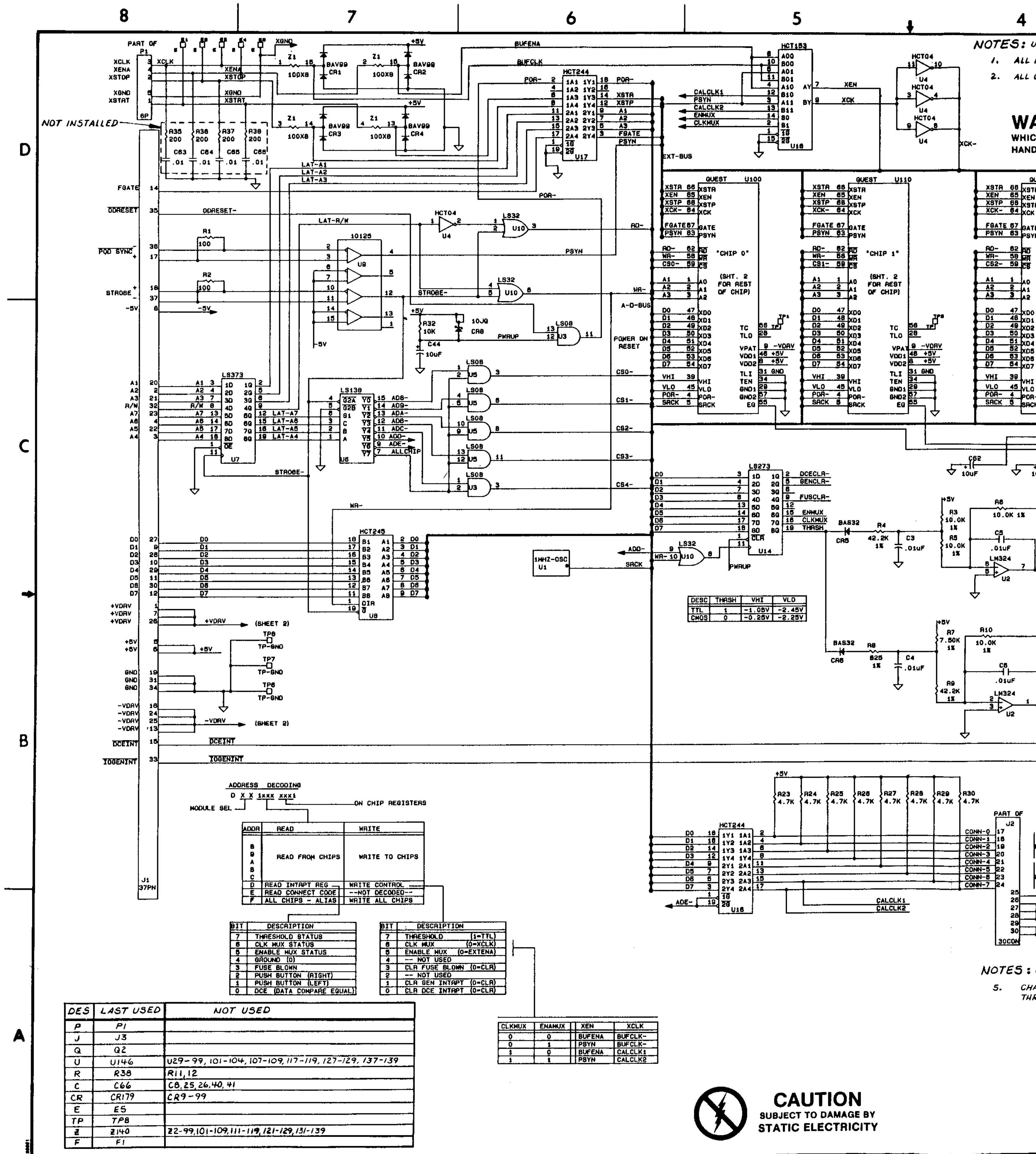
CKT 8



CKT 1

NOT INSTALLED

9100A-1607



ADDRESS DECODING

D X X 1xxx xxx1

MODULE SEL — ON CHIP REGISTERS

ADDR	READ	WRITE
8 9 A B C	READ FROM CHIPS	WRITE TO CHIPS
D	READ INTRPT REG	WRITE CONTROL
E	READ CONNECT CODE	--NOT DECODED--
F	ALL CHIPS - ALIAS	WRITE ALL CHIPS

BIT	DESCRIPTION
7	THRESHOLD STATUS
6	CLK MUX STATUS
5	ENABLE MUX STATUS
4	GROUND (0)
3	FUSE BLOWN
2	PUSH BUTTON (RIGHT)
1	PUSH BUTTON (LEFT)
0	DCE (DATA COMPARE EQUAL)

BIT	DESCRIPTION
7	THRESHOLD (1=TTL)
6	CLK MUX (0=XCLK)
5	ENABLE MUX (0=EXTENA)
4	-- NOT USED
3	CLR FUSE BLOWN (0=CLR)
2	-- NOT USED
1	CLR GEN INTRPT (0=CLR)
0	CLR DCE INTRPT (0=CLR)

CLKMUX	ENAMUX	XEN	XCLK
0	0	BUFENA	BUFCLK-
0	1	PSYN	BUFCLK-
1	0	BUFENA	CALCLK1
1	1	PSYN	CALCLK2

DESC	THRSH	VHI	VLO
TTL	1	-1.05V	-2.45V
CMOS	0	-0.25V	-2.25V

DES	LAST USED	NOT USED
P	P1	
J	J3	
Q	Q2	
U	U146	U29-99, 101-104, 107-109, 117-119, 127-129, 137-139
R	R38	R11, 12
C	C66	C8, 25, 26, 40, 41
CR	CR179	CR9-99
E	E5	
TP	TP8	
Z	Z140	Z2-99, 101-109, 111-119, 121-129, 131-139
F	F1	

CAUTION
SUBJECT TO DAMAGE BY STATIC ELECTRICITY

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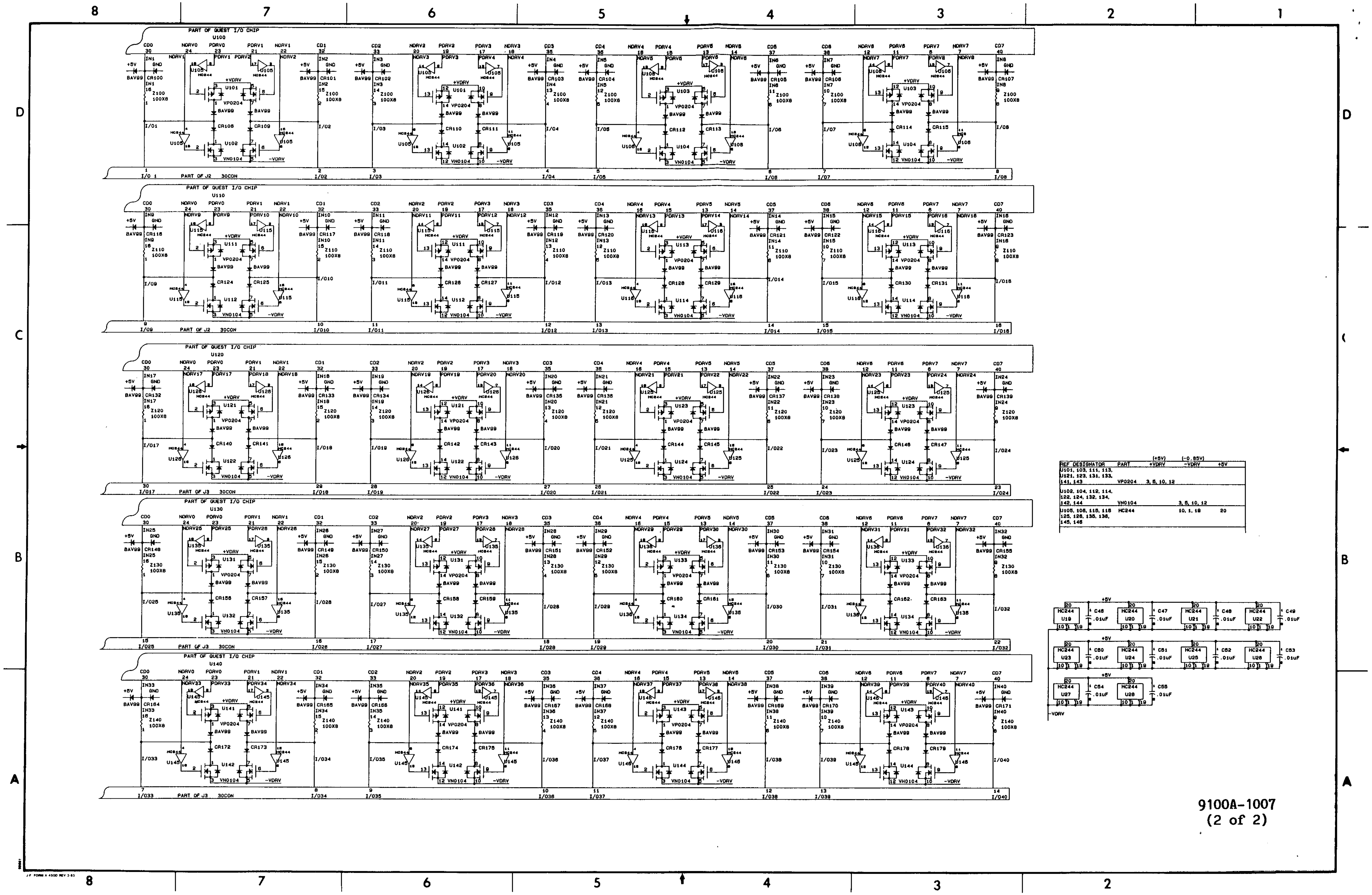
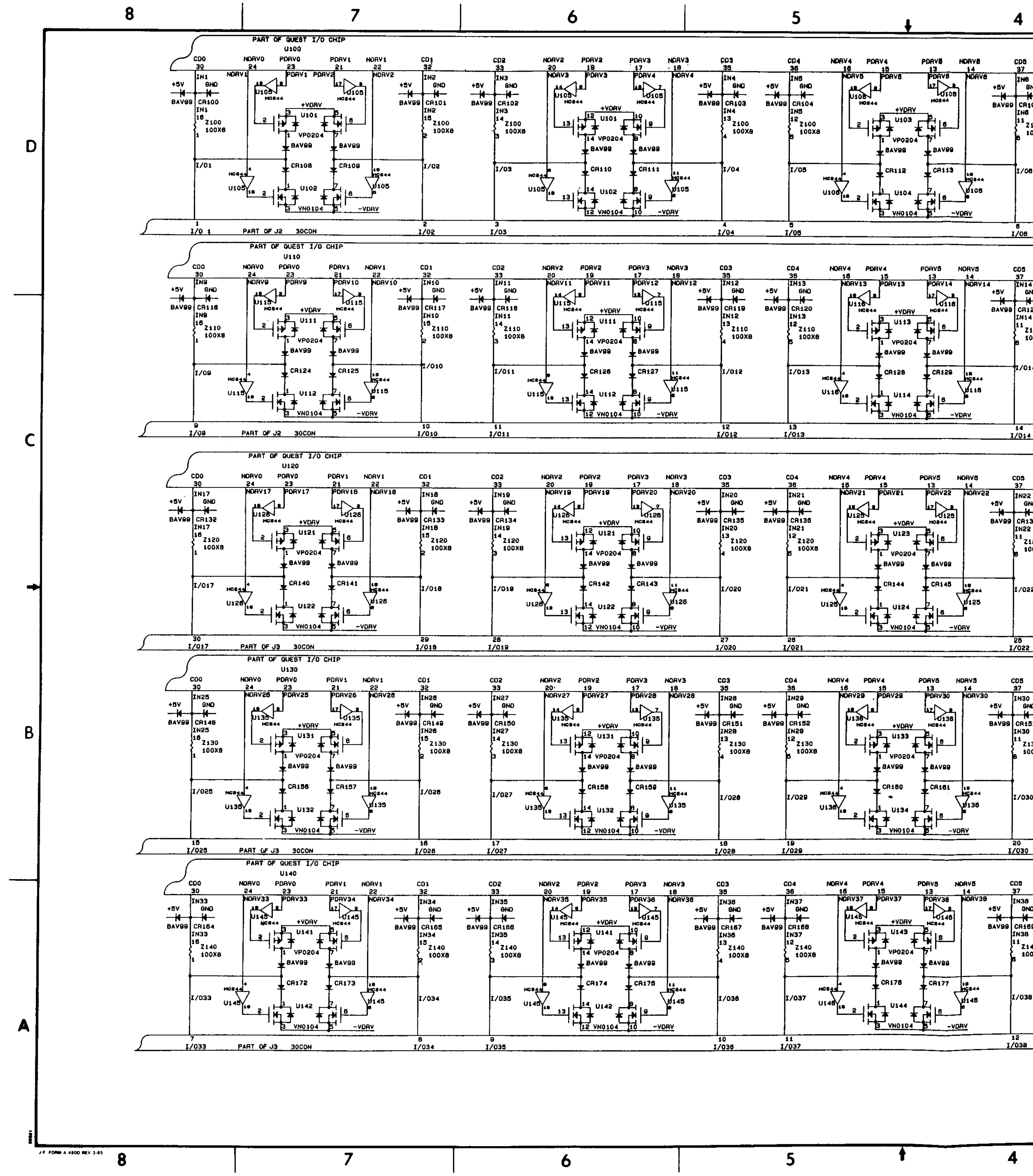


Figure 7-7. A7 I/O Module (Main) PCA (cont.)



PART OF QUEST I/O CHIP
U100
U110
U120
U130
U140
PART OF J2 30CON
PART OF J3 30CON
8
7
6
5
4
D
C
B
A

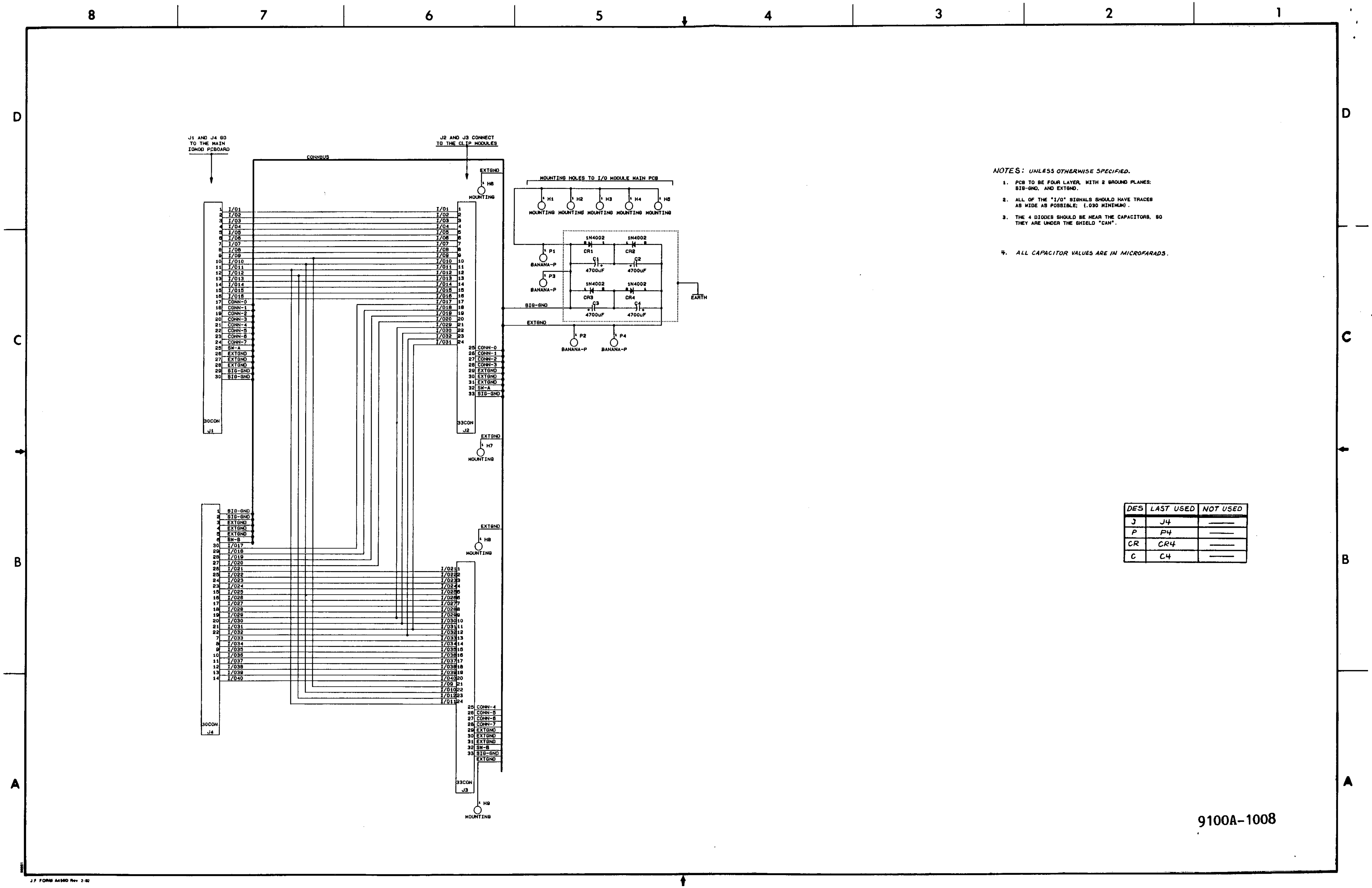
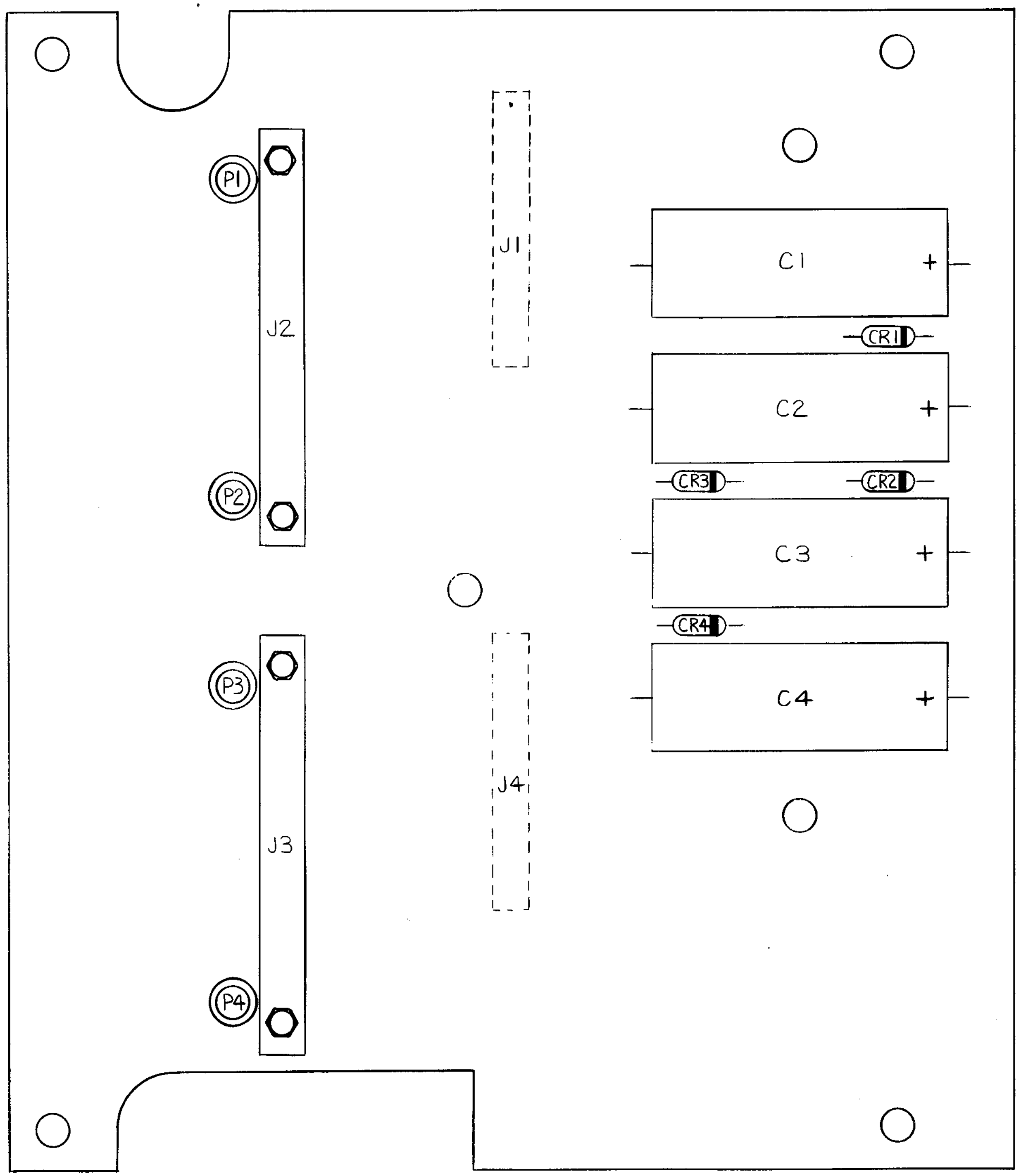
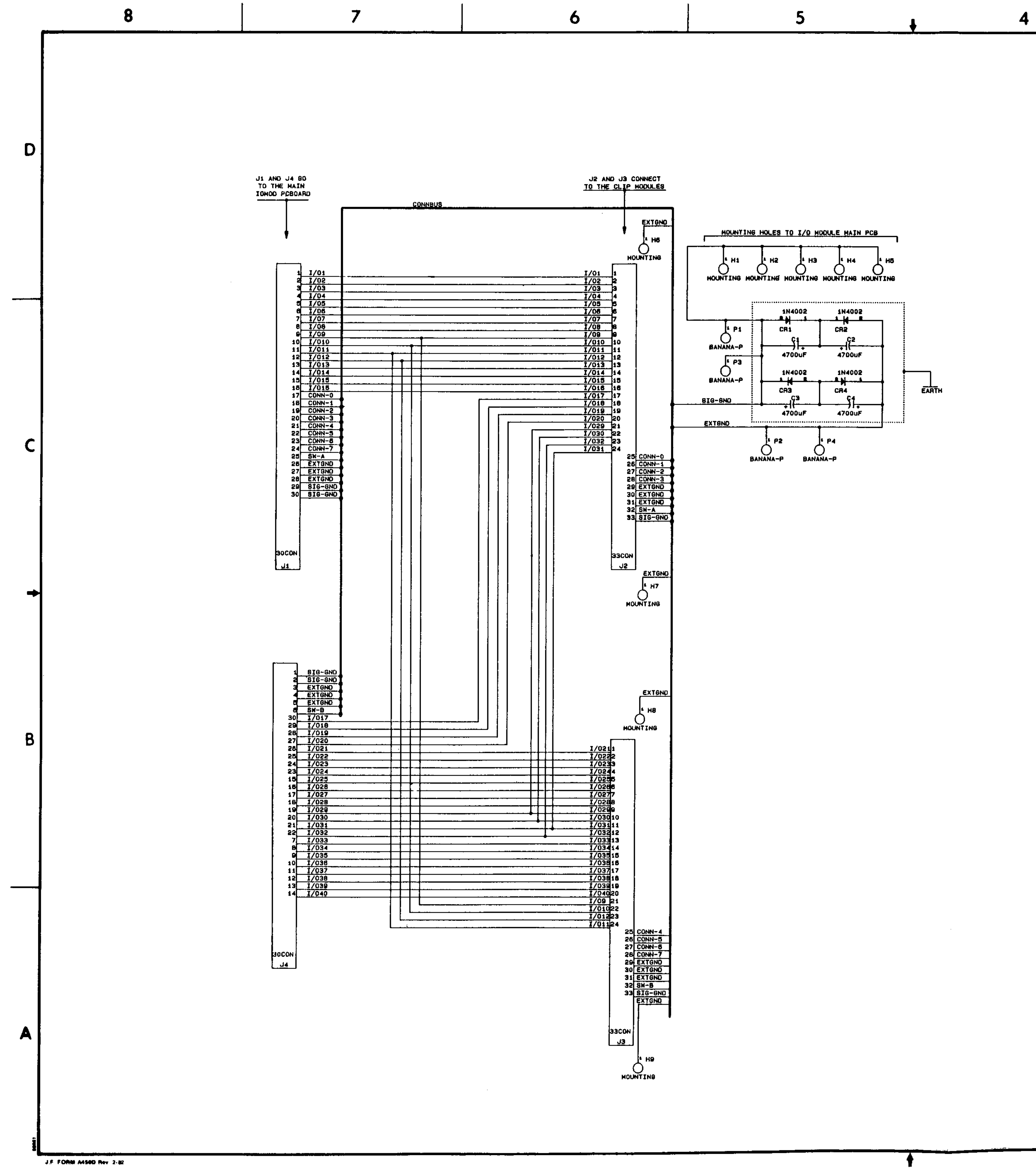
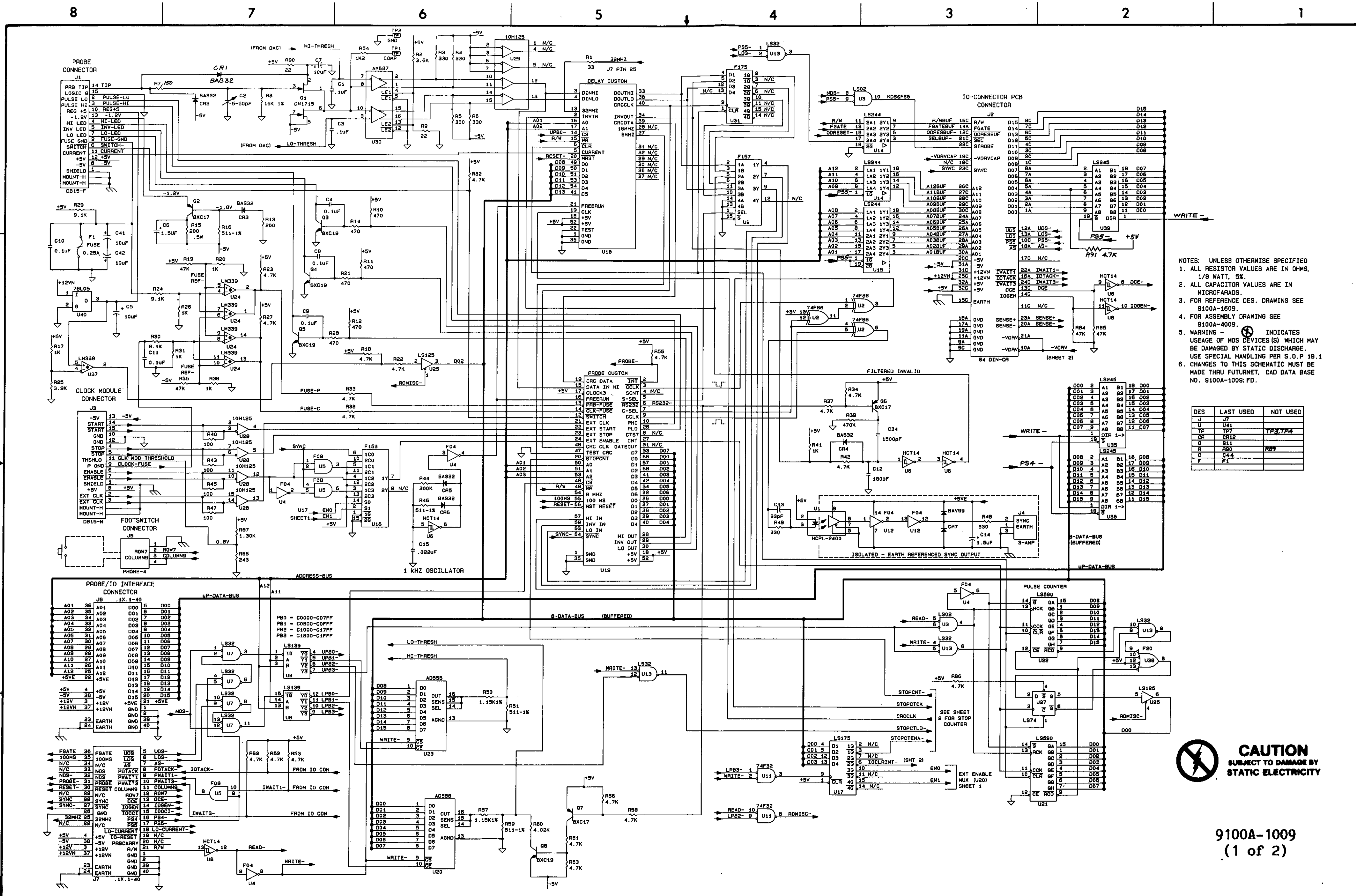


Figure 7-8. A8 I/O Module (Top) PCA


P1
P2
P3
P4
J1
J2
J3
J4
C1
C2
C3
C4
CR1
CR2
CR3
CR4

9100A-1608


8
7
6
5
4
D
C
B
A
J1 AND J4 GO TO THE MAIN IOMOD PCBOARD
J2 AND J3 CONNECT TO THE CLIP MODULES
CONNBUS
MOUNTING HOLES TO I/O MODULE MAIN PCB
EARTH
J1
J2
J3
J4

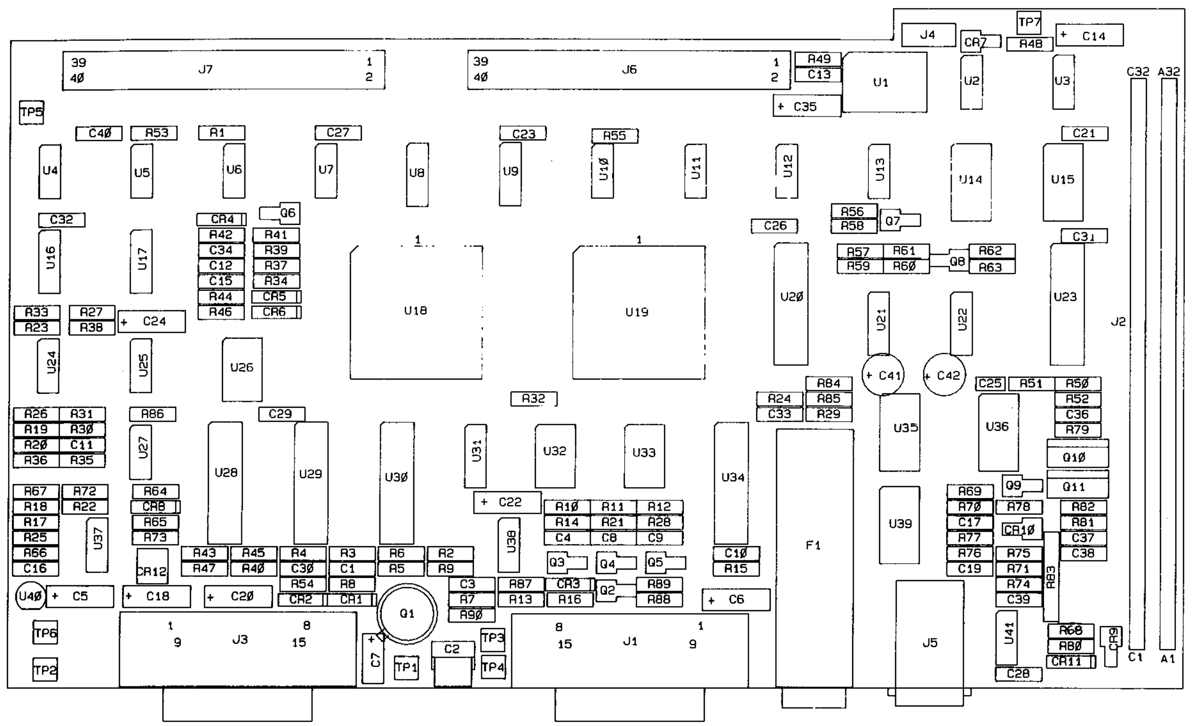


NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS, 1/8 WATT, 5%.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
3. FOR REFERENCE DES. DRAWING SEE 9100A-1609.
4. FOR ASSEMBLY DRAWING SEE 9100A-4009.
5. WARNING - INDICATES USEAGE OF MOS DEVICES (S) WHICH MAY BE DAMAGED BY STATIC DISCHARGE. USE SPECIAL HANDLING PER S.O.P 19.1
6. CHANGES TO THIS SCHEMATIC MUST BE MADE THRU FUTURNET, CAD DATA BASE NO. 9100A-1009: FD.

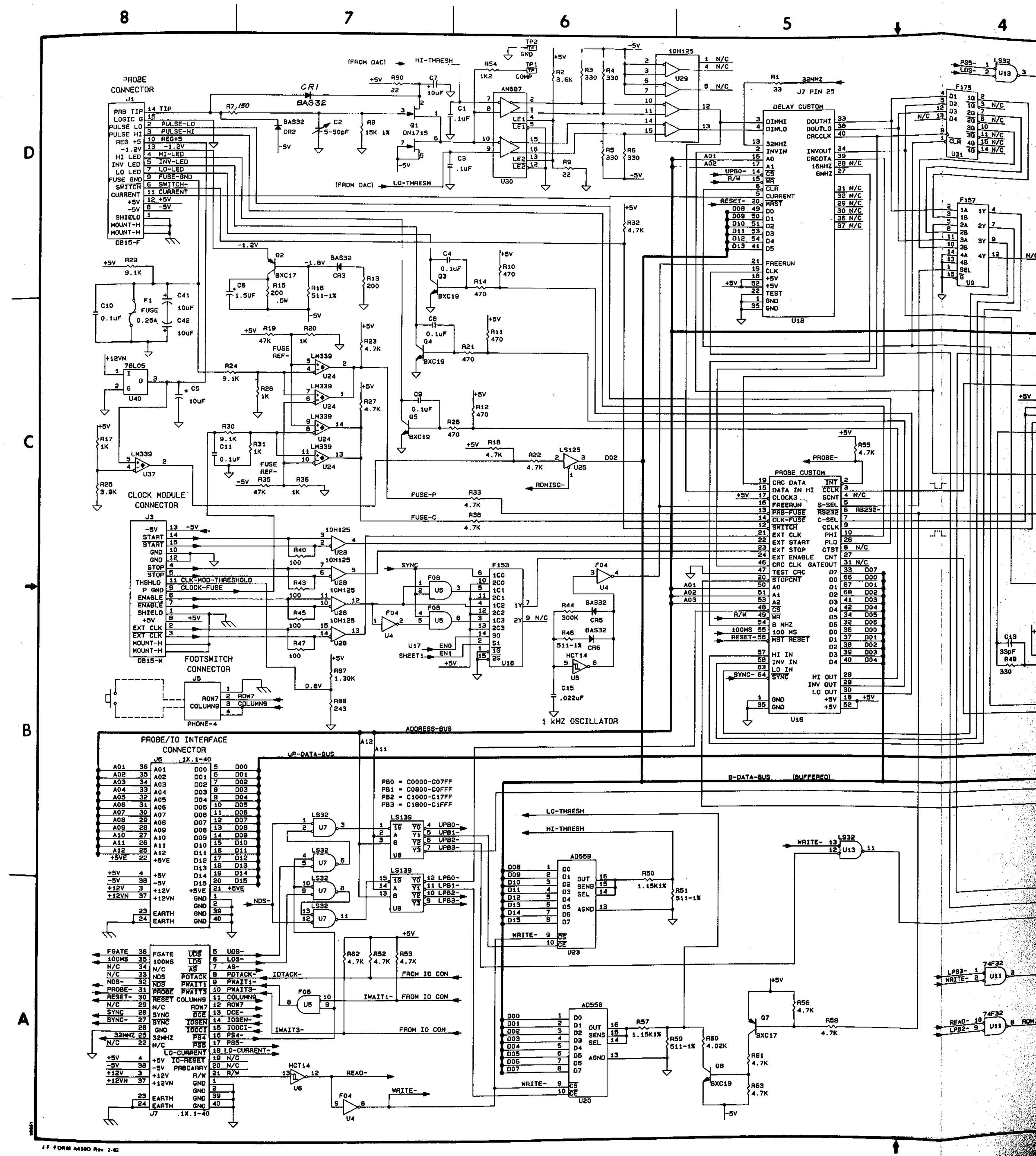
DES	LAST USED	NOT USED
J	J7	
U	U41	
TP	TP7	TP3,TP4
CR	CR12	
Q	Q11	
R	R90	R89
C	C44	
F	F1	

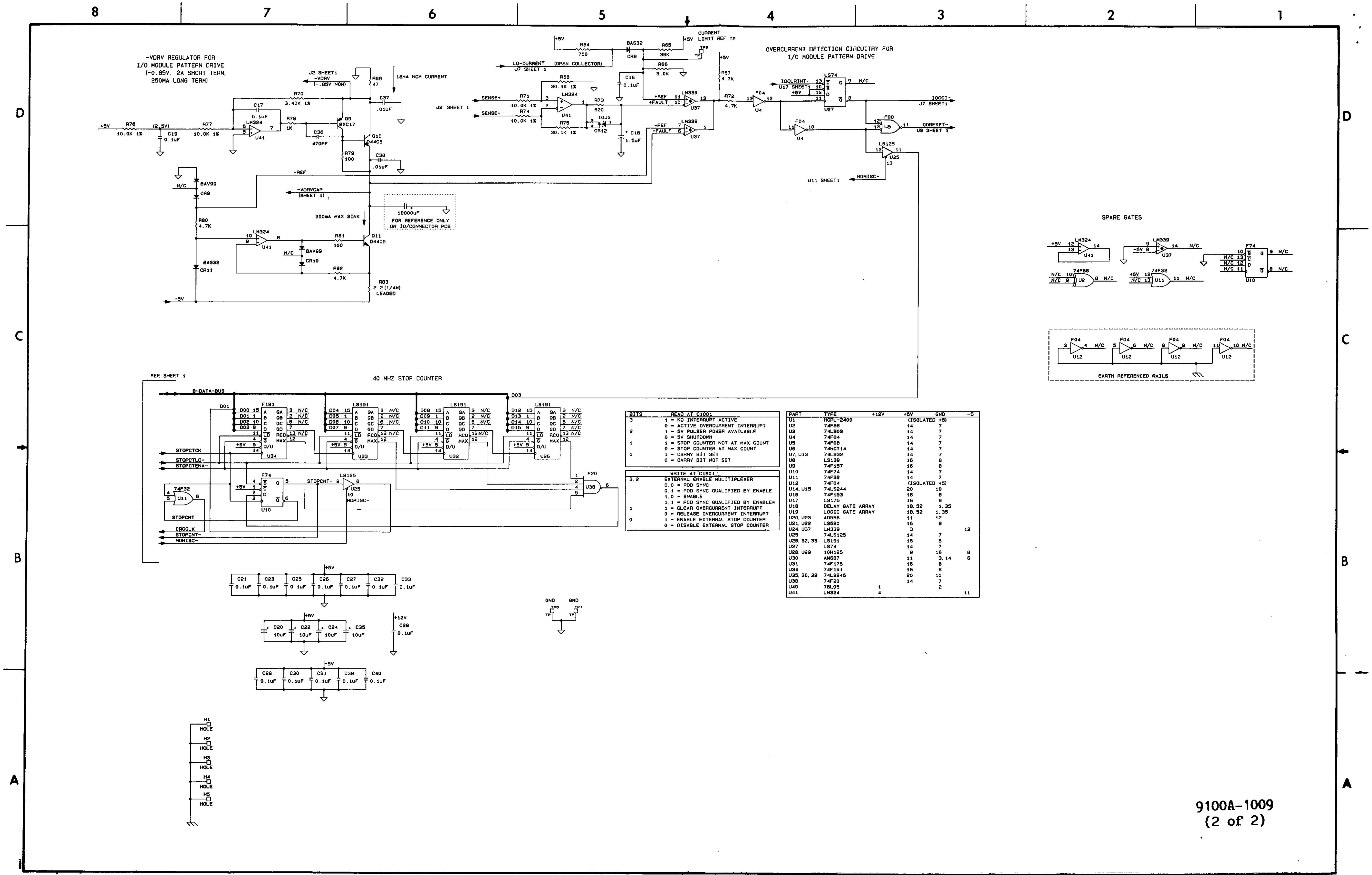
9100A-1009
(1 of 2)

Figure 7-9. A9 Probe I/O PCA



9100A-1609


PROBE CONNECTOR
CLOCK MODULE CONNECTOR
FOOTSWITCH CONNECTOR
PROBE/IO INTERFACE CONNECTOR
1 KHZ OSCILLATOR
DELAY CUSTOM
PROBE CUSTOM
ADDRESS-BUS
uP-DATA-BUS
B-DATA-BUS (BUFFERED)

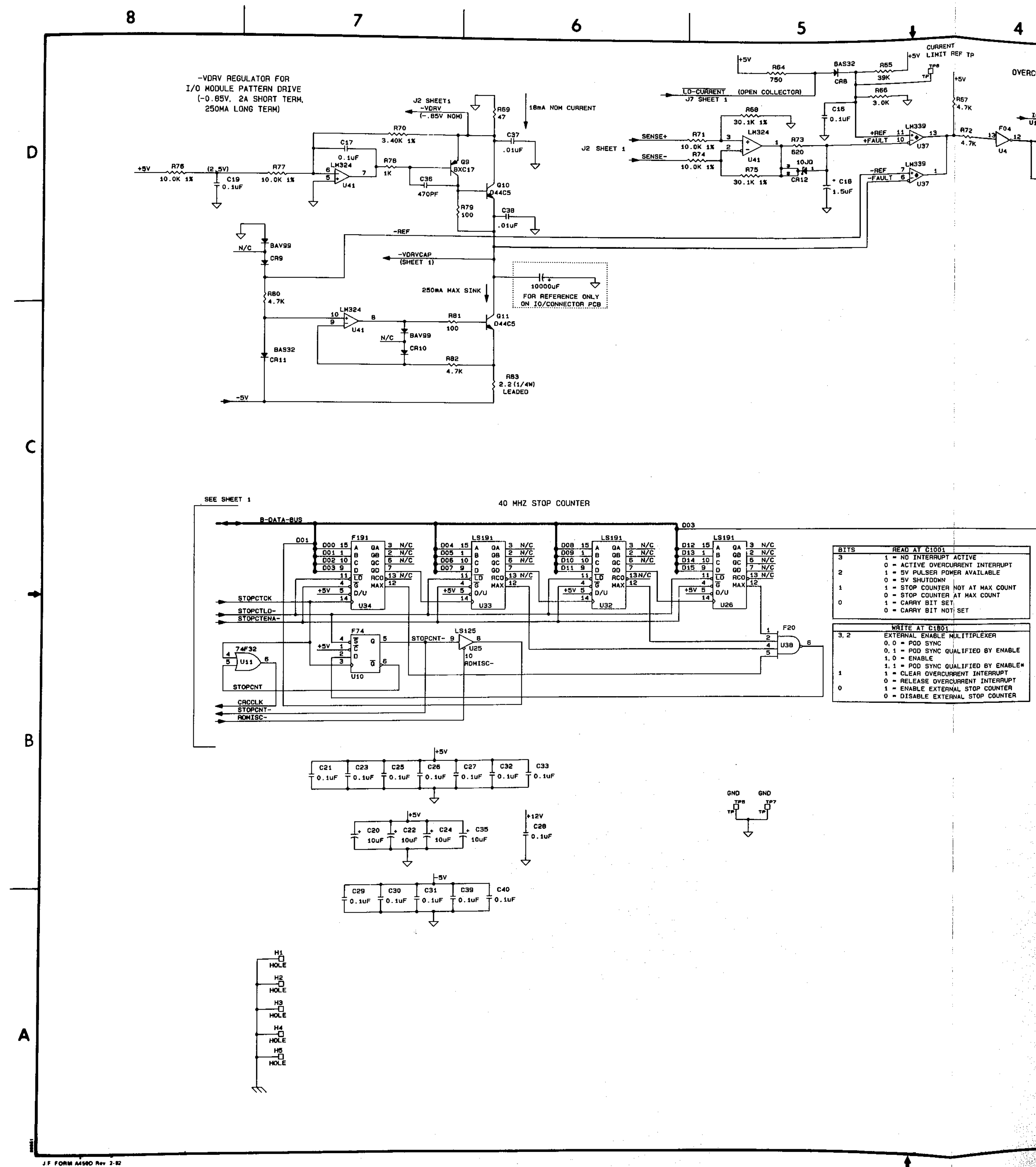


BITS	READ AT C1001
3	1 = NO INTERRUPT ACTIVE
	0 = ACTIVE OVERCURRENT INTERRUPT
2	1 = 5V PULSER POWER AVAILABLE
	0 = 5V SHUTDOWN
1	1 = STOP COUNTER NOT AT MAX COUNT
	0 = STOP COUNTER AT MAX COUNT
0	1 = CARRY BIT SET
	0 = CARRY BIT NOT SET

	WRITE AT C1801
3, 2	EXTERNAL ENABLE MULITIPLEXER
	0, 0 = POD SYNC
	0, 1 = POD SYNC QUALIFIED BY ENABLE
	1, 0 = ENABLE
	1, 1 = POD SYNC QUALIFIED BY ENABLE*
1	1 = CLEAR OVERCURRENT INTERRUPT
	0 = RELEASE OVERCURRENT INTERRUPT
0	1 = ENABLE EXTERNAL STOP COUNTER
	0 = DISABLE EXTERNAL STOP COUNTER

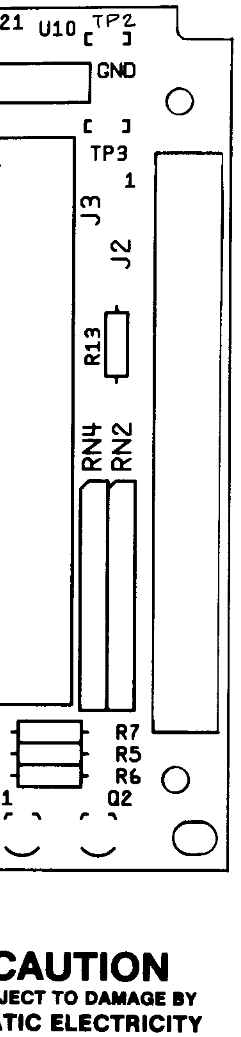
PART	TYPE	+12V	+5V	GND	-5
U1	HCPL-2400		(ISOLATED +5)		
U2	74F86		14	7	
U3	74LS02		14	7	
U4	74F04		14	7	
U5	74F08		14	7	
U6	74HCT14		14	7	
U7, U13	74LS32		14	7	
U8	LS139		16	8	
U9	74F157		16	8	
U10	74F74		14	7	
U11	74F32		14	7	
U12	74F04		(ISOLATED +5)		
U14, U15	74LS244		20	10	
U16	74F153		16	8	
U17	LS175		16	8	
U18	DELAY GATE ARRAY		18, 52	1, 35	
U19	LOGIC GATE ARRAY		18, 52	1, 35	
U20, U23	AD558		11	12	
U21, U22	LS590		16	8	
U24, U37	LM339		3		12
U25	74LS125		14	7	
U26, 32, 33	LS191		16	8	
U27	LS74		14	7	
U28, U29	10H125		9	16	8
U30	AM687		11	3, 14	6
U31	74F175		16	8	
U34	74F191		16	8	
U35, 36, 39	74LS245		20	10	
U38	74F20		14	7	
U40	78L05	1		2	
U41	LM324	4			11

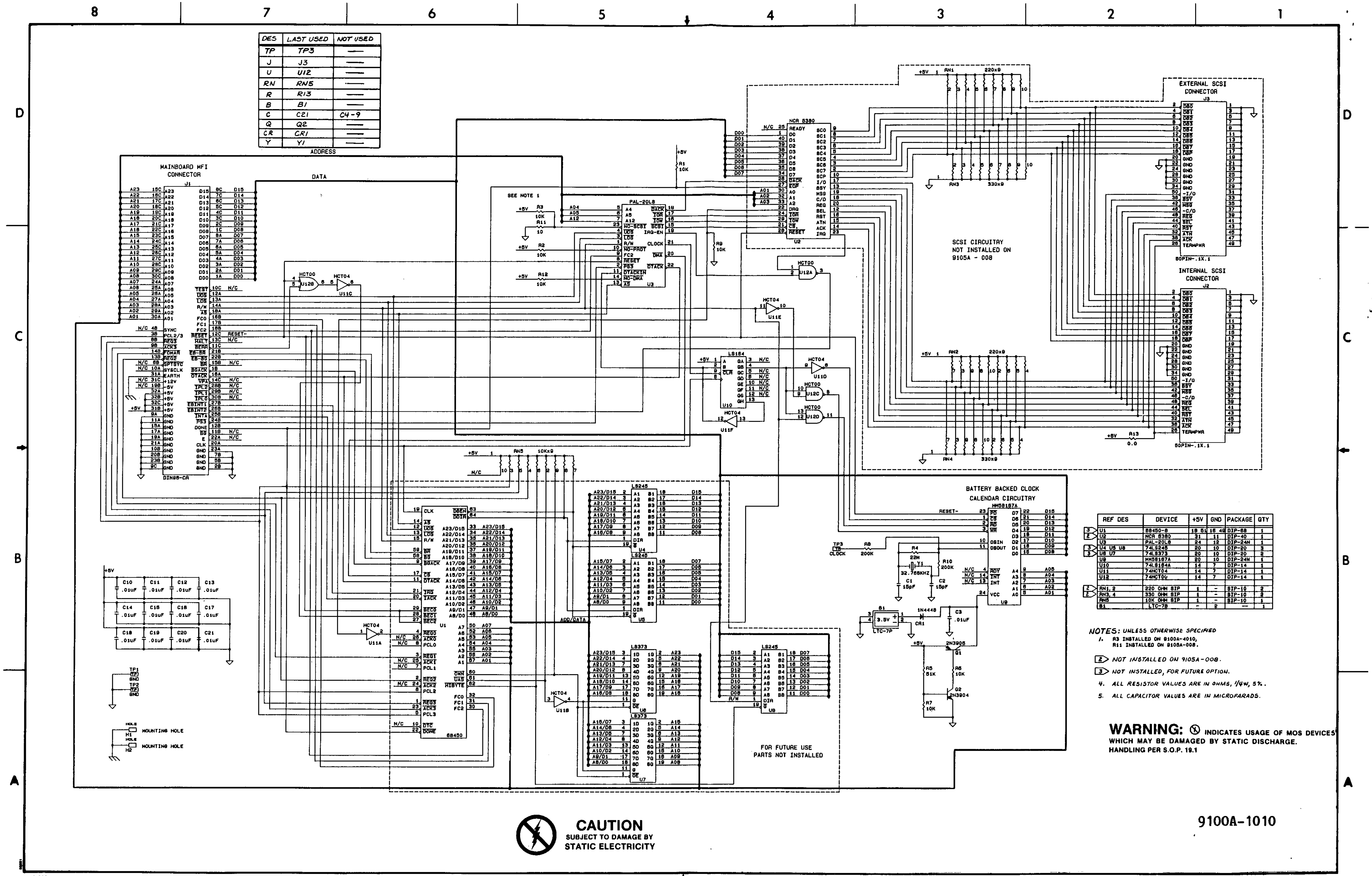
Figure 7-9. A9 Probe I/O PCA (cont.)



BITS	READ AT C1001
3	1 = NO INTERRUPT ACTIVE
	0 = ACTIVE OVERCURRENT INTERRUPT
2	1 = 5V PULSER POWER AVAILABLE
	0 = 5V SHUTDOWN
1	1 = STOP COUNTER NOT AT MAX COUNT
	0 = STOP COUNTER AT MAX COUNT
0	1 = CARRY BIT SET
	0 = CARRY BIT NOT SET

	WRITE AT C1801
3, 2	EXTERNAL ENABLE MULITIPLEXER
	0, 0 = POD SYNC
	0, 1 = POD SYNC QUALIFIED BY ENABLE
	1, 0 = ENABLE
	1, 1 = POD SYNC QUALIFIED BY ENABLE*
1	1 = CLEAR OVERCURRENT INTERRUPT
	0 = RELEASE OVERCURRENT INTERRUPT
0	1 = ENABLE EXTERNAL STOP COUNTER
	0 = DISABLE EXTERNAL STOP COUNTER





DES	LAST USED	NOT USED
TP	TP3	—
J	J3	—
U	U12	—
RN	RN5	—
R	R13	—
B	B1	—
C	C21	C4-9
Q	Q2	—
CR	CR1	—
Y	Y1	—

REF DES	DEVICE	+5V	GND	PACKAGE	QTY
3 U1	68450-8	18 51	16 49	DIP-68	1
2 U2	NCR 5380	31	11	DIP-40	1
U3	PAL-20L8	24	12	DIP-24N	1
3 U4 U5 U8	74LS245	20	10	DIP-20	3
3 U6 U7	74LS373	20	10	DIP-20	2
U9	MM58167A	20	10	DIP-24W	1
U10	74LS164A	14	7	DIP-14	1
U11	74HCT04	14	7	DIP-14	1
U12	74HCT00	14	7	DIP-14	1
2 RN1, 2	220 OHM SIP	1	-	SIP-10	2
2 RN3, 4	330 OHM SIP	1	-	SIP-10	2
RN5	10K OHM SIP	1	-	SIP-10	1
B1	LTC-7B	-	2	--	1

NOTES: UNLESS OTHERWISE SPECIFIED

1. R3 INSTALLED ON 9100A-4010, R11 INSTALLED ON 9105A-008.

2 NOT INSTALLED ON 9105A-008.

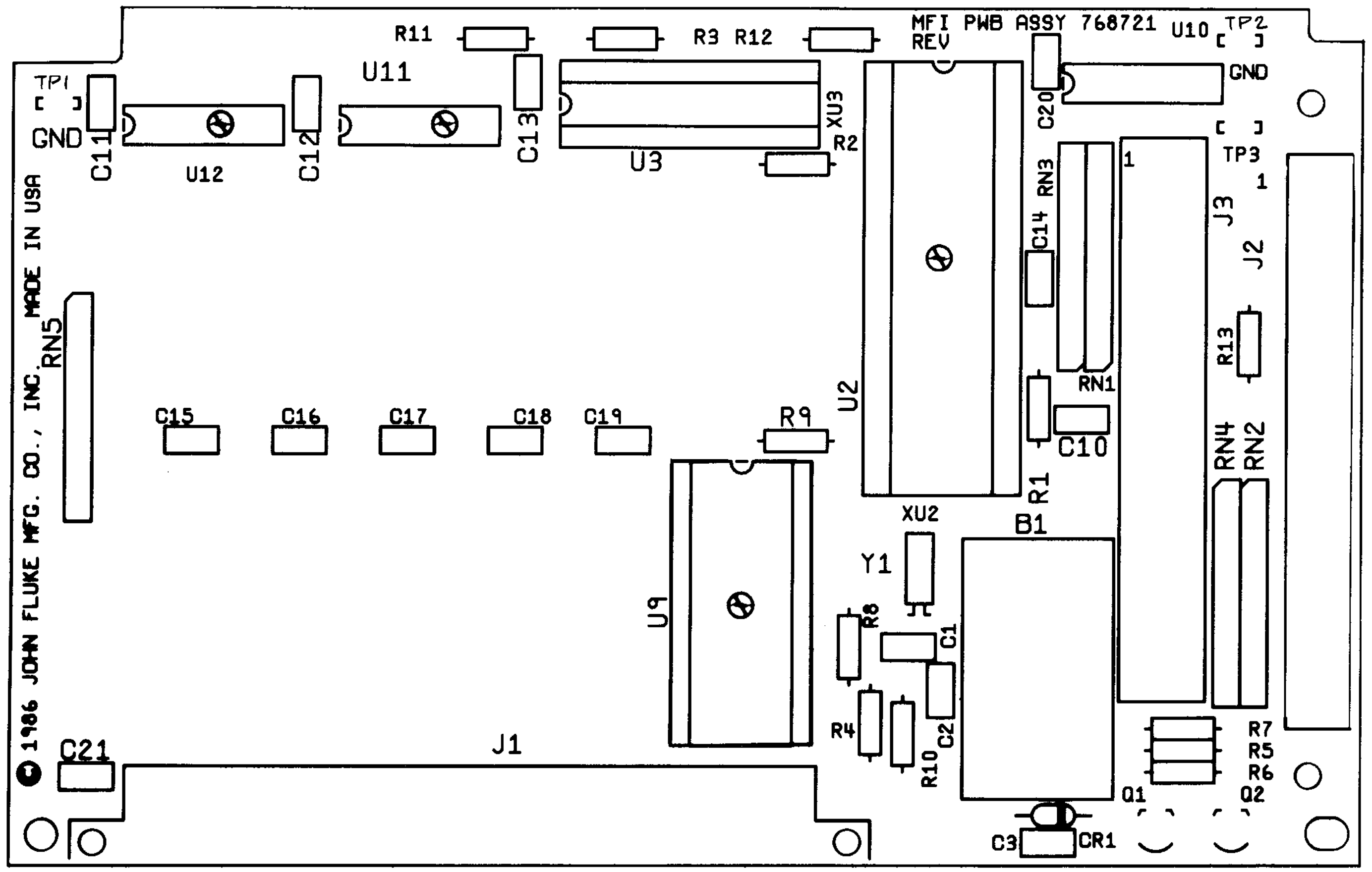
3 NOT INSTALLED, FOR FUTURE OPTION.

4. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.

5. ALL CAPACITOR VALUES ARE IN MICROFARADS.

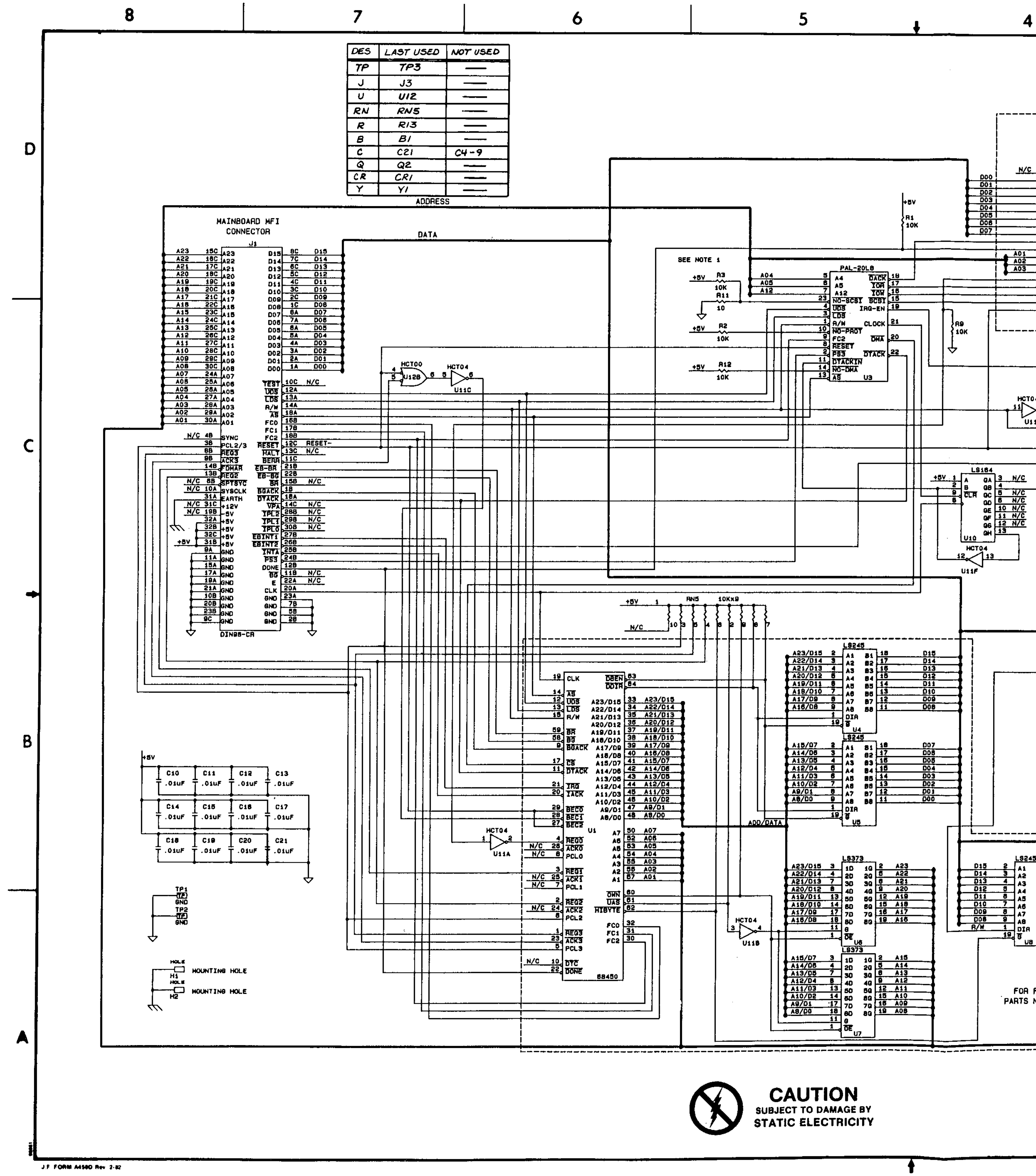
WARNING: INDICATES USAGE OF MOS DEVICES WHICH MAY BE DAMAGED BY STATIC DISCHARGE. HANDLING PER S.O.P. 19.1

Figure 7-10. A10 Multi-Function Interface PCA

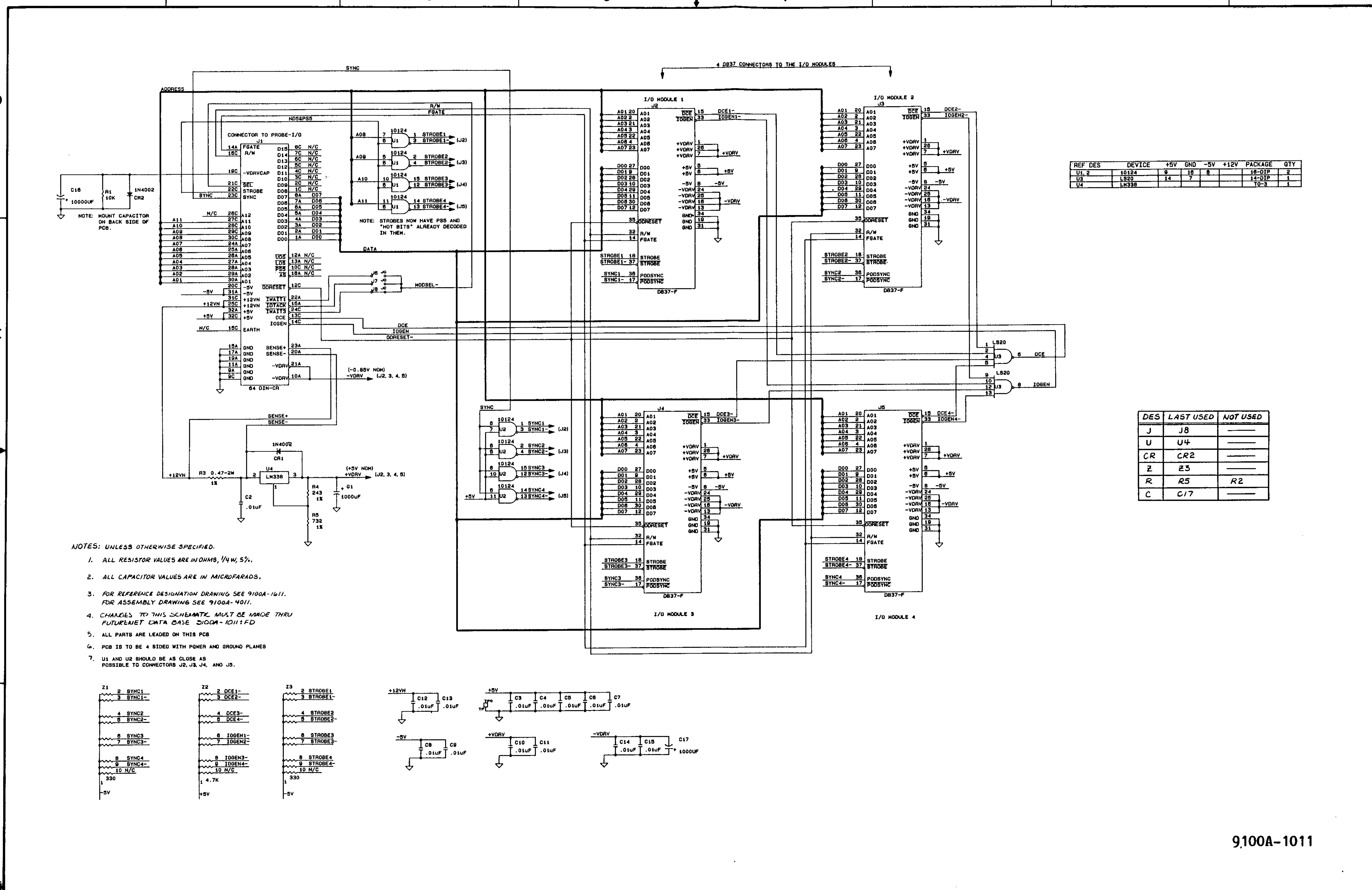


9100A-1610

CAUTION
SUBJECT TO DAMAGE BY
STATIC ELECTRICITY



DES	LAST USED	NOT USED
TP	TP3	—
J	J3	—
U	U12	—
RN	RN5	—
R	R13	—
B	B1	—
C	C21	C4-9
Q	Q2	—
CR	CR1	—
Y	Y1	—



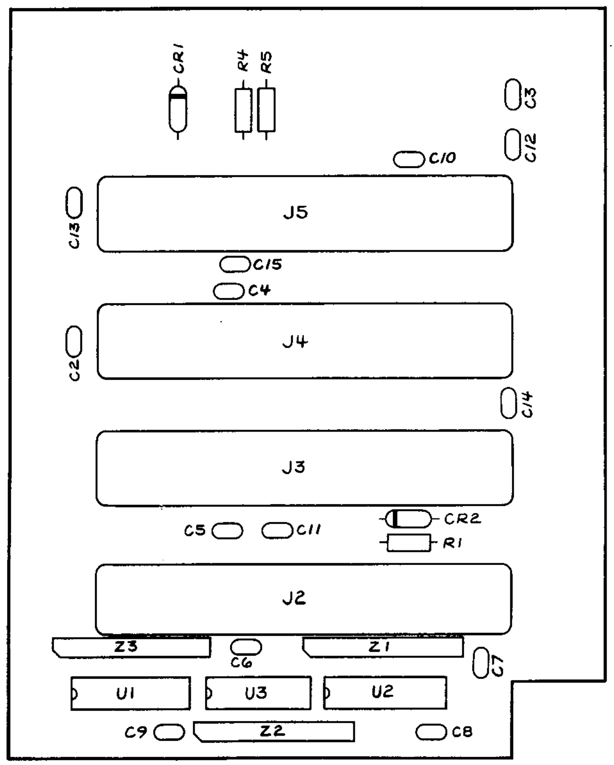
REF DES	DEVICE	+5V	GND	-5V	+12V	PACKAGE	QTY
U1, 2	10124	9	16	8		16-DIP	2
U3	LS20	14	7			14-DIP	1
U4	LM338					TO-3	1

DES	LAST USED	NOT USED
J	J8	———
U	U4	———
CR	CR2	———
Z	Z3	———
R	R5	R2
C	C17	———

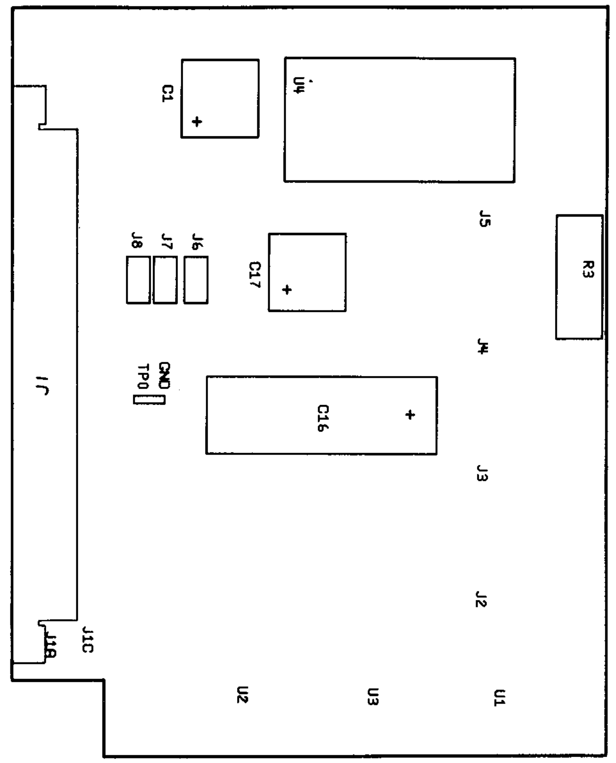
NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL RESISTOR VALUES ARE IN OHMS, 1/4 W, 5%.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
3. FOR REFERENCE DESIGNATION DRAWING SEE 9100A-1611. FOR ASSEMBLY DRAWING SEE 9100A-4011.
4. CHANGES TO THIS SCHEMATIC MUST BE MADE THRU FUTURENET DATA BASE 9100A-1011:FD
5. ALL PARTS ARE LEADED ON THIS PCB
6. PCB IS TO BE 4 SIDED WITH POWER AND GROUND PLANES
7. U1 AND U2 SHOULD BE AS CLOSE AS POSSIBLE TO CONNECTORS J2, J3, J4, AND J5.

Figure 7-11. A11 I/O Connector PCA

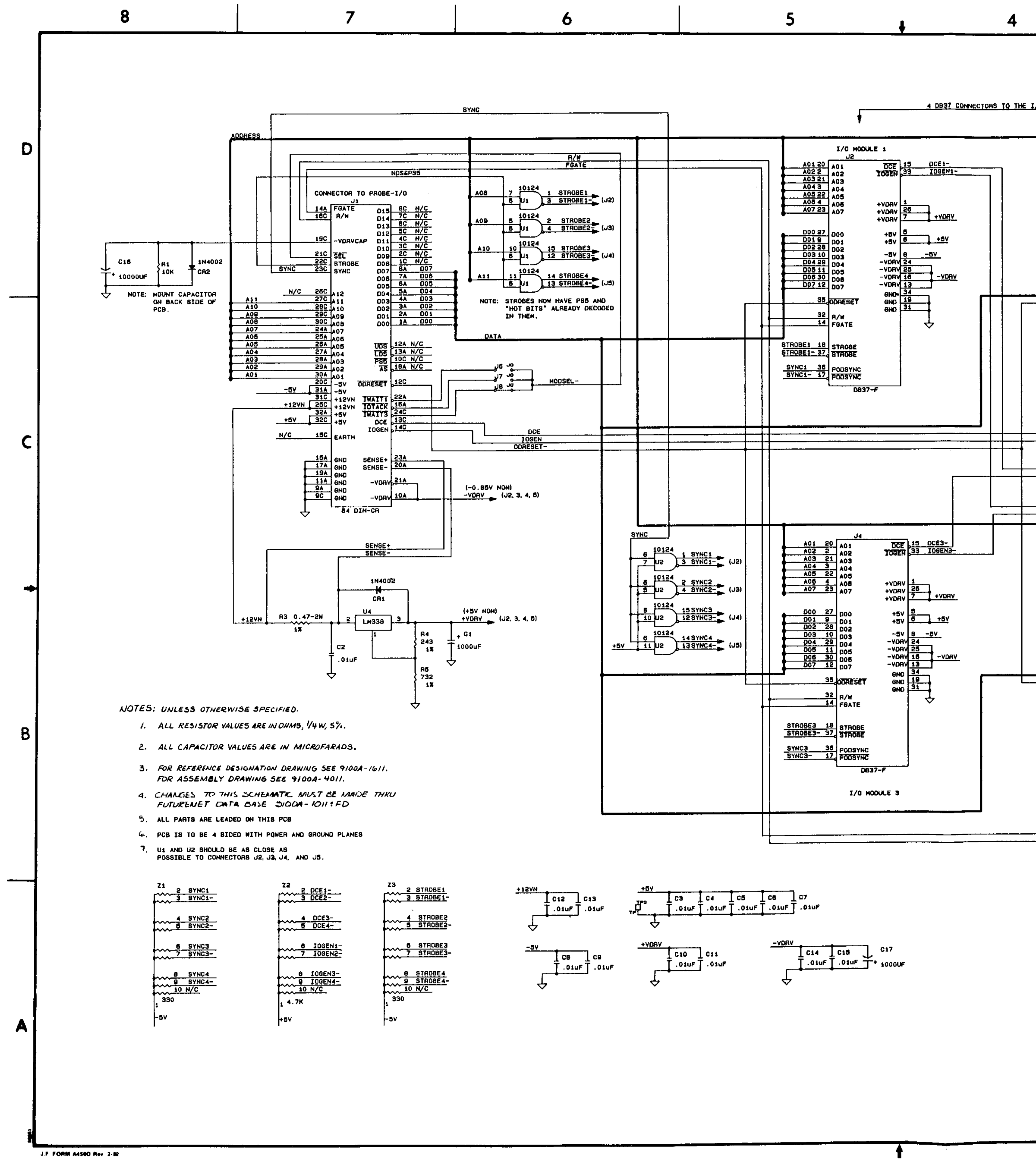


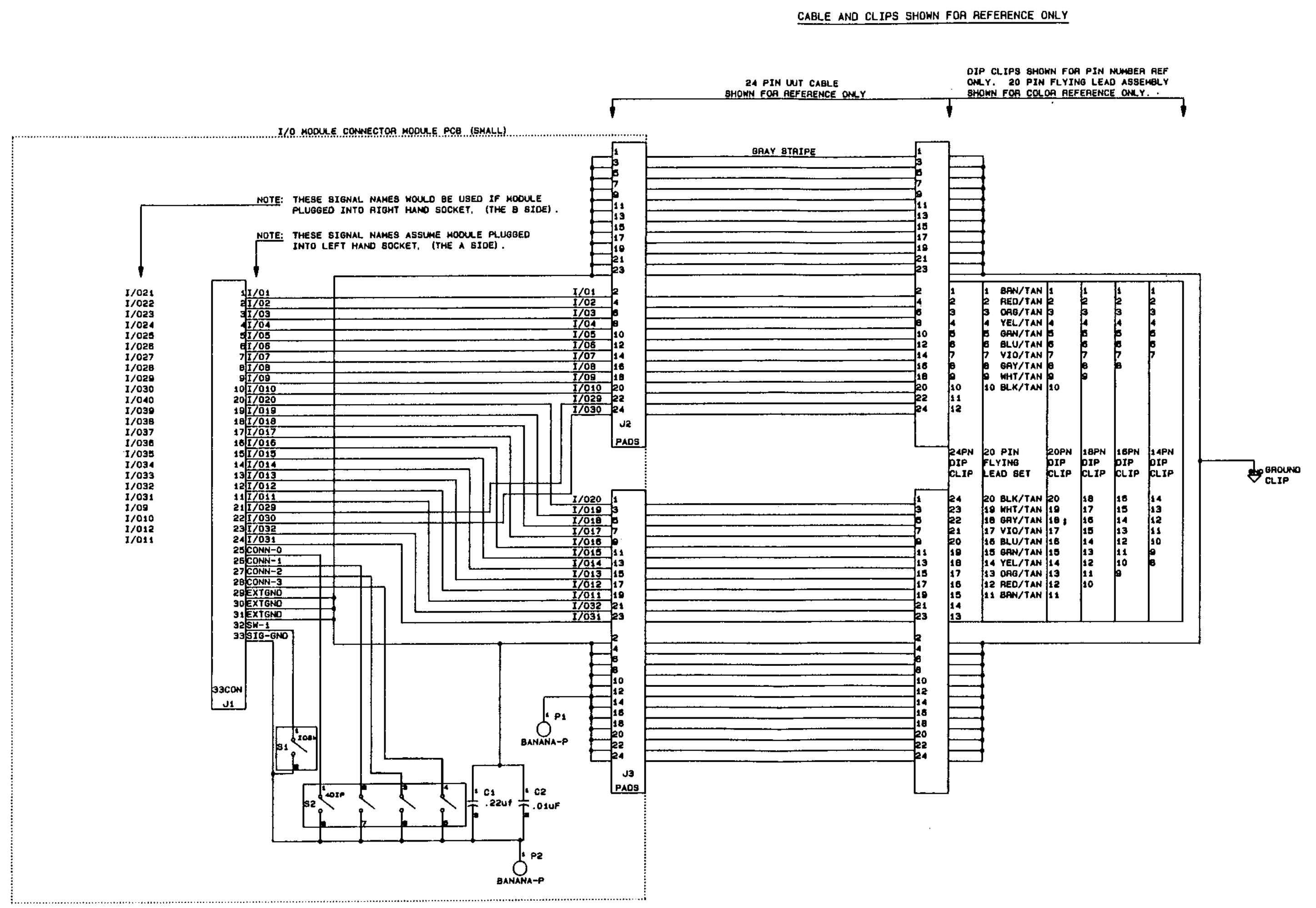
CKT 4 SIDE



CKT 1 SIDE

9100A-1611



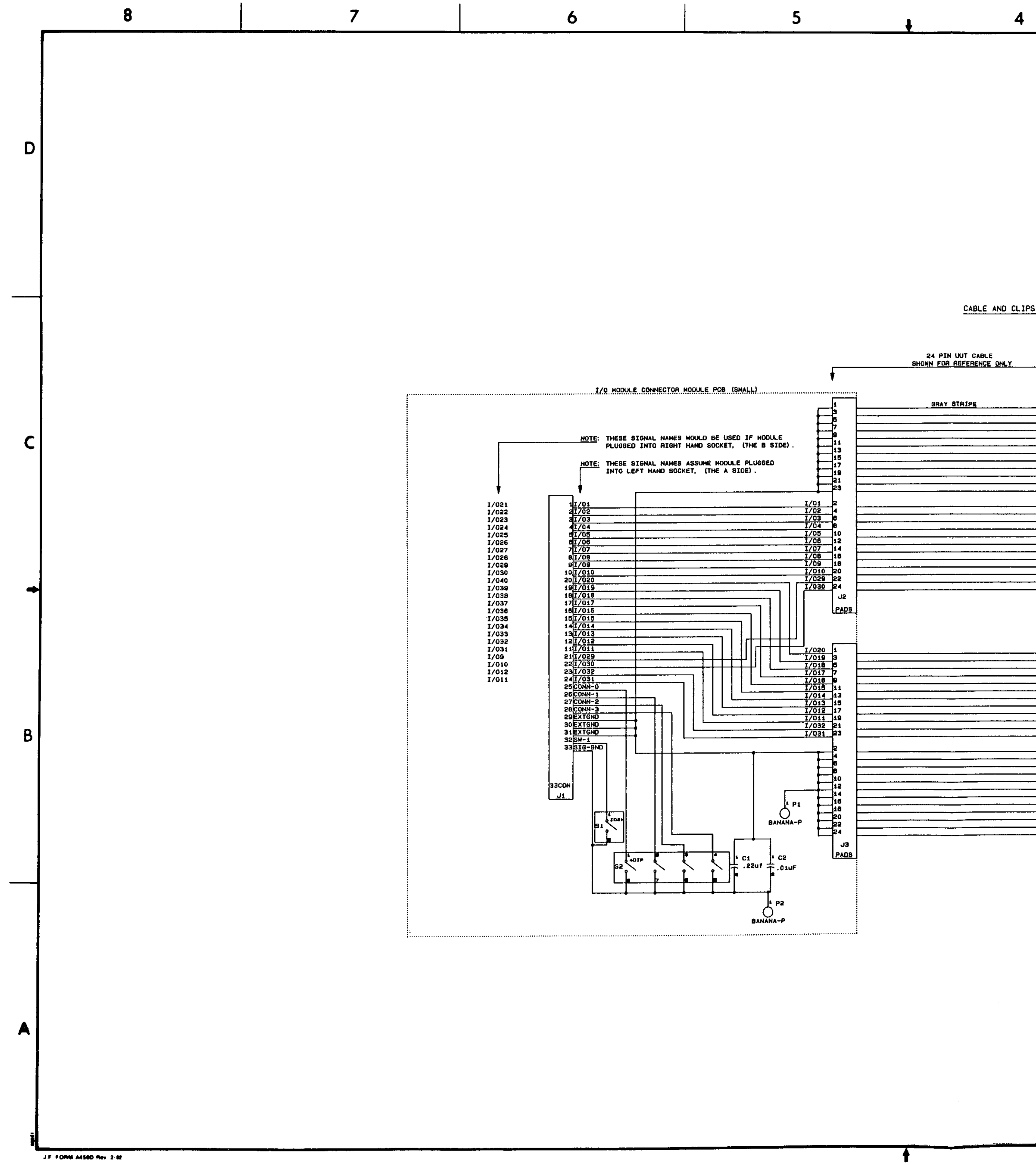


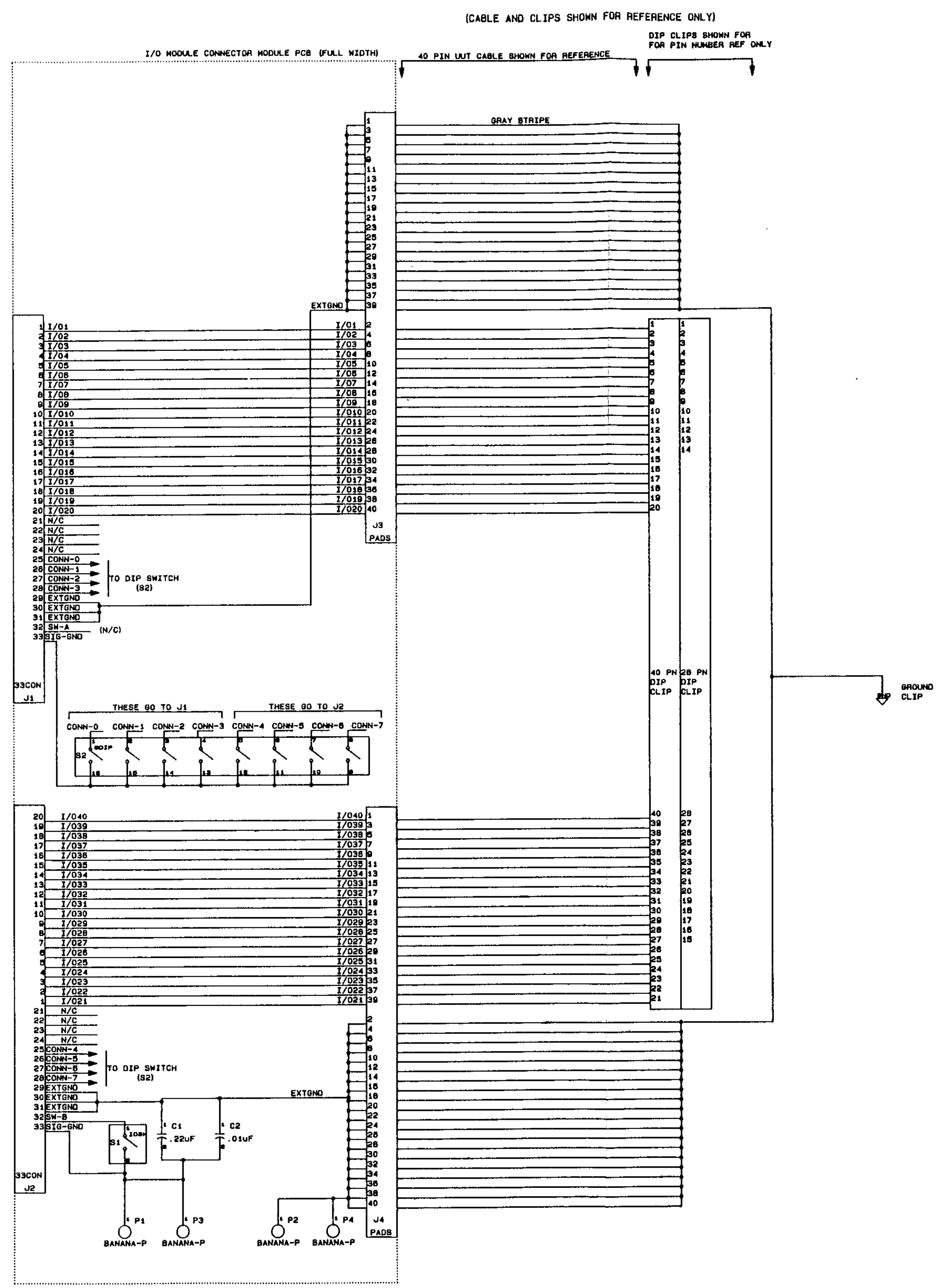
NOTES: UNLESS OTHERWISE SPECIFIED.

1. J2 AND J3 ARE REALLY ARRAYS OF SOLDER PADS WHERE THE CABLE ASSEMBLY WILL SOLDER IN.
2. SWITCH S1 IS THE "IO" SWITCH, ACCESSIBLE FROM THE OUTSIDE OF THE MODULE.
3. ALL RESISTOR VALUES ARE IN OHMS, 1/8 W, 5%.
4. ALL CAPACITOR VALUES ARE IN MICROFARADS.

DES	LAST USED	NOT USED
J	J3	—
P	P2	—
S	S2	—
C	C2	—

Figure 7-12. A12 DIP Clip Module (Half)


8
7
6
5
4
D
C
B
A
CABLE AND CLIPS
24 PIN UUT CABLE SHOWN FOR REFERENCE ONLY
I/O MODULE CONNECTOR MODULE PCB (SMALL)
GRAY STRIPE
NOTE: THESE SIGNAL NAMES WOULD BE USED IF MODULE PLUGGED INTO RIGHT HAND SOCKET. (THE B SIDE).
NOTE: THESE SIGNAL NAMES ASSUME MODULE PLUGGED INTO LEFT HAND SOCKET. (THE A SIDE).
33CON
J1
J2
PADS
J3
PADS
S1
S2
C1 .22uf
C2 .01uF
P1 BANANA-P
P2 BANANA-P
J F FORM A4560 Rev 2-82



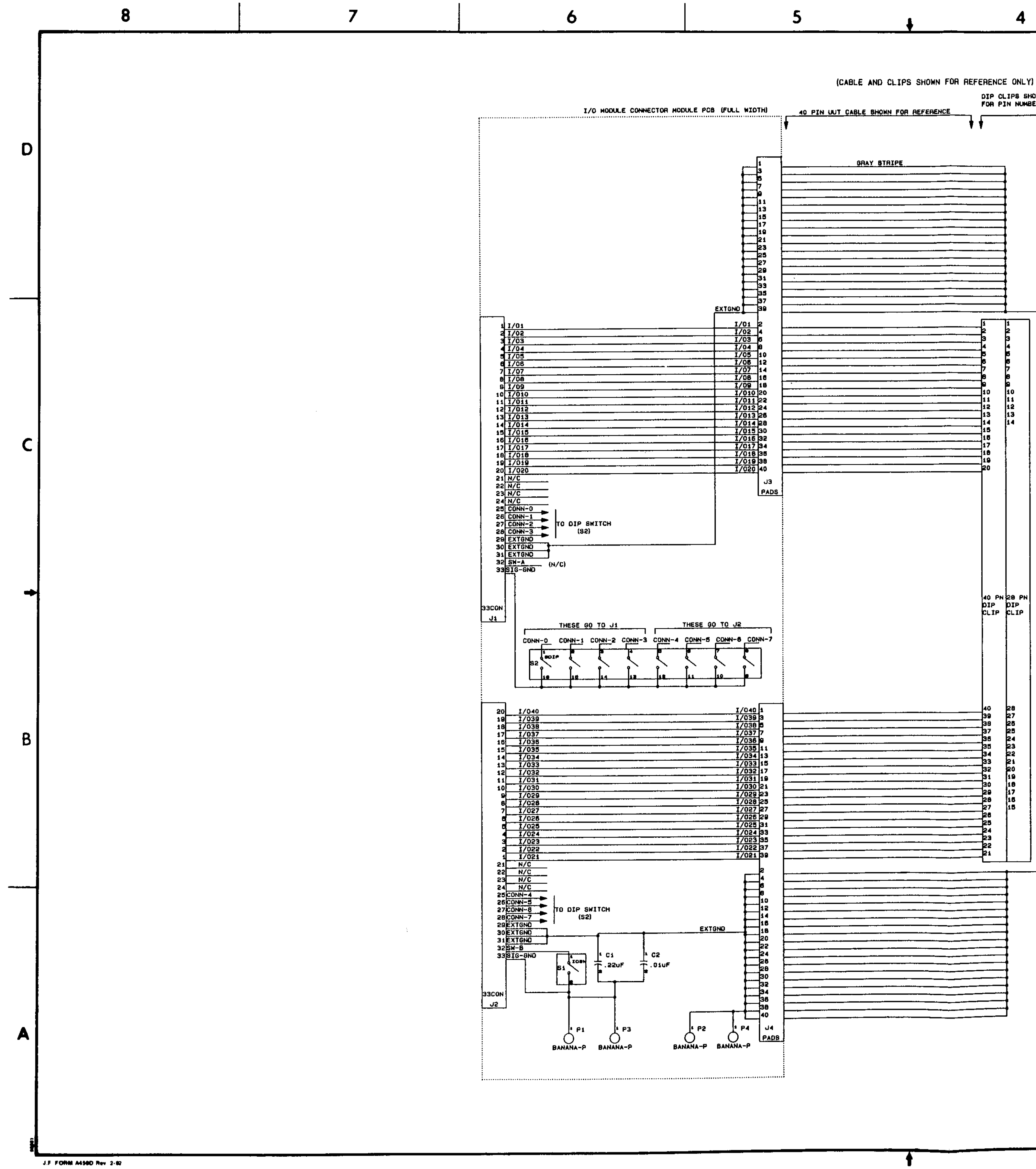
NOTES: UNLESS OTHERWISE SPECIFIED.

1. J3 AND J4 ARE REALLY ARRAYS OF SOLDER PADS WHERE THE CABLE ASSEMBLY WILL SOLDER IN.
2. SWITCH S1 IS THE "IO" SWITCH. ACCESSIBLE FROM THE OUTSIDE OF THE MODULE.
3. ALL RESISTOR VALUES ARE IN OHMS 1/8W, 5%.
4. ALL CAPACITOR VALUES ARE IN MICROFARADS.

DES	LAST USED	NOT USED
J	J4	—
P	P4	—
S	S2	—
C	C2	—

9100A-1013

Figure 7-13. A13 DIP Clip Module (Full)



(CABLE AND CLIPS SHOWN FOR REFERENCE ONLY)
I/O MODULE CONNECTOR MODULE PCB (FULL WIDTH)
40 PIN UUT CABLE SHOWN FOR REFERENCE
GRAY STRIPE
EXTGND
TO DIP SWITCH (S2)
THESE GO TO J1
THESE GO TO J2
CONN-0
CONN-1
CONN-2
CONN-3
CONN-4
CONN-5
CONN-6
CONN-7
33CON J1
33CON J2
J3 PADS
J4 PADS
40 PN DIP CLIP
28 PN DIP CLIP
C1 .22uF
C2 .01uF
P1
P2
P3
P4
BANANA-P

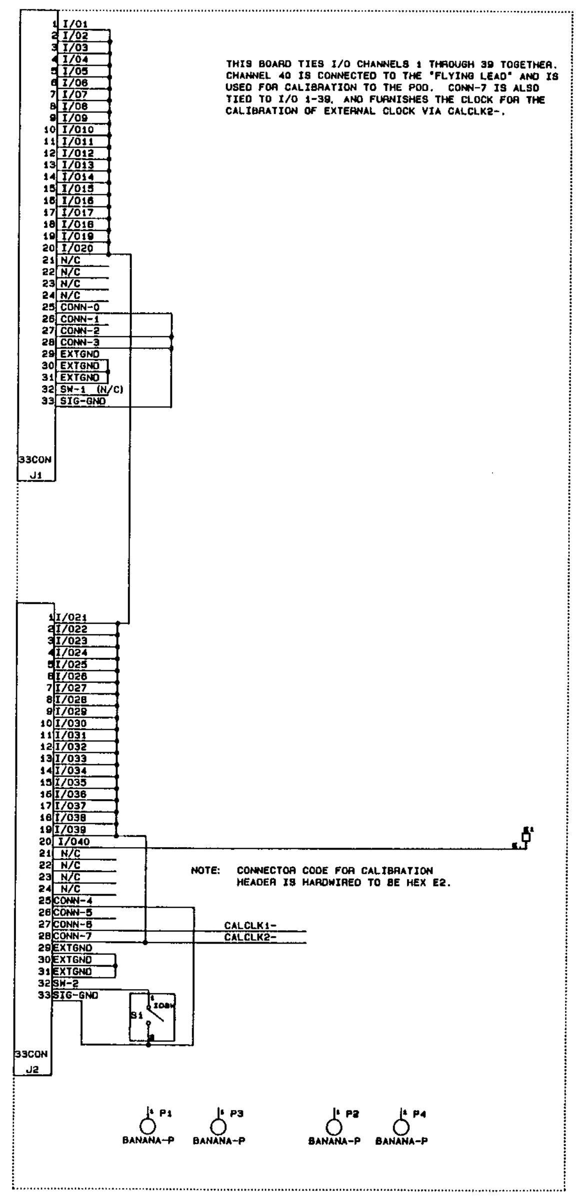
8 7 6 5 4 3 2 1

D C B A

NOTES: UNLESS OTHERWISE SPECIFIED.

1. *ALL RESISTOR VALUES ARE IN OHMS, 1/8W, 5%.*
2. *ALL CAPACITOR VALUES ARE IN MICROFARADS.*
3. *FOR ASSEMBLY DRAWING SEE 9100A-4014.*
4. *CHANGES TO THIS SCHEMATIC MUST BE MADE THRU FUTURENET, CAD DATA BASE NO. 9100-1014:FD.*

DES	LAST USED	NOT USED
J	J2	
P	P4	
S	S1	
E	E1	



9100A-1014

J F FORM A4560 Rev 2-82

Figure 7-14. A14 Calibration Module PCA

8 7 6 5 4

D

C

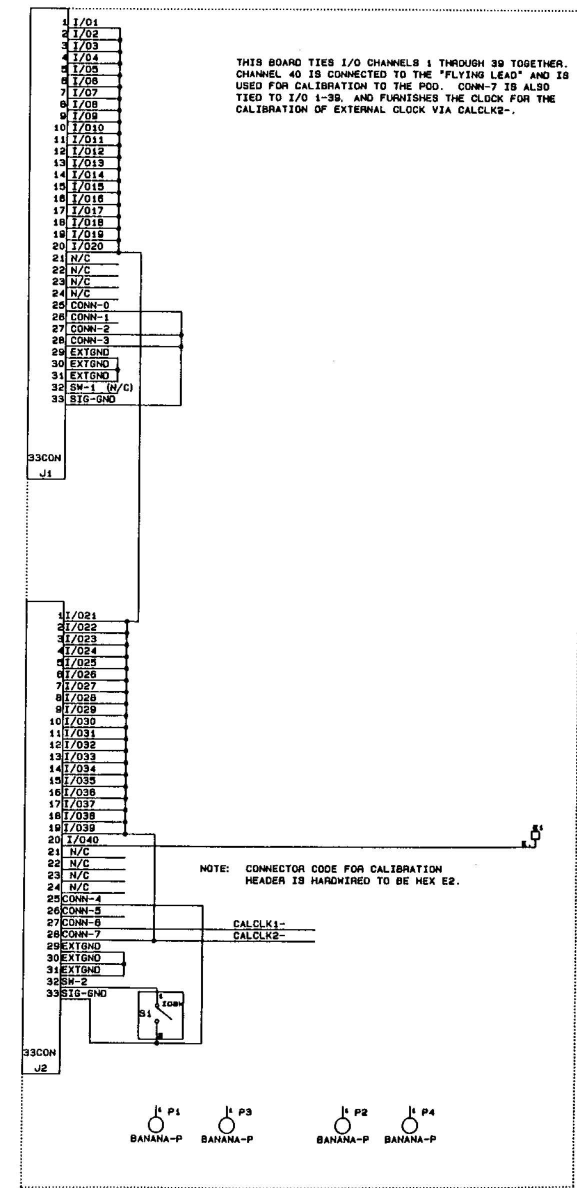
B

A

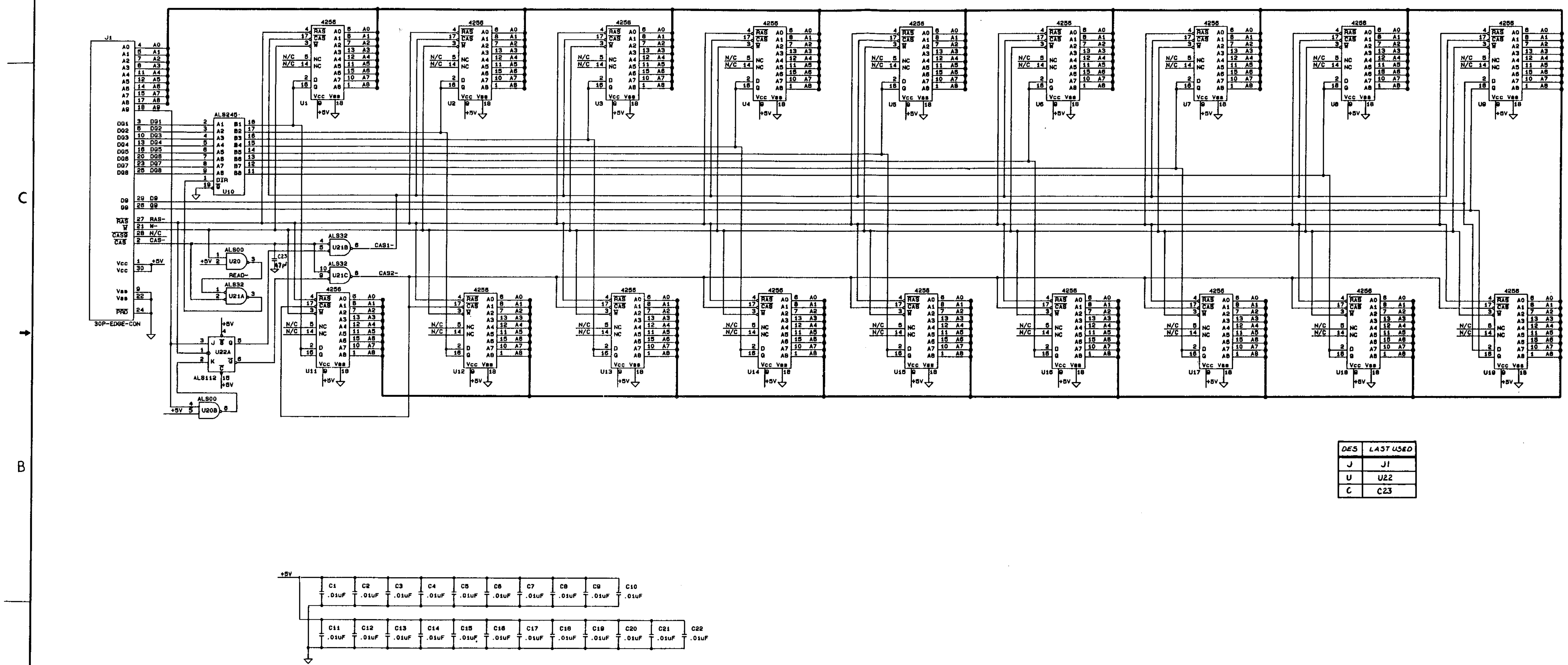
NOTES: UNLESS OTHERWISE SPECIFIED.

1. *ALL RESISTOR VALUES ARE IN OHMS, 1/8W, 5%.*
2. *ALL CAPACITOR VALUES ARE IN MICROFARADS.*
3. *FOR ASSEMBLY DRAWING SEE 9100A-4014.*
4. *CHANGES TO THIS SCHEMATIC MUST BE MADE THRU FUTURENET, CAD DATA BASE NO. 9100-1014: FD.*

DES	LAST USED	NOT USED
J	J2	
P	P4	
S	S1	
E	E1	



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL CAPACITOR VALUES ARE IN MICROFARADS.
2. FOR REFERENCE DESIGNATION DRAWING SEE 9100A-1616, FOR ASSEMBLY DRAWING SEE 9100A-4016.
3. CHANGES TO THIS SCHEMATIC MUST BE MADE THRU FUTURENET, CAD DATA BASE NO. 9100A-1016: FD.
4. **WARNING:** Ⓢ INDICATES USAGE OF MOS DEVICE(S) WHICH MAY BE DAMAGED BY STATIC DISCHARGE. USE SPECIAL HANDLING PER S.O.P. 19.1

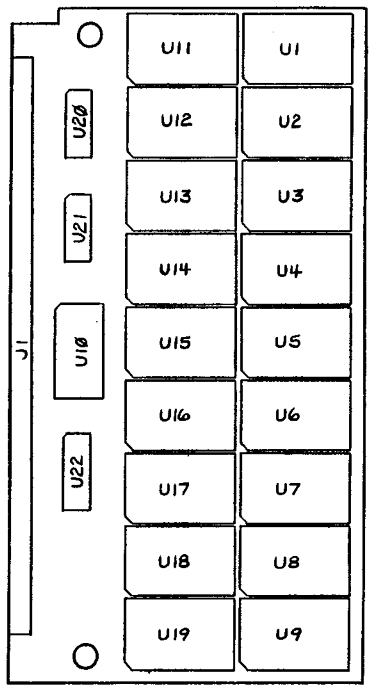


DES	LAST USED
J	J1
U	U22
C	C23

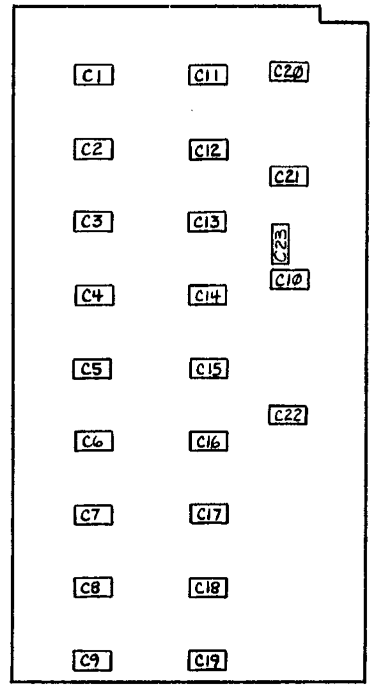
CAUTION
SUBJECT TO DAMAGE BY STATIC ELECTRICITY

9100A-1016

Figure 7-15. A16 512K RAM Module



CKT 4

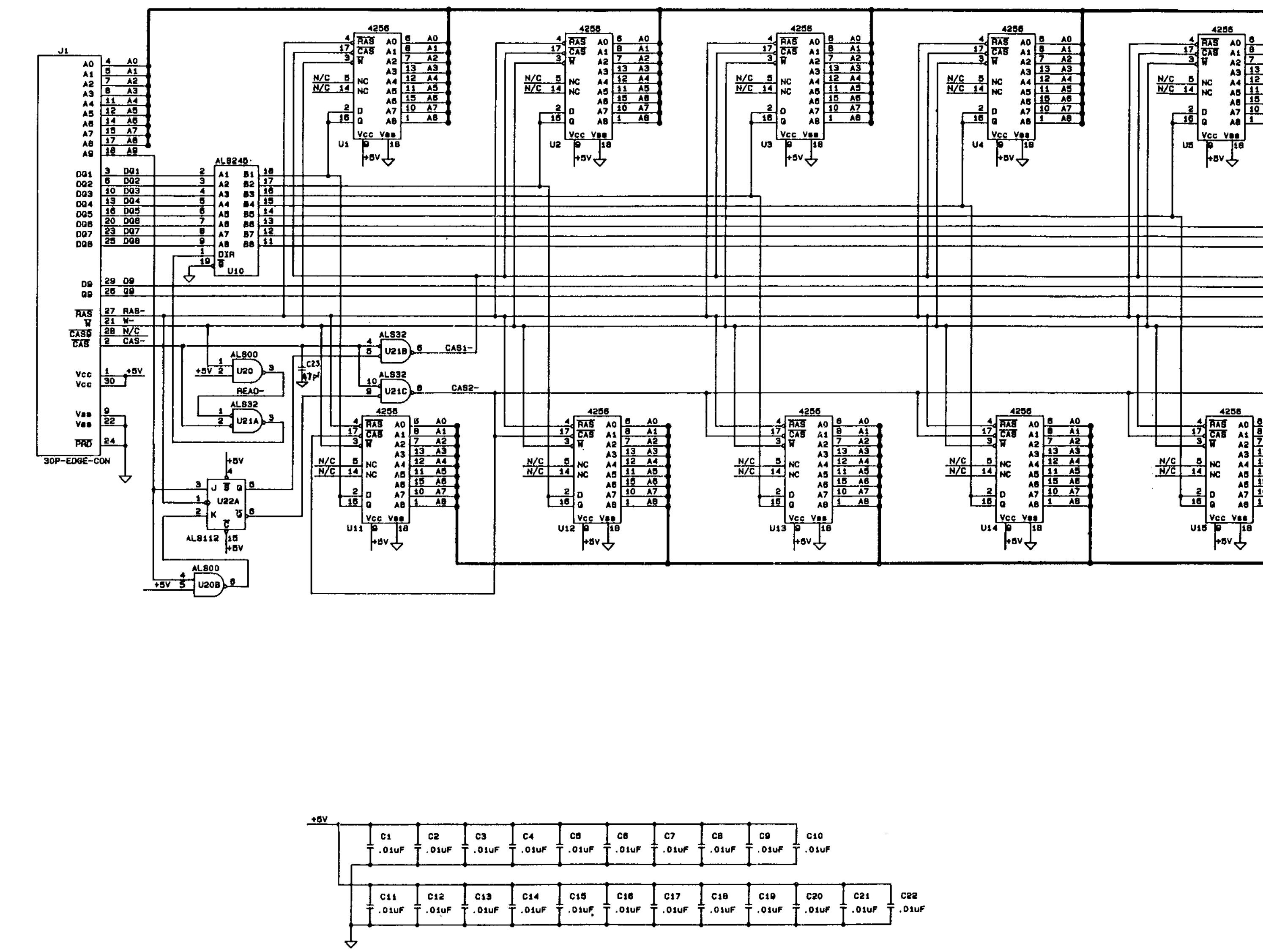


CKT 1

9100A-1616

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITOR VALUES ARE IN MICROFARADS.
2. FOR REFERENCE DESIGNATION DRAWING SEE 9100A-1616, FOR ASSEMBLY DRAWING SEE 9100A-4016.
3. CHANGES TO THIS SCHEMATIC MUST BE MADE THRU FUTURENET, CAD DATA BASE NO. 9100A-1016:FD.
4. **WARNING:** INDICATES USAGE OF MOS DEVICE(S) WHICH MAY BE DAMAGED BY STATIC DISCHARGE. USE SPECIAL HANDLING PER S.O.P. 19.1



CAUTION
SUBJECT TO DAMAGE BY STATIC ELECTRICITY

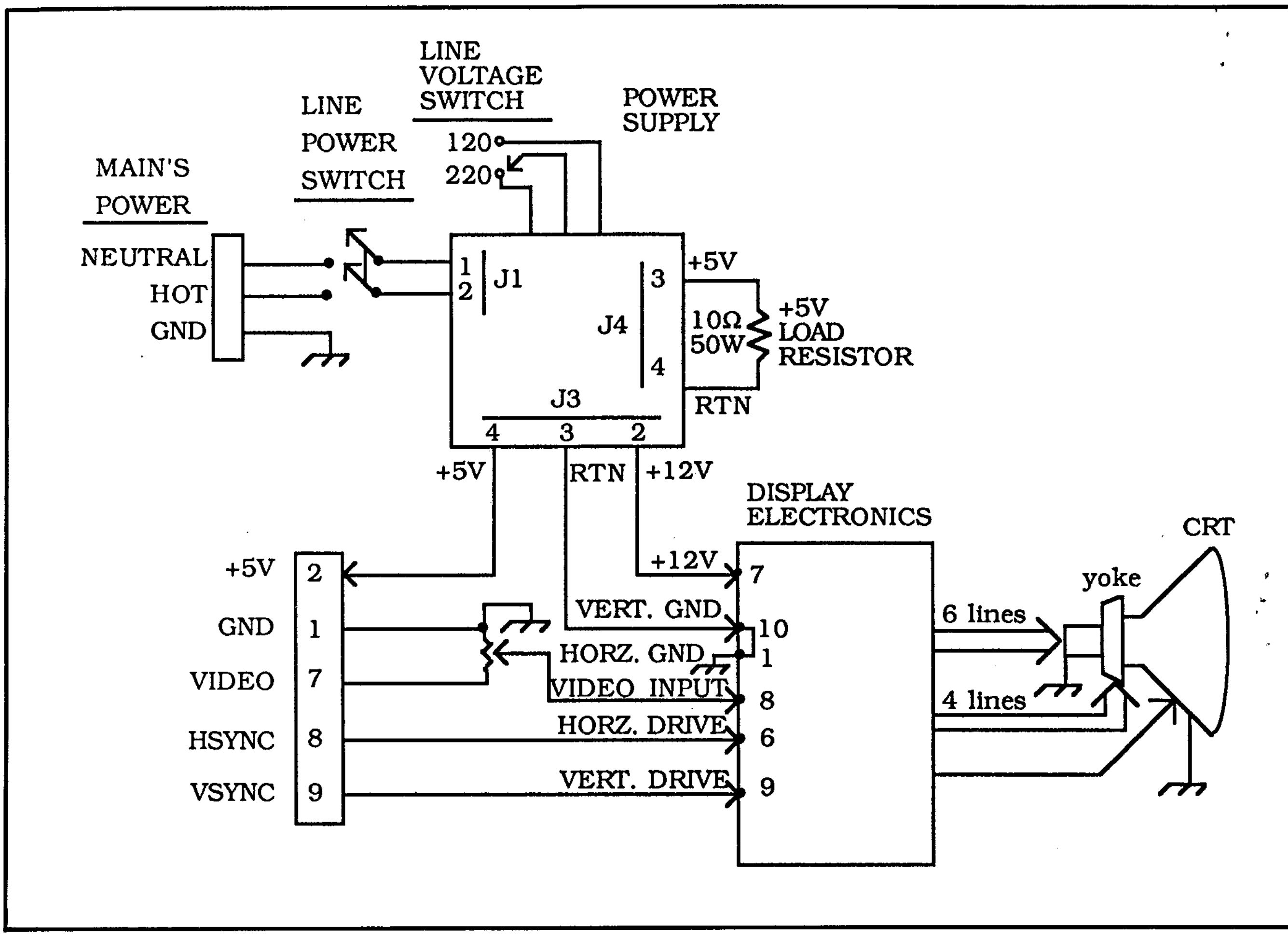


Figure 7-16. A19 Monochrome Monitor, Block Diagram

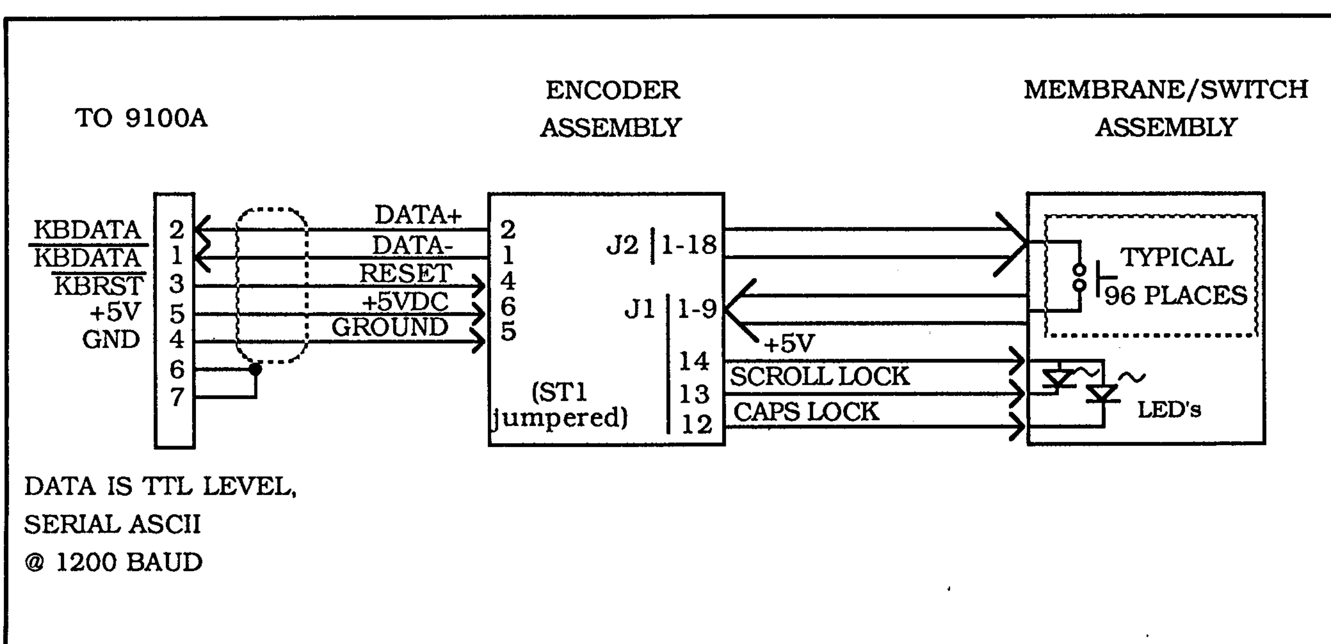


Figure 7-17. -013 Programmer's Keyboard, Block Diagram

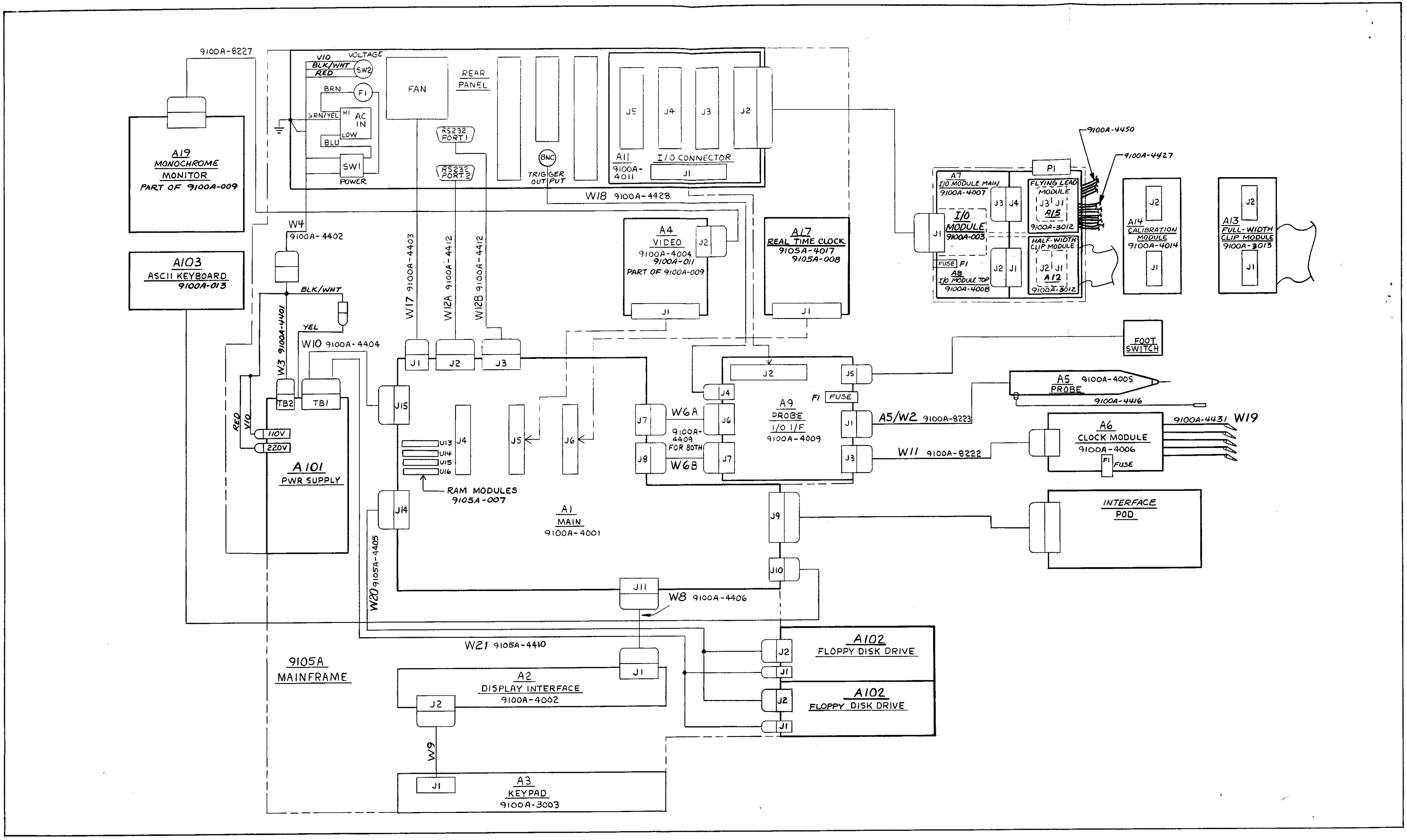


Figure 7-19. Interconnect Diagram, 9105A

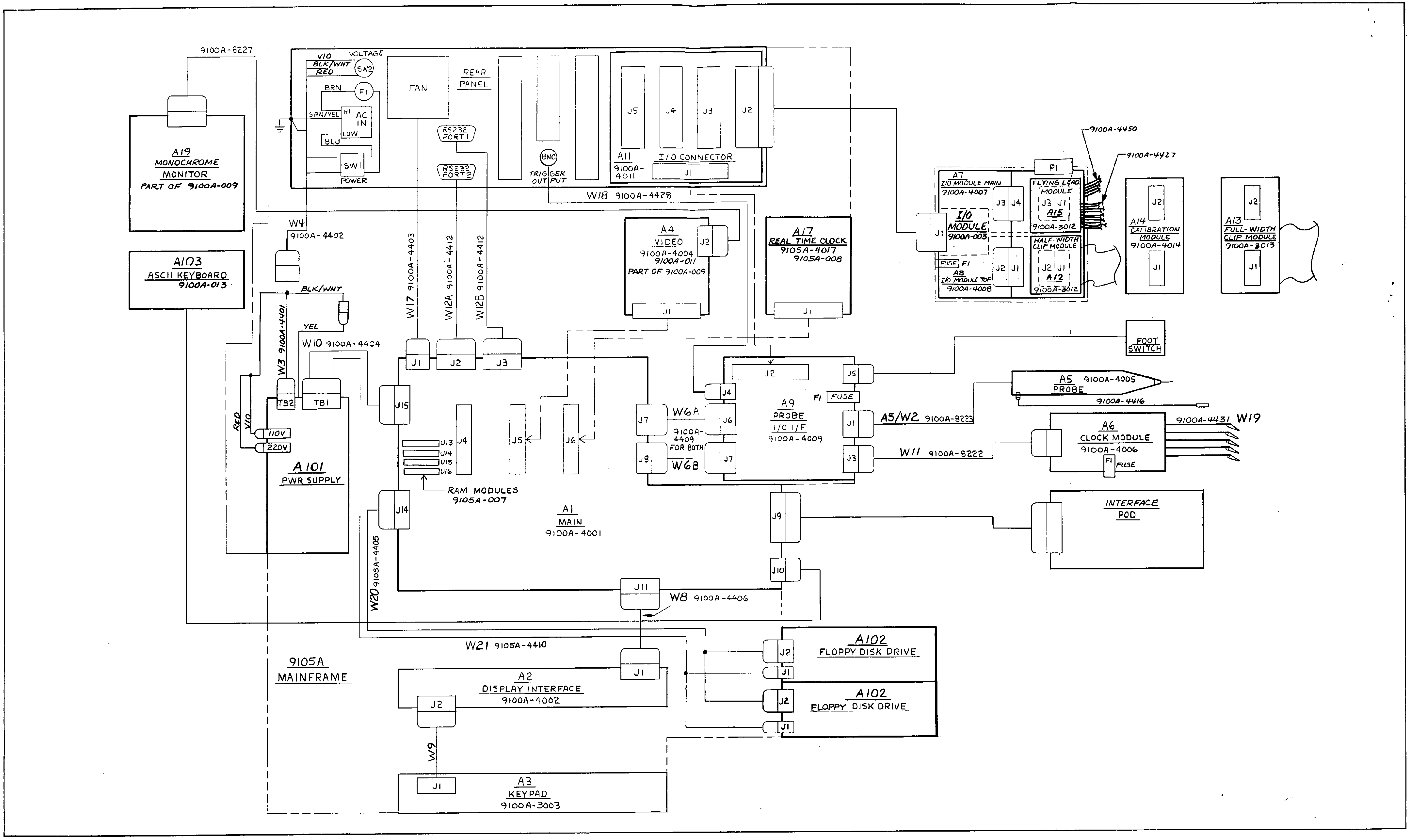


Figure 7-19. Interconnect Diagram, 9105A